AN2339
Application note

STR91x hardware development getting started

Introduction

The STR91x MCUs are derivatives of the STMicroelectronics STR9 family of 32-bit 0.18µ HCMOS microcontrollers. They combine high CPU performance (CPU frequency up to 96 MHz) with rich peripheral functionalities and enhanced I/O capabilities. They offer up to 96 MIPS directly from Flash memory, very large SRAM with optional battery backup and support clock generation via PLL or via an external clock. The STR91x can perform signal-cycle DSP instructions good for speech processing, audio algorithms, and low-end imaging.

This application note provides a complement to the information in the STR91x datasheet and reference manual by describing the minimum hardware environment required to build an application around the STR91x. It's divided into six chapters: minimum hardware requirements, power supply, clock management, reset control, development and debugging tool support and basic schematic. Each chapter gives the hardware needed for each specific section and does not describe the STR91x blocks in detail. To get detailed description of these features, refer to STR91x datasheet and reference manual or STR910 Eval-Board datasheet.

Contents

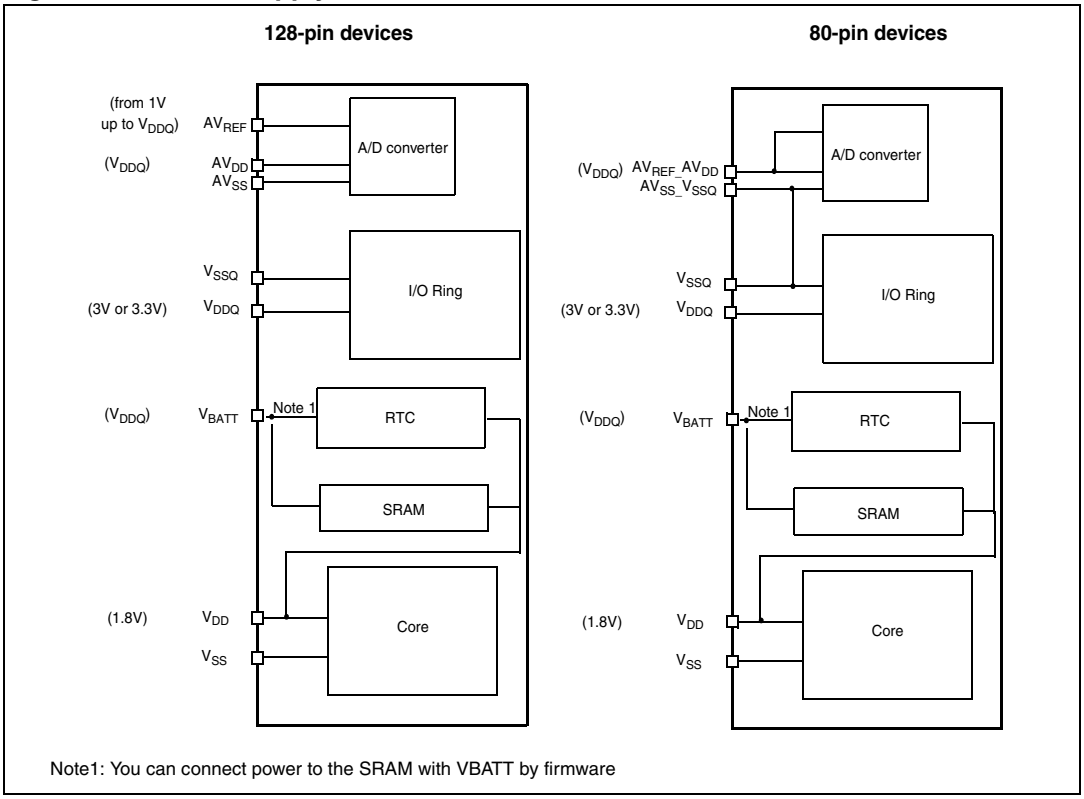
1 Hardware requirements summary

In order to build an application around STR91x, the application board should, at least, provide the following features:

- Power supply
- Clock management
- Reset control
- JTAG/Mictor connector

2 Power supply

Figure 1. Power Supply Overview



Note1: You can connect power to the SRAM with VBATT by firmware

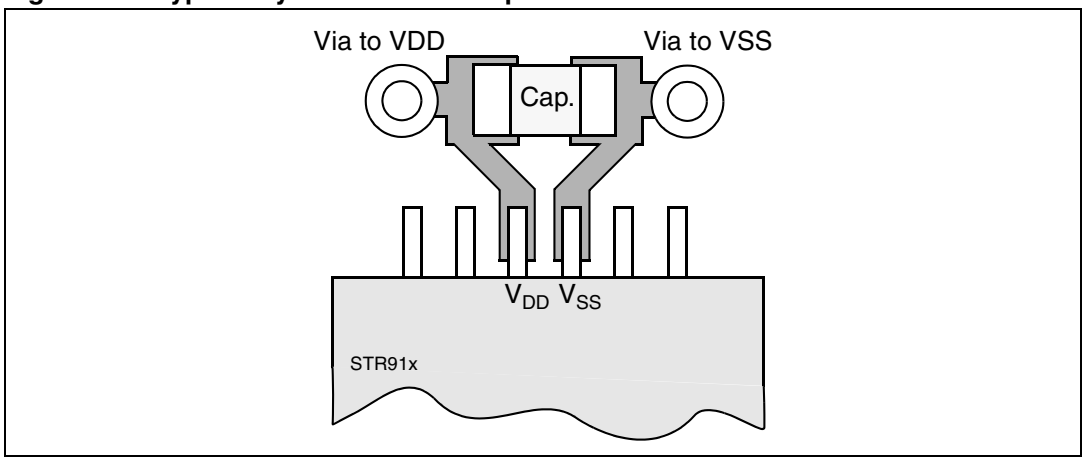
2.1 Main operating voltages

The STR91x devices are processed in 0.18 µm technology, ARM966E-S RISC core and I/O peripherals need different power supplies. In fact, STR91x requires two separate operating voltage supplies. The CPU and memories operate in a range from 1.65V to 2.0V on the VDD pins, and the I/O ring operates in the 2.7V to 3.3V or 3.0V to 3.6V range on the VDDQ pins.

All pins need to be properly connected to the power supplies. These connections, including pads, tracks and vias should have an impedance as low as possible. This is typically achieved with thick track widths and preferably dedicated power supply planes in multi-layer PCBs.

In addition, each VDD/VSS and VDDQ/VSSQ pair should be decoupled with ceramic capacitors which need to be placed as close as possible to the appropriate pins or below the pins on the contrary side of the PCB. Typical values are 10nF to 100nF, but exact values depend on the application needs. The following figure shows the typical layout on such a VDD/VSS pair.

Figure 2. Typical layout for VDD/VSS pair



2.2 Analog supply and reference

The ADC unit on 128-pin packages has an independent A/D Converter Supply and Reference Voltage. This means that it has an isolated analog voltage supply input at pin AVDD to accept a very clean voltage source. The analog voltage supply range on pin AVDD is the same range as the digital voltage supply on pin VDDQ. Additionally, an isolated analog supply ground connection is provided on pin AVSS only for further ADC supply isolation. They offer a separate external analog reference voltage input for the ADC unit on the AVREF pin for better accuracy on low voltage input, and the voltage on AVREF can range from 1.0V to VDDQ.

On 80-pin packages, the analog supply is shared with the ADC reference voltage pin, and the analog ground is shared with the digital ground at a single point in the STR91xF device on pin AVSS_VSSQ. Also the ADC reference voltage is tied internally to the ADC unit supply voltage on pin AVCC_AVREF, meaning the ADC reference voltage is fixed to the ADC unit supply voltage.

2.3 Battery backup supply

You can optionally connect a battery to the VBATT pin (2.5V to 3.5V) of the STR91x so that SRAM contents are automatically preserved when the normal operating voltage on the VDD pin is lost or drops below the 1.4V threshold. Automatic switchover of VBATT power to SRAM can be disabled by firmware if you want the battery to power only the RTC and not the SRAM.

Note: 1 You are advised to ground all unused pins on ports 0-9 to reduce noise susceptibility, noise generation, and minimize power consumption. There are no internal or programmable pull-up resistors on ports 0-9.

2 All pins on ports 0-9 are 5V tolerant

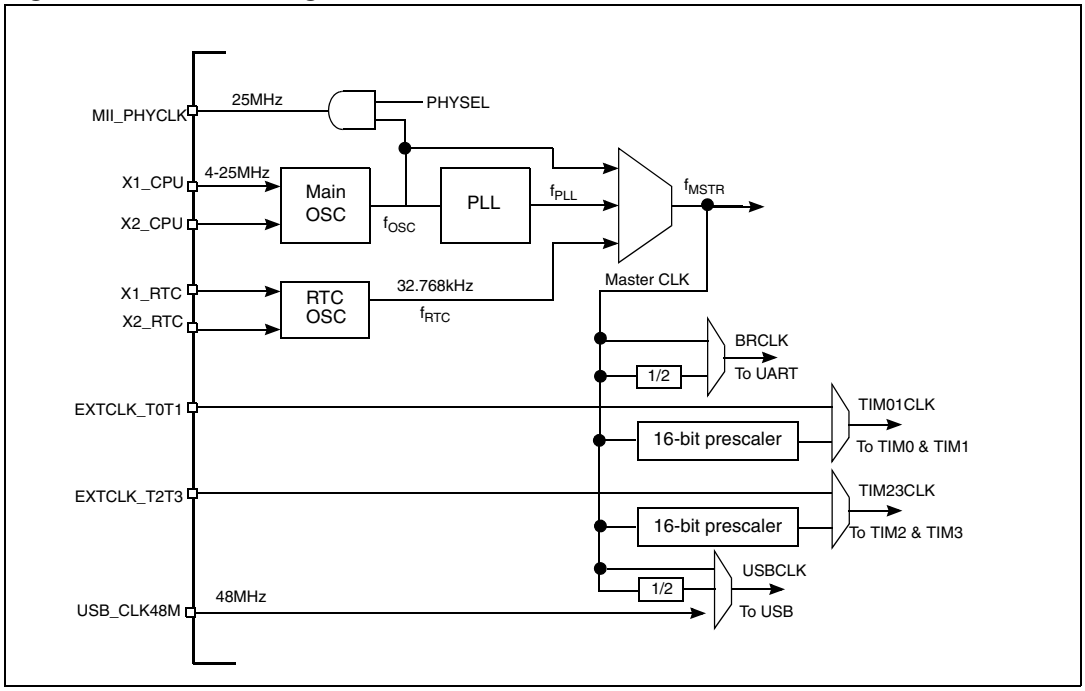
3 Pins on ports 0,1,2,4,5,7,8,9 have 4 mA drive and 4 mA sink. Ports 3 and 6 have 8 mA drive and 8 mA sink.

For more details on the power supply, refer to the STR91xF datasheet.

3 Clock management

The STR91x offers a flexible way for selecting the core and peripheral clocks, the devices have up to four external clock source inputs: Main Oscillator, RTC, USB Clock and TIM clocks. It also provides one output clock.

Figure 3. Clock Management

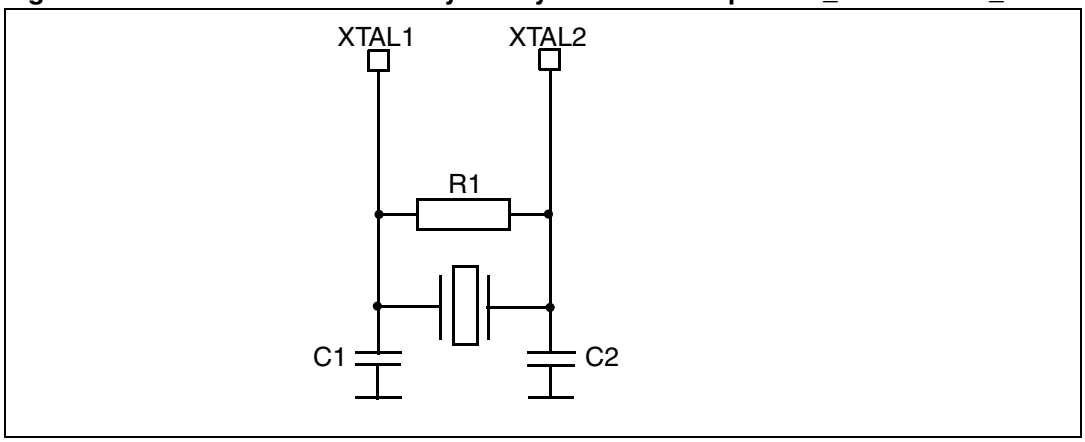


3.1 Main oscillator

The source for the main oscillator input is a 4 to 25 MHz external crystals connected to STR91xF pins X1_CPU and X2_CPU or an external oscillator device connected to pin X1_CPU, in this case the X2_CPU pin can be left open and not used.

The recommended circuitry for a crystal is shown below. C1, C2 and R1 values depend greatly on the crystal type and manufacturer. You should ask your crystal supplier for the best values for these components.

Figure 4. Recommended circuitry for crystal oscillator pins X1_CPU and X2_CPU



The values of the load capacitors C1 and C2 also heavily depend on the crystal type and frequency. For best oscillation stability they normally have the same value. Typical values are in the range from below 10pF up to 30pF. The parasitic capacitance of the board layout also needs to be considered and typically adds a few pF to the component values. The resistor R1 is recommended for feedback stability and has a value of around 1MΩ.

Note: In the PCB layout all connections should be as short as possible. Any additional signals, especially those that could interfere with the oscillator, should be locally separated from the PCB area around the oscillation circuit using suitable shielding.

3.2 Real time clock

3.2.1 External crystal

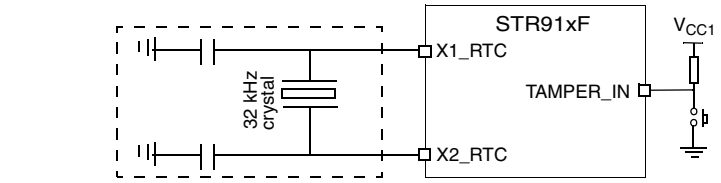
A 32.768 kHz external crystal can be connected to pins X1_RTC and X2_RTC, or an external oscillator connected to pin X1_RTC to constantly run the real time clock unit. This 32.768 kHz clock source can also be used as an input to the clock control unit to run the CPU in slow clock mode for reduced power.

3.2.2 Tamper detection

On 128-pin STR91xF devices only, there is a tamper detect input pin, TAMPER_IN, used to detect and record the time of a tamper event on the end product such as malicious opening of an enclosure, unwanted opening of a panel, etc. The activation mode of the tamper pin is programmable to one of two modes:

1. One is Normally Closed/Tamper Open.
2. The second mode will detect when a signal on the tamper input pin is driven from low-to-high, or high-to-low depending on firmware configuration.

Figure 5. 32.768 kHz oscillator



For more details concerning capacitance, refer to the crystal manufacturer datasheet.
V_{CC1} can be:

V_{BATT}: if you want to preserve tamper function when V_{DD} and V_{DDQ} are switched off.
V_{DDQ}: if you don't want to preserve tamper function when V_{DD} and $V_{DDQ}$are switched off

3.3 USB clock

STR91x contains a USB 2.0 Full Speed device module interface that operates at a precise frequency of 48 MHz. This clock is usually provided by an external oscillator connected to the USB clock pin USB_CLK48M. However, to save board space and cost, the 48 MHz USB clock can also be generated by the internal PLL using one single external oscillator for both system and USB module.

Note: Care is required when programming the PLL multiplier and divider factors, not to exceed the maximum allowed operating frequency (96 MHz). At power up, the CPU defaults to run the oscillator clock, as the PLL is not ready (locked). The LOCK bit is set when the PLL clock has stabilized.

3.4 TIM clock

Like the USB interface, TIM0/TIM1 and TIM2/TIM3 can receive an external clock on pin EXTCLK_T0T1 and EXTCLK_T2T3 respectively.

3.5 Output clock

The STR91xF devices can optionally output a 25 MHz clock to the external Ethernet PHY interface device via output pin MII_PHYCLK, in this case, the STR91xF must use a 25 MHz signal on its main oscillator input. The advantage here is that an inexpensive 25 MHz crystal may be used to source a clock to both STR91xF and the external PHY device. Alternatively an external 25 MHz oscillator can be connected directly to the external PHY interface device. In this case the STR91xF can use a crystal at a frequency other than 25 MHz.

4 Reset control

There are two types of internal hardware reset, defined as System Reset and Global Reset. The STR91x device also provides a Reset output signal.

4.1 Reset input

4.1.1 System Reset

A system reset resets all registers except the Clock Control Register, PLL Configuration Register, System Status Register, Flash Configuration register, Protection register and the FMI Bank address and Bank size Registers.

A system reset is generated when one of the following events occurs:

- A low level on the RESET_INn pin (External Reset):
  - This input signal is active low. It has no internal pull-up to VDDQ. A valid active-low input signal of t_{RINMIN} = 100ns.
- JTAG Reset Command (JTAG reset):

  The JTAG interface has two reset signals connected to the debug target hardware:
  - **nTRST** drives the JTAG **nTRST** signal on the ARM processor core. It is an open collector output that is activated whenever the In-Circuit Emulators (ICE) software has to re-initialize the debug interface in the target system.
  - **nSRST** is a bidirectional signal that both drives and senses the system reset signal on the target. The open collector output is driven LOW by the debugger to re-initialize the target system.
- Watchdog reset
  - In Watchdog mode, a reset is generated when the counter reaches the end of count.

For more details, refer to *Section 5.1: JTAG interface on page 12*

*Note: If the **nRESET** and **nTRST** signals are linked together, resetting the system also resets the TAP controller.*

4.1.2 Global Reset

A global reset sets all the registers to their reset values, it is generated when one of the following events occurs:

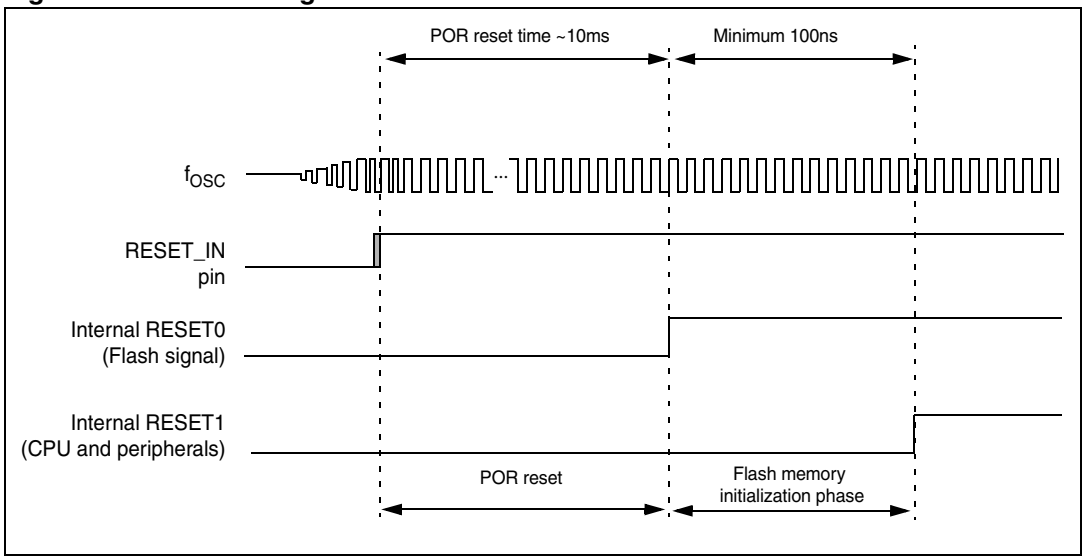
LVD circuitry

LVD circuitry will always cause a global reset if the CPU V_{DD} source drops below it's fixed threshold of 1.4V. However, the LVD trigger threshold to cause a global reset for the I/O ring's V_{DDQ} source is set to one of two different levels, depending on the V_{DDQ} operating range. If V_{DDQ} operation is at 2.7V to 3.3V, the LVD dropout trigger threshold is 2.4V. If V_{DDQ} operation is 3.0V and 3.6V, the LVD threshold is 2.7V.

Power On Reset (POR reset)

Internal reset is active until VDDQ and VDD are both above the LVD thresholds. This POR condition has a duration of t_{POR} (10ms min), after which the CPU fetches the first instruction from address 0x0000 0000.

Figure 6. Reset timing



4.2 Reset output

The RESET_OUT pin can be used to reset other application components when a system or global reset occurs.

5 Development and debugging tool support

The STR91xF device supports connection to both In-Circuit Emulators (ICE) via standard JTAG interface and trace tools via an Embedded Trace Macrocell (ETM9) interface.

5.1 JTAG interface

The STR91x has a user debug interface. It contains a six-pin serial interface conforming to JTAG, IEEE standard 1149.1-1993, “Standard Test Access Port-Scan Boundary Architecture”. JTAG allows the ICE device to be plugged to the board and used to debug the software running on the STR91x.

JTAG emulation allows the core to be started and stopped under control of the connected debugger software. The user can then display and modify registers and memory contents, and set break and watch points.

5.1.1 JTAG interface pins

The JTAG interface pins consist of the following signals:

Table 1. JTAG interface signals

Std name	STR91x name	Direction/ Description	Function
nTRST	JTRST	Test Reset (from JTAG equipment)	This active LOW open-collector is used to reset the JTAG port and the associated debug circuitry. It is asserted at power-up by each module, and can be driven by the JTAG equipment.
TDI	JTDI	Test data in (from JTAG equipment)	TDI goes down the stack of modules to the motherboard and then back up the stack, labelled TDO, connecting to each component in the scan chain.
TMS	JTMS	Test mode select (from JTAG equipment)	TMS controls transitions in the tap controller state machine. TMS connects to all JTAG components in the scan chain as the signal flows down the module stack.
TCK	JTCK	Test clock (from JTAG equipment)	TCK synchronizes all JTAG transactions. TCK connects to all JTAG components in the scan chain. Series termination resistors are used to reduce reflections and maintain good signal integrity. TCK flows down the stack of modules and connects to each JTAG component. However, if there is a device in the scan chain that synchronizes TCK to some other clock, then all down-stream devices are connected to the RTCK signal on that component.

Table 1. JTAG interface signals

Std name	STR91x name	Direction/ Description	Function
RTCK	JRTCK	Return TCK (to JTAG equipment)	The RTCK signal is returned by the core to the JTAG equipment, and the clock is not advanced until the core had captured the data. In adaptive clocking mode, the debugging equipment waits for an edge on RTCK before changing TCK.
TDO	JTDO	Test data out (to JTAG equipment)	TDO is the return path of the data input signal TDI.
nSRST	nRSTIN	System reset (bidirectional)	nSRST is an active LOW open-collector signal that can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when a board has been reset by the user. When the signal is driven LOW by the reset controller on the core module, the motherboard resets the whole system by driving nSYSRST low.
DBGRQ	GND (not used)	Debug request (from JTAG equipment)	DBGRQ is a request for the processor core to enter debug state.
DBGACK	GND (not used)	Debug acknowledge (to JTAG equipment)	DBGACK indicates to the debugger that the processor core has entered debug mode.

The JTAG input signals have weak internal pull-up and pull-down resistors, but these are not always active:

- When debug protection is activated (JTAG permanently held in reset internally)
- At power up and down there may be a short duration where the power on reset is already released internally, but where the resistors are not yet active.

To avoid any floating input pins even for a very short period it is highly recommended to always provide additional external pull-up and pull-down resistors. This recommendation is valid whether the JTAG port is used or not.

The following table shows the recommended values and types:

Table 2. Recommended JTAG debug port components

Signal name	Recommended external resistor type
JTCK	Should have a pull-down between pin and VSSQ to enable hot swap and post-mortem debugging
JTDI	Pull-up between pin and VDDQ
JTDO	Pull-up between pin and VDDQ
JTMS	Pull-up between pin and VDDQ
JTRST	Pull-down between pin and VSSQ
JRTCK	Should have a pull-down to fix a stable value on that signal when debugging a non-synthesizable core.

Note: 1 The recommended value for pull-ups and pull-downs is 10kΩ, although the optimum value depends on the signal load. For example, pull-downs should be about 1kΩ when working with TTL logic.

2 It is recommended that you place the JTAG header as closely as possible to the STR91x device, because this minimizes any possible signal degradation caused by long PCB tracks.

5.1.2 JTAG signal integrity and maximum cable lengths

When using longer cables it is essential to consider the cable as a transmission line and to provide appropriate impedance matching, otherwise reflections occur.

With the typical situation at the target end (weak drivers, no impedance matching resistors) you can only expect reliable operation over short cables (approximately 30cm). If operation over longer cables is required:

- For very long cables, a solution is to buffer the JTAG signals through differential drivers, such as the LVDS cable. Reliable operation is possible over tens of metres using this technique.
- For intermediate lengths of cables, you can instead improve the circuitry used at the target end. The recommended solution is to add an external buffer with good current drive and a 100. series resistor for the **TDO** and **RTCK** signals

5.2 ETM interface

The STR91x supports the connection of an external Embedded Trace Module (ETM9) to provide real time code tracing of the ARM966E-S macrocell in an embedded system.

The ETM interface is primarily one-way. To provide code tracing, the ETM block must be able to monitor various ARM9E-S inputs and outputs. The required ARM9E-S inputs and outputs are collected and driven out from the ARM966E-S macrocell from the ETM interface registers.

In STR91x devices the ETM9 interface has nine pins in total, four of which are data lines, and all pins can be used for GPIO when tracing is no longer needed. The ETM9 interface is used in conjunction with the JTAG interface for trace configuration.

5.2.1 ETM Interface pins

The ETM interface pins consist of the following signals:

Table 3. ETM interface signals

Target board	STR91x name	Signal pin	Description
NC	Not used	1	No Connect
NC	Not used	3	No Connect
VSSQ	VSSQ	5	Signal ground
DBGRQ	Not used	7	Debug request
NSRST	nRSTIN	9	Open-collector output from the run control to the target system reset.
TDO	JTDO	11	Open-collector output from the run control to the target system reset
RTCK	JRTCK	13	Return test clock from the target JTAG port
TCK	JTCK	15	Test clock to the run control unit from the JTAG port
TMS	JTMS	17	Test mode select from run control to the JTAG port
TDI	JTDI	19	Test data input from run control to the JTAG port
NTRST	JNTRST	21	Active-low JTAG reset
Port A TRACEPKT[15]	Not used	23	The trace packet port
Port A TRACEPKT[14]	Not used	25	The trace packet port
Port A TRACEPKT[13]	Not used	27	The trace packet port
Port A TRACEPKT[12]	Not used	29	The trace packet port
Port A TRACEPKT[11]	Not used	31	The trace packet port
Port A TRACEPKT[10]	Not used	33	The trace packet port
Port A TRACEPKT[9]	Not used	35	The trace packet port
Port A TRACEPKT[8]	Not used	37	The trace packet port
NC	Not used	2	No Connect
NC	Not used	4	No Connect
Port A TRACECLK	ETM_TRCLK	6	Clocks trace data on rising edge or both edges
DBGACK	Not used	8	Debug acknowledge from the test chip, high when in debug state
EXTRIG	ETM_EXTRIG	10	Optional external trigger signal to the Embedded trace Macrocell (ETM)
VTRef	VDDQ	12	Signal level reference

Table 3. ETM interface signals

Target board	STR91x name	Signal pin	Description
Vsupply	V33	14	Supply voltage
Port A TRACEPKT[7]	Not used	16	The trace packet port
Port A TRACEPKT[6]	Not used	18	The trace packet port
Port A TRACEPKT[5]	Not used	20	The trace packet port
Port A TRACEPKT[4]	Not used	22	The trace packet port
Port A TRACEPKT[3]	ETM_PCK3	24	The trace packet port
Port A TRACEPKT[2]	ETM_PCK2	26	The trace packet port
Port A TRACEPKT[1]	ETM_PCK1	28	The trace packet port
Port A TRACEPKT[0]	ETM_PCK0	30	The trace packet port
Port A TRACESYNC	ETM_TRSYNC	32	Start of branch sequence signal
Port A PIPESTAT[2]	ETM_PSTAT2	34	RAM pipeline status
Port A PIPESTAT[1]	ETM_PSTAT2	36	RAM pipeline status
Port A PIPESTAT[0]	ETM_PSTAT1	38	RAM pipeline status

5.2.2 Minimizing signal skew (balancing PCB track lengths)

You must attempt to match the lengths of the PCB tracks carrying all of **TRACECLK**, **PIPESTAT**, **TRACESYNC,** and **TRACEPKT** from the STR91x to the Mictor connector to within approximately 0.5 inches (12.5mm) of each other. Any greater differences directly impact the setup and hold time requirements.

5.2.3 Minimizing crosstalk

Normal high-speed design rules must be observed. For example, do not run dynamic signals parallel to each other for any significant distance, keep them spaced well apart, and use a ground plane and so forth. Particular attention must be paid to the **TRACECLK** signal. If in any doubt, place grounds or static signals between the **TRACECLK** and any other dynamic signals.

5.2.4 Impedance matching and termination

Termination is almost certainly necessary, but there are some circumstances where it is not required. The decision is related to track length between the STR91x and the Mictor connector.

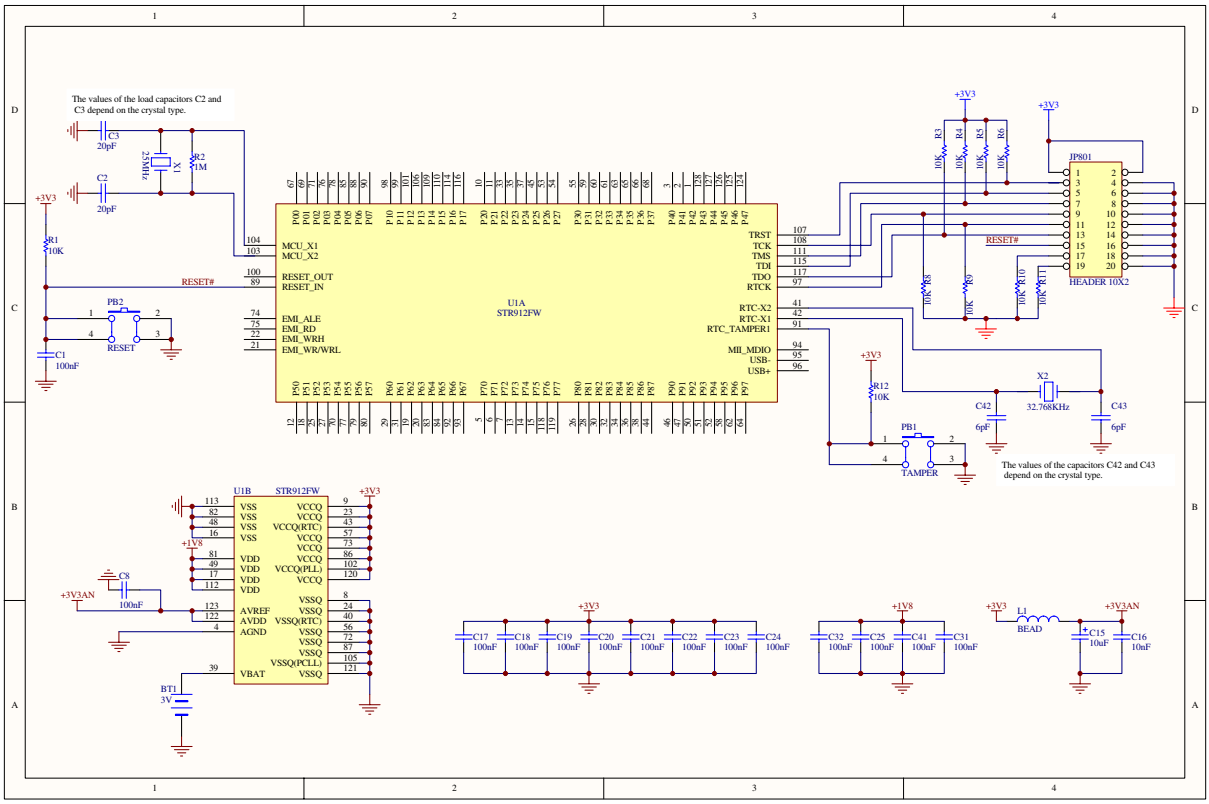
5.2.5 Rules for series terminators

Series (source) termination is the most commonly used method. The basic rules are:

1. The series resistor must be placed as close as possible to the STR91x pins (less than 0.5 inches)
2. The value of the resistor must equal the impedance of the track minus the output impedance of the output driver.
3. A source terminated signal is only valid at the end of the signal path. At any point between the source and the end of the track, the signal appears distorted because of reflections. Any device connected between the source and the end of the signal path therefore sees the distorted signal and might not operate correctly. Care must be taken not to connect devices in this way, unless the distortion does not affect device operation.

6 STR91x basic schematic

The following schematic describes the minimum hardware requirements to get the STR91x running.



7 Revision history

Table 4. Document revision history

Date	Revision	Changes
14-Apr-2006	1	Initial release.
10-May-2006	2	Added *Section 6: STR91x basic schematic*.