BAL-NRF01D3

50 Ω nominal input / conjugate match balun to nRF51422-QFAA, nRF24LE1, nRF51822-QFAA/AB, with integrated harmonic filter

Features
- 50 Ω nominal input / conjugate match to Nordic Semiconductor chips nRF24LE1 QFN32, nRF24AP2-1CH, nRF24AP2-8CH, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0)
- Low insertion loss
- Low amplitude imbalance
- Low phase imbalance
- Small footprint < 1.5 mm²

Benefits
- Very low profile < 595 μm after reflow
- High RF performance
- RF BOM and area reduction

Applications
- 2.45 GHz impedance matched balun filter
- Optimized for Nordic’s chip set nRF24LE1/AP2, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0)

Description
STMicroelectronics BAL-NRF01D3 is an ultramiiniature balun. The device integrates matching network and harmonics filter. Matching impedance has been customized for the following Nordic Semiconductor circuits: nRF24LE1 QFN-32 pins, nRF24AP2-1CH, nRF24AP2-8CH, nRF51422-QFAA (build code CA/C0), nRF51822-QFAA (build code CA/C0) and nRF51822-QFAB (build code AA/A0).

The device uses STMicroelectronics’ IPD technology on a non-conductive glass substrate to optimize RF performance.

The BAL-NRF01D3 has been tested and approved by Nordic Semiconductor in their nRF2723 and nRF2752 nRFgo modules.

Figure 1: Application schematic

![Application schematic](5 bumps)
# Characteristics

## Table 1: Absolute maximum ratings (limiting values)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIN</td>
<td>Input power RFIN</td>
<td>-</td>
<td>20 dBm</td>
</tr>
<tr>
<td>VESD</td>
<td>ESD ratings MIL STD883C (HBM: $C = 100 \text{ pF}, R = 1.5 \Omega, \text{ air discharge}$)</td>
<td>2000</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>ESD ratings charge device model (JESD22-C101-C)</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>ESD ratings machine model (MM: $C = 200 \text{ pF}, R = 25 \text{ W}, L = 500 \text{ nH}$)</td>
<td>200</td>
<td>-</td>
</tr>
<tr>
<td>TOP</td>
<td>Operating temperature</td>
<td>-40</td>
<td>-105 °C</td>
</tr>
</tbody>
</table>

## Table 2: Impedances ($T_{\text{amb}} = 25 \degree \text{C}$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZOUT</td>
<td>Nominal differential output impedance</td>
<td>-</td>
<td>- Ω</td>
</tr>
<tr>
<td>ZIN</td>
<td>Nominal input impedance</td>
<td>50</td>
<td>- Ω</td>
</tr>
</tbody>
</table>

## Table 3: RF performance ($T_{\text{amb}} = 25 \degree \text{C}$)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>Frequency range (bandwidth) 2400 2540</td>
<td>2400 2540</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>IL</td>
<td>Insertion loss in bandwidth</td>
<td>2.25</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RL</td>
<td>Return loss in bandwidth</td>
<td>10</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$\phi_{\text{imb}}$</td>
<td>Phase imbalance</td>
<td>3</td>
<td>°</td>
<td></td>
</tr>
<tr>
<td>$A_{\text{imb}}$</td>
<td>Amplitude imbalance</td>
<td>0.1</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>2f0</td>
<td>2nd harmonic filtering</td>
<td>4880 MHz</td>
<td>10</td>
<td>dB</td>
</tr>
<tr>
<td>3f0</td>
<td>3rd harmonic filtering</td>
<td>7320 MHz</td>
<td>20</td>
<td>dB</td>
</tr>
</tbody>
</table>
1.1 RF measurement

![Figure 2: Transmission (T\text{amb} = 25 °C)](image)

![Figure 3: Return loss on SE port (T\text{amb} = 25 °C)](image)

![Figure 4: Return loss on DIFF port (T\text{amb} = 25 °C)](image)

![Figure 5: Amplitude imbalance (T\text{amb} = 25 °C)](image)

![Figure 6: Phase imbalance (T\text{amb} = 25 °C)](image)
2 Application information

Figure 7: Application schematic (courtesy of Nordic Semiconductor)

Figure 8: nRF2723 application board (courtesy of Nordic Semiconductor)
Figure 9: nRF2752 application board (courtesy of Nordic Semiconductor)
3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

- Epoxy meets UL94, V0
- Lead-free package

3.1 Flip-Chip 5 bumps package information

**Figure 10: Flip-Chip 5 bumps package outline**

![Flip-Chip 5 bumps package outline](image)

**Table 4: Flip-Chip 5 bumps dimensions**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>X dimension of the die</td>
<td>1445</td>
<td>1485</td>
<td>1525</td>
<td>mm</td>
</tr>
<tr>
<td>Y</td>
<td>Y dimension of the die</td>
<td>980</td>
<td>1020</td>
<td>1060</td>
<td>mm</td>
</tr>
<tr>
<td>A</td>
<td>X pitch</td>
<td>604</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>B</td>
<td>Y pitch</td>
<td>500</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>A1</td>
<td>Distance from bump to edge of die on X axis</td>
<td>224</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>B1</td>
<td>Distance from bump to edge of die on Y axis</td>
<td>260</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>A2</td>
<td>Distance from VCC bump to SE bump on X axis</td>
<td>433</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>B2</td>
<td>Distance from bump to edge of die on Y axis</td>
<td>510</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>C</td>
<td>GND, VCC bump to SE bump pitch</td>
<td>500</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>D</td>
<td>Bump diameter</td>
<td>240</td>
<td>255</td>
<td>260</td>
<td>mm</td>
</tr>
<tr>
<td>T1</td>
<td>Substrate thickness</td>
<td>425</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>H</td>
<td>Bump height</td>
<td>205</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>T</td>
<td>Total die thickness</td>
<td>570</td>
<td>630</td>
<td>690</td>
<td>mm</td>
</tr>
</tbody>
</table>
3.2 Flip-chip 5 bumps packing information

Figure 11: Footprint - 3 mils stencil - non solder mask defined
Copper pad diameter:
220 µm recommended
180 µm minimum
260 µm maximum
Solder mask opening:
320 µm recommended
300 µm minimum
340 µm maximum
Solder stencil opening:
220 µm recommended
*depending on paste, it can go down to 270 µm

Figure 12: Footprint - 3 mils stencil - solder mask defined
Solder mask opening:
220 µm recommended
180 µm minimum
260 µm maximum
Copper pad diameter:
320 µm recommended
300 µm minimum
Solder stencil opening:
220 µm recommended
*depending on paste, it can go down to 270 µm

Figure 13: Footprint - 5 mils stencil - non solder mask defined
Copper pad diameter:
220 µm recommended
180 µm minimum
260 µm maximum
Solder mask opening:
320 µm recommended
300 µm minimum
340 µm maximum
Solder stencil opening:
330 µm recommended

Figure 14: Footprint - 5 mils stencil - solder mask defined
Solder mask opening:
220 µm recommended
180 µm minimum
260 µm maximum
Copper pad diameter:
320 µm recommended
300 µm minimum
Solder stencil opening:
330 µm recommended
*depending on paste, it can go down to 270 µm

Figure 15: Marking
Dot, ST logo
□ ECOPACK grade
xx = marking
z = manufacturing location
yww = datecode
Figure 16: Flip Chip tape and reel specifications

More packing information is available in the application note:
- AN2348 Flip-Chip: “Package description and recommendations for use”
- AN4111: “BAL-NRF01D3 matched balun with integrated harmonics filter for Nordic Semiconductor chips with ultralow power transceivers”
4 Ordering information

Table 5: Ordering information

<table>
<thead>
<tr>
<th>Order code</th>
<th>Marking</th>
<th>Package</th>
<th>Weight</th>
<th>Base qty.</th>
<th>Delivery mode</th>
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</thead>
<tbody>
<tr>
<td>BAL-NRF01D3</td>
<td>SC</td>
<td>Flip-Chip package (5 bumps)</td>
<td>1.82 mg</td>
<td>5000</td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

5 Revision history

Table 6: Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
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</thead>
<tbody>
<tr>
<td>15-Oct-2012</td>
<td>1</td>
<td>First issue.</td>
</tr>
<tr>
<td>13-Nov-2012</td>
<td>2</td>
<td>Added references to nRF51 series. Added Figure 9. Updated y-axis labels in Figure 2.</td>
</tr>
<tr>
<td>04-Mar-2013</td>
<td>3</td>
<td>Updated footprint illustrations in Figure 13, and Figure 14.</td>
</tr>
<tr>
<td>06-Aug-2013</td>
<td>4</td>
<td>Added dimensions in Figure 10. Updated marking orientation in Figure 11 and Figure 12.</td>
</tr>
<tr>
<td>13-Jan-2014</td>
<td>5</td>
<td>Updated document title and product references.</td>
</tr>
<tr>
<td>07-Jul-2015</td>
<td>6</td>
<td>Updated Table 1.</td>
</tr>
<tr>
<td>21-Jun-2017</td>
<td>7</td>
<td>Updated Figure 10: &quot;Flip-Chip 5 bumps package outline&quot; and Table 4: &quot;Flip-Chip 5 bumps dimensions&quot;.</td>
</tr>
</tbody>
</table>
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