TDA7590
Digital signal processing IC for speech and audio applications

Features

- 24-bit, fixed point, 120 MIPS DSP core
- Large on-board memory (128KW-24 bit)
- Host access to internal RAM through expansion port
- Access to external RAM (16Mw) through expansion port
- Integrated stereo, 18-bit Sigma-DELTA A/D and 20-bit D/A converters
- Programmable CODEC sample rate up to 48 kHz
- On-board PLL for core clock and converters
- External Flash/SRAM memory bank management
- I²C and SCI serial interface for external control
- 2 enhanced synchronous serial interface (ESSI)
- JTAG interface
- Host interface
- 144-pin TQFP, 0.50 mm pitch
- Automotive temperature range (from -40 °C to +85 °C)

Applications

- Real time digital speech and audio processing:
  - speech recognition
  - speech synthesis
  - speech compression
  - echo canceling
  - noise canceling
  - MP3 decoding

Description

The TDA7590 is a high performances, fully programmable 24-bit, 120 MIPS. Digital signal processor (DSP), designed to support several speech and audio applications, as automatic speech recognition, speech synthesis, MP3 decoding, echo and noise cancellation.

Nevertheless, the embedded CODECs bandwidth and the generic processing engine allow to proceed also full-band audio signals. The large amount of on-chip memory (128 Kwords), together with the 16 Mwords external memory addressable and the 32 general purpose I/O pins permit to build a DSP-system avoiding the usage of an additional microcontroller.

The presence of serial and parallel interfaces allows easy connection with external devices including CODECs, DSPs, microprocessors and personal computers.

In particular, the debug/JTAG interface permits the on-chip emulation of the firmware developed. Further, the presence of the timers and watchdog block makes TDA7590 suitable for PWM processing and allows the integration of a system watchdog.

Table 1. Device summary

<table>
<thead>
<tr>
<th>Order code</th>
<th>Package</th>
<th>Packing</th>
</tr>
</thead>
<tbody>
<tr>
<td>E-TDA7590</td>
<td>TQFP144 (20x20x1.0 exposed pad down)(1)</td>
<td>Tray</td>
</tr>
<tr>
<td>E-TDA7590TR</td>
<td></td>
<td>Tape and reel</td>
</tr>
</tbody>
</table>

1. In ECOPACK® package (see Section 8: Package information on page 22).
## Contents

1. **Block diagram** .............................................. 6

2. **Pin description** ............................................ 7
    2.1 Pin connection ........................................... 7
    2.2 Pin function ............................................. 8
    2.3 Thermal data ............................................ 13

3. **Key parameters** ........................................... 14
    3.1 Power consumption ....................................... 14
        3.1.1 CODEC (ADC/DAC) test description .............. 15

4. **Electrical specification** ................................ 16
    4.1 Absolute maximum ratings .............................. 16
    4.2 Electrical characteristics for I/O pins ............... 16

5. **24 bit DSP core** .......................................... 17

6. **Memories** .................................................. 18

7. **DSP peripherals** .......................................... 19
    7.1 Serial audio interface (SAI) .......................... 19
    7.2 Serial communication interface (SCI) ............... 19
    7.3 I^2C interface ........................................... 19
    7.4 Host interface (HI) ..................................... 19
    7.5 ESSI ..................................................... 20
    7.6 EOC ..................................................... 20
    7.7 Timers and watchdog block ............................ 21
    7.8 PLL ..................................................... 21
    7.9 CODEC cell .............................................. 21

8. **Package information** .................................... 22

9. **Appendix 1** ................................................. 23
9.1 Benchmarking program ........................................... 23

Revision history .......................................................... 41
List of tables

Table 1. Device summary ............................................................... 1
Table 2. Pin function ................................................................. 8
Table 3. Thermal data ................................................................. 13
Table 4. Key parameters ............................................................. 14
Table 5. Absolute maximum ratings .......................................... 16
Table 6. Recommended DC operating conditions ............................. 16
Table 7. General interface electrical characteristics ....................... 16
Table 8. Document revision history .............................................. 41
List of figures

Figure 1. Block diagram ................................................................. 6
Figure 2. Pin connection (top view) ..................................................... 7
Figure 3. TQFP144 mechanical data and package dimensions .................... 22
1  Block diagram

Figure 1.  Block diagram
2 Pin description

2.1 Pin connection

Figure 2. Pin connection (top view)
## 2.2 Pin function

<table>
<thead>
<tr>
<th>N°</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SRD1/TI02 I/O</td>
<td></td>
<td>Serial receive data. Serial input data for receiver. Timer 2 input/output.</td>
</tr>
<tr>
<td>2</td>
<td>STD1 I/O</td>
<td></td>
<td>Serial transmit data. Serial output data from transmitter.</td>
</tr>
<tr>
<td>3</td>
<td>SC02 I/O</td>
<td></td>
<td>Serial control 2. Transmitter frame sync only in asynchronous mode, transmitter and receiver frame sync in synchronous mode.</td>
</tr>
<tr>
<td>4</td>
<td>SC01 I/O</td>
<td></td>
<td>Serial control 1. Receive frame sync in asynchronous mode, output from transmitter 2 or serial flag 1 in synchronous mode.</td>
</tr>
<tr>
<td>5</td>
<td>DE_N I/O</td>
<td></td>
<td>Test data output (input/output). Debug request input and acknowledge output.</td>
</tr>
<tr>
<td>6</td>
<td>NMI_N I</td>
<td></td>
<td>Non-maskable interrupt/ PINIT. Used to enable the PLL during RESET and as a non-maskable interrupt at all other times.</td>
</tr>
<tr>
<td>7</td>
<td>SRD0 I/O</td>
<td></td>
<td>Serial receive data. Serial input data for receiver.</td>
</tr>
<tr>
<td>8</td>
<td>IOVDD I</td>
<td></td>
<td>IO power supply.</td>
</tr>
<tr>
<td>9</td>
<td>IOVSS I</td>
<td></td>
<td>IO ground.</td>
</tr>
<tr>
<td>10</td>
<td>STD0 I/O</td>
<td></td>
<td>Serial Transmit Data. Serial output data from transmitter.</td>
</tr>
<tr>
<td>11</td>
<td>SC10/SCL I/O</td>
<td></td>
<td>ESSI serial control 0. Receive clock in asynchronous mode, output from transmitter or serial flag in synchronous mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(^2\text{C SCL serial clock line.} )</td>
</tr>
<tr>
<td>12</td>
<td>SC00 I/O</td>
<td></td>
<td>Serial control 0. Receive clock in asynchronous mode, output from transmitter 1 or serial flag 0 in synchronous mode.</td>
</tr>
<tr>
<td>13</td>
<td>RXD I/O</td>
<td></td>
<td>SCI receive data. Receives byte-oriented serial data.</td>
</tr>
<tr>
<td>14</td>
<td>TXD I/O</td>
<td></td>
<td>SCI read enable. Transmits serial data from SCI transmit shift register.</td>
</tr>
<tr>
<td>15</td>
<td>SCLK I/O</td>
<td></td>
<td>SCI serial clock. Input or output clock from which data is transferred in synchronous mode and from which the transmit and/or receive baud rate is derived in asynchronous mode.</td>
</tr>
<tr>
<td>16</td>
<td>SCK1/TI01 I/O</td>
<td></td>
<td>Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Timer 1 input/output.</td>
</tr>
<tr>
<td>17</td>
<td>SCK0 I/O</td>
<td></td>
<td>Serial clock. Serial bit clock for transmitter only in asynchronous mode, serial bit clock for both receiver and transmitter in synchronous mode.</td>
</tr>
<tr>
<td>18</td>
<td>RESETN I</td>
<td></td>
<td>System reset. A low level applied to RESET_N input initializes the IC.</td>
</tr>
<tr>
<td>19</td>
<td>SCANEN I</td>
<td></td>
<td>SCAN enable. When active with TESTEN also active, controls the shifting of the internal scan chains.</td>
</tr>
<tr>
<td>20</td>
<td>TESTEN I</td>
<td></td>
<td>Test enable. When active, puts the chip into test mode and muxes the XTI clock to all flip-flops. When SCANEN is also active, the scan chain shifting is enabled.</td>
</tr>
<tr>
<td>21</td>
<td>COREVSS I</td>
<td></td>
<td>Core ground.</td>
</tr>
<tr>
<td>22</td>
<td>COREVDD I</td>
<td></td>
<td>Core power supply.</td>
</tr>
<tr>
<td>23</td>
<td>TIO0 I/O</td>
<td></td>
<td>Timer 0 input/output.</td>
</tr>
<tr>
<td>24</td>
<td>VSSSUB I</td>
<td></td>
<td>Analog substrate isolation.</td>
</tr>
<tr>
<td>N°</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----</td>
<td>----------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>25</td>
<td>DAC1</td>
<td>O</td>
<td>DAC1 left single analog output.</td>
</tr>
<tr>
<td>26</td>
<td>DAC0M</td>
<td>O</td>
<td>DAC0 negative right differential analog output.</td>
</tr>
<tr>
<td>27</td>
<td>DAC0P</td>
<td>O</td>
<td>DAC0 positive right differential analog output.</td>
</tr>
<tr>
<td>28</td>
<td>CODEC_VSS</td>
<td>I</td>
<td>Voltage ground.</td>
</tr>
<tr>
<td>29</td>
<td>REF0</td>
<td>I</td>
<td>Codec power supply.</td>
</tr>
<tr>
<td>30</td>
<td>CODEC_VDD</td>
<td>I</td>
<td>Codec reference.</td>
</tr>
<tr>
<td>31</td>
<td>ADC1</td>
<td>I</td>
<td>ADC1 left single analog input.</td>
</tr>
<tr>
<td>32</td>
<td>ADC0M</td>
<td>I</td>
<td>DAC0 negative right differential analog inputs.</td>
</tr>
<tr>
<td>33</td>
<td>ADC0P</td>
<td>I</td>
<td>DAC0 positive right differential analog inputs.</td>
</tr>
<tr>
<td>36</td>
<td>EXTDACLK</td>
<td>I</td>
<td>External DAC clock. Optional external clock source from which LRCLK and SCLK can be generated.</td>
</tr>
<tr>
<td>37</td>
<td>XTI</td>
<td>I</td>
<td>Crystal oscillator input. External clock input or crystal connection.</td>
</tr>
<tr>
<td>38</td>
<td>XTO</td>
<td>O</td>
<td>Crystal oscillator output. Crystal oscillator output drive.</td>
</tr>
<tr>
<td>39</td>
<td>PLL_VDD</td>
<td>I</td>
<td>PLL power supply.</td>
</tr>
<tr>
<td>40</td>
<td>PLL_VSS</td>
<td>I</td>
<td>PLL ground input.</td>
</tr>
<tr>
<td>41</td>
<td>HDS</td>
<td>I/O</td>
<td>Host data strobe. Polarity programmable Host data strobe input for single strobe mode. Polarity programmable Host write strobe input for double strobe mode.</td>
</tr>
<tr>
<td>42</td>
<td>HRW</td>
<td>I/O</td>
<td>Host read/write. Host read/write for single strobe bus mode. Polarity programmable Host read data strobe for double strobe mode.</td>
</tr>
<tr>
<td>43</td>
<td>HACK</td>
<td>I/O</td>
<td>Host acknowledge. Polarity programmable host interrupt acknowledge for single host request mode. Polarity programmable host receive request interrupt for double host request mode.</td>
</tr>
<tr>
<td>44</td>
<td>HREQ</td>
<td>I/O</td>
<td>Host request. Polarity programmable host request interrupt for single host request mode. Polarity programmable host transfer request interrupt for double host request mode.</td>
</tr>
<tr>
<td>45</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>46</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>47</td>
<td>HCS</td>
<td>I/O</td>
<td>Host chip select. Polarity programmable host chip select for non-multiplexed mode. Host address Line 10 for multiplexed mode.</td>
</tr>
<tr>
<td>48</td>
<td>HA9</td>
<td>I/O</td>
<td>Host address 9. Address line 9 in multiplexed mode otherwise address line 2 in non-multiplexed mode.</td>
</tr>
<tr>
<td>49</td>
<td>HA8</td>
<td>I/O</td>
<td>Host address 8. Address line 8 in multiplexed mode otherwise address line 1 in non-multiplexed mode.</td>
</tr>
<tr>
<td>50</td>
<td>HAS</td>
<td>I/O</td>
<td>Host address strobe. Address strobe for multiplexed bus or Address 0 for non multiplexed.</td>
</tr>
<tr>
<td>51</td>
<td>HAD[7]</td>
<td>I/O</td>
<td>Host 8-bit data line 7. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>N°</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>--------</td>
<td>------</td>
<td>-------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>52</td>
<td>HAD[6]</td>
<td>I/O</td>
<td>Host 8-bit data line 6. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>53</td>
<td>HAD[5]</td>
<td>I/O</td>
<td>Host 8-bit data line 5. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>54</td>
<td>HAD[4]</td>
<td>I/O</td>
<td>Host 8-bit data line 4. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>55</td>
<td>COREVDD</td>
<td>I</td>
<td>Core power supply.</td>
</tr>
<tr>
<td>56</td>
<td>COREVSS</td>
<td>I</td>
<td>Core ground.</td>
</tr>
<tr>
<td>57</td>
<td>HAD[3]</td>
<td>I/O</td>
<td>Host 8-bit data line 3. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>58</td>
<td>HAD[2]</td>
<td>I/O</td>
<td>Host 8-bit data line 2. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>59</td>
<td>HAD[1]</td>
<td>I/O</td>
<td>Host 8-bit data line 1. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>60</td>
<td>HAD[0]</td>
<td>I/O</td>
<td>Host 8-bit data line 0. Host data bus and/or address lines when in multiplexed mode.</td>
</tr>
<tr>
<td>63</td>
<td>BR_N</td>
<td>O</td>
<td>Bus request. Asserted when port A requires bus mastership to perform off-chip accesses.</td>
</tr>
<tr>
<td>64</td>
<td>BB_N</td>
<td>I/O</td>
<td>Bus busy. Asserted by port A when bus_busy_in_n is negated and BG_N is asserted.</td>
</tr>
<tr>
<td>65</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>66</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>67</td>
<td>WEN_N</td>
<td>O</td>
<td>Write enable.</td>
</tr>
<tr>
<td>68</td>
<td>OEN_N</td>
<td>O</td>
<td>Output enable.</td>
</tr>
<tr>
<td>70</td>
<td>AA[0]</td>
<td>O</td>
<td>Address attributes line 0. Port A address attributes/chip select pins with programmable polarity.</td>
</tr>
<tr>
<td>71</td>
<td>BG_N</td>
<td>I</td>
<td>Bus grant. When asserted, Port A becomes the bus master elect. Bus mastership is attained when bus busy is negated by the current bus master.</td>
</tr>
<tr>
<td>72</td>
<td>AB[0]</td>
<td>O</td>
<td>Address bus line 0. Port A external address bus.</td>
</tr>
<tr>
<td>74</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>75</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>N°</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----</td>
<td>--------</td>
<td>------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>80</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>81</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>86</td>
<td>COREVDD</td>
<td>I</td>
<td>Core power supply.</td>
</tr>
<tr>
<td>87</td>
<td>COREVSS</td>
<td>I</td>
<td>Core ground.</td>
</tr>
<tr>
<td>90</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>91</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>97</td>
<td>AB[17]</td>
<td>O</td>
<td>Address bus line 17. Port A external address bus.</td>
</tr>
<tr>
<td>100</td>
<td>DB[0]</td>
<td>I/O</td>
<td>Address bus 0. Port A external data bus.</td>
</tr>
<tr>
<td>103</td>
<td>COREVDD</td>
<td>I</td>
<td>Core power supply.</td>
</tr>
<tr>
<td>104</td>
<td>COREVSS</td>
<td>I</td>
<td>Core ground.</td>
</tr>
<tr>
<td>111</td>
<td>IOVDD</td>
<td>I</td>
<td>IO Power Supply.</td>
</tr>
<tr>
<td>N°</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>--------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>112</td>
<td>IOVSS</td>
<td>I</td>
<td>IO Ground.</td>
</tr>
<tr>
<td>119</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>120</td>
<td>IOVSS</td>
<td>I</td>
<td>IO Ground.</td>
</tr>
<tr>
<td>123</td>
<td>DB[17]</td>
<td>I/O</td>
<td>Data Bus line 17. Port A external data bus.</td>
</tr>
<tr>
<td>124</td>
<td>DB[18]</td>
<td>I/O</td>
<td>Data Bus line 18. Port A external data bus.</td>
</tr>
<tr>
<td>126</td>
<td>COREVDD</td>
<td>I</td>
<td>Core power supply.</td>
</tr>
<tr>
<td>127</td>
<td>COREVSS</td>
<td>I</td>
<td>Core ground.</td>
</tr>
<tr>
<td>129</td>
<td>IOVDD</td>
<td>I</td>
<td>IO power supply.</td>
</tr>
<tr>
<td>130</td>
<td>IOVSS</td>
<td>I</td>
<td>IO ground.</td>
</tr>
<tr>
<td>132</td>
<td>DB[22]</td>
<td>I/O</td>
<td>Data Bus line 22. Port A external data bus.</td>
</tr>
<tr>
<td>133</td>
<td>DB[23]</td>
<td>I/O</td>
<td>Data Bus line 23. Port A external data bus.</td>
</tr>
<tr>
<td>134</td>
<td>IRQA</td>
<td>I</td>
<td>Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.</td>
</tr>
<tr>
<td>135</td>
<td>IRQB</td>
<td>I</td>
<td>Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.</td>
</tr>
<tr>
<td>136</td>
<td>IRQC</td>
<td>I</td>
<td>Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.</td>
</tr>
<tr>
<td>137</td>
<td>IRQD</td>
<td>I</td>
<td>Interrupt request line/ Mode control. Used as mode control during RESET and as interrupt request line at all other times.</td>
</tr>
<tr>
<td>138</td>
<td>TRSTN</td>
<td>I</td>
<td>Test reset. JTAG output pin for serial data out from debug interface.</td>
</tr>
<tr>
<td>139</td>
<td>TDI</td>
<td>I</td>
<td>Test data input. JTAG input pin for serial data input for debug interface.</td>
</tr>
<tr>
<td>140</td>
<td>TCK</td>
<td>I</td>
<td>Test clock. JTAG input pin for clocking debug interface.</td>
</tr>
<tr>
<td>141</td>
<td>TMS</td>
<td>I</td>
<td>Test mode select. JTAG input pin for control of TAP Controller of debug interface.</td>
</tr>
<tr>
<td>142</td>
<td>TDO</td>
<td>O</td>
<td>Test data output. JTAG output pin for serial data out from debug interface.</td>
</tr>
</tbody>
</table>
Table 2. Pin function  (continued)

<table>
<thead>
<tr>
<th>N°</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>143</td>
<td>SC12</td>
<td>I/O</td>
<td>Serial control 2. Transmitter frame sync only in asynchronous mode,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>transmitter and receiver frame sync in synchronous mode.</td>
</tr>
<tr>
<td>144</td>
<td>SC11/SDA</td>
<td>I/O</td>
<td>Serial control 1. Receive frame sync in asynchronous mode, output from</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>transmitter 2 or serial flag 1 in synchronous mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I²C SDA. Serial data line.</td>
</tr>
</tbody>
</table>

2.3 Thermal data

Table 3. Thermal data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th-j-pins}$</td>
<td>Thermal resistance junction to pins</td>
<td>32</td>
<td>°C/W</td>
</tr>
</tbody>
</table>
3 Key parameters

3.1 Power consumption

Power consumption depends on application running and DSP clock frequency. Supply current values are measured and guaranteed at testing level by adopting the benchmarking program reported in Appendix 1.

Table 4. Key parameters

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>General</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fosc</td>
<td>Crystal frequency</td>
<td></td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>CORE_VDD</td>
<td>Operating voltage</td>
<td>1.62</td>
<td>1.8</td>
<td>1.98</td>
<td>V</td>
</tr>
<tr>
<td>CODEC_VDD</td>
<td>Operating voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>IOVDD</td>
<td>Operating voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>PLL_VDD</td>
<td>Operating voltage</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>IDD_1.8V</td>
<td>Supply current</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>IDD_3.3V</td>
<td>Supply current</td>
<td></td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Tamb</td>
<td>Operating temperature</td>
<td>-40</td>
<td></td>
<td>85</td>
<td>°C</td>
</tr>
<tr>
<td>DSP core</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fdsp</td>
<td>DSP clock frequency</td>
<td></td>
<td></td>
<td>120</td>
<td>MHz</td>
</tr>
<tr>
<td>ADC single ended</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vpp</td>
<td>Maximum input range at ADC1</td>
<td></td>
<td></td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>THD/S</td>
<td>Total harmonics distortion to signal</td>
<td>-71</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(THD+N)/S</td>
<td>(THD + Noise) to signal</td>
<td>-70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
<td></td>
<td></td>
<td>75</td>
<td>dB</td>
</tr>
<tr>
<td>ICL</td>
<td>Interchannel isolation</td>
<td>-100</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>ADC differential</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vpp</td>
<td>Maximum input range at ADC0M-ADC0P</td>
<td></td>
<td></td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td>THD/S</td>
<td>Total harmonics distortion to signal</td>
<td>-65</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(THD+N)/S</td>
<td>(THD + Noise) to signal</td>
<td>-65</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
<td></td>
<td></td>
<td>84</td>
<td>dB</td>
</tr>
<tr>
<td>ICL</td>
<td>Interchannel isolation</td>
<td>-100</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>DAC single ended</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vpp</td>
<td>Maximum input range at ADC1</td>
<td></td>
<td></td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>THD/S</td>
<td>Total harmonics distortion to signal</td>
<td>-64</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(THD+N)</td>
<td>(THD + Noise) to signal</td>
<td>-60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>
3.1.1 CODEC (ADC/DAC) test description

Reported typical values (table 3. - ADC and DAC sections) have been measured at Lab level during product evaluation phase. General definitions and procedures are separately defined in following dedicated paragraphs.

**Total harmonic distortion with noise to signal (THD+N)/S**

THD+N is defined as the ratio of the total power of the second power and higher harmonic with noise components to the power of the fundamental for that signal. For THD+N measurement, choose the DSP analyzer in digital analyzer with THD ratio as measurement option. Measure the THD+N value at -3 dB amplitude of the input signal. First measure the THD+N value at 1Vrms which is 0 dB reference and then measure the value at -3 dB reference.

**Dynamic range (DR)**

DR is defined as the level of THD+N measured when the input sine wave amplitude is so small that no harmonics apart from the fundamental tone are present in the output signal. This way THD+N becomes practically the ratio between the whole signal and noise floor, being a different way to express SNR. As a convention, at which no harmonics should be present in the output signal, it is fixed at -40dB of the full scale amplitude.

**Crosstalk or interchannel isolation**

A disturbance, caused by electromagnetic interference, along a circuit or a cable pair. An electric signal disrupts another signal in an adjacent circuit and can cause it to become confused and cross over each other. Crosstalk is measured by applying a signal -3dB amplitude of input signal at one channel (A) and no signal at an other channel (B), measuring the effect on this channel (B) because of the channel (A).

**Total harmonic distortion to signal (THD)/S**

THD is defined as the ratio of the sum of only those components of the output signal which are harmonic of system input, after having removed the fundamental tone corresponding to the pure sine wave as input and the input signal. This measurement is done by using the Harmonic analyzer which can isolate up to 15th harmonic components on the acquired signal and report the sum of all of them, centering the fundamental tone on the frequency provided by the input signal generator. These measurements are performed at -3dB reference amplitude of input signal.

### Table 4. Key parameters (continued)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DR</td>
<td>Dynamic range</td>
<td>89</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>ICL</td>
<td>Interchannel isolation</td>
<td>-100</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Vpp</td>
<td>Maximum input range at ADC1</td>
<td></td>
<td>2.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>THD/S</td>
<td>Total harmonics distortion to signal</td>
<td>-58</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>(THD+N)/S</td>
<td>(THD + Noise) to signal</td>
<td>-57</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
<td>90</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>ICL</td>
<td>Interchannel Isolation</td>
<td>-85</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>
4 Electrical specification

4.1 Absolute maximum ratings

Table 5. Absolute maximum ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL_VDD</td>
<td>3.3V PLL power supply voltage</td>
<td>-0.5 to 4</td>
<td>V</td>
</tr>
<tr>
<td>CODEC_VDD</td>
<td>3.3V CODEC analog power supply</td>
<td>-0.5 to 4</td>
<td>V</td>
</tr>
<tr>
<td>IOVDD</td>
<td>3.3V IO power supply</td>
<td>-0.5 to 4</td>
<td>V</td>
</tr>
<tr>
<td>CORE_VDD</td>
<td>1.8V CORE power supply</td>
<td>-0.5 to 2.2</td>
<td>V</td>
</tr>
<tr>
<td>IO_MAX</td>
<td>Input or output voltage</td>
<td>-0.5 to (IOVDD +0.5)</td>
<td>V</td>
</tr>
</tbody>
</table>

4.2 Electrical characteristics for I/O pins

Table 6. Recommended DC operating conditions

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOVDD</td>
<td>IO power supply voltage</td>
<td>3 to 3.6(1)</td>
<td>V</td>
</tr>
<tr>
<td>Tj</td>
<td>Operating junction temperature</td>
<td>-40 to 105</td>
<td>°C</td>
</tr>
</tbody>
</table>

1. All the specification are valid only within these recommended operating conditions.

Table 7. General interface electrical characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>lll</td>
<td>Low level input current without pull-up device</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lih</td>
<td>High level input current without pull-down device</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>loz</td>
<td>Tri-state output leakage without pull up/down device</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>lozFT</td>
<td>Five Volt tolerant tri-state output leakage without pull up/down device</td>
<td></td>
<td>1</td>
<td>μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>l latch-up</td>
<td>I/O latch-up current</td>
<td>V &lt; 0V, V &lt; Vdd</td>
<td>200</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vesd</td>
<td>Electrostatic protection (HBM)</td>
<td>leakage &lt; 1mA</td>
<td>2000</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vil</td>
<td>Low level input voltage(1)</td>
<td></td>
<td>0.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vih</td>
<td>High level input voltage(1)</td>
<td></td>
<td>2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vhyst</td>
<td>Schmitt trigger hysteresis(1)</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vol</td>
<td>Low level output voltage (1)(2)(3)</td>
<td>Iol = XmA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voh</td>
<td>High level output voltage (1)(2)(3)</td>
<td>Ioh = -XmA</td>
<td>IOVDD - 0.15</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1. TTL specifications only apply to the supply voltage range Vdd = 3.15V to 3.6V.
2. Takes into account 200mV voltage drop in both supply lines.
3. X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.
5 24 bit DSP core

The DSP core is a general purpose 24-bit DSP. The main feature of the DSP core are listed below:

• 120 MHz operating frequency (120 MIPS)
• Fully pipelined 24 x 24 bit parallel multiplier-accumulator
• Saturation/limiting logic
• 56-bit parallel barrel shifter
• Linear, reverse carry and modulo addressing modes
• 24-bit address buses for program, X and Y data spaces and DMA
• Memory-expandible hardware stack
• Nested zero-overhead DO loops
• Fast interrupts
• Powerful JTAG emulation port
• Software wait and stop low power standby modes
• Program address tracing support
• Two 24-bit data moves in parallel with arithmetic operations
• External interrupts including non-maskable interrupt
• Interrupts may be independently masked and prioritized
• Bit-manipulation instructions can access any register or memory location
• On board support for DMA controller
6 Memories

128 K x 24-bit RAM divided into 4 areas, program RAM (PRAM), X data RAM (XRAM), Y data RAM (YRAM) and flexible allocation RAM (FLEX) as follows:

- 16 kB PRAM
- 40 kB FLEX RAM. FLEX RAM is accessed through the expansion port by the DSP core.
- External access to the FLEX RAM is also supported.
- 72 kB RAM is allocated as XRAM and YRAM. Four configurations are supported:
  - 4 kB XRAM and 68 kB YRAM
  - 8 kB XRAM and 64 kB YRAM
  - 16 kB XRAM and 56 kB YRAM
  - 24 kB XRAM and 48 kB YRAM
7 DSP peripherals

7.1 Serial audio interface (SAI)

The SAI is used to communicate between the CODEC and the DSPs.

In addition, digital audio can be directly input for processing. There is only one SAI found on the chip that can be accessed by either the DSP or the DMA controller. The main features of this block are listed below:
- Slave operating modes, all clock lines can be inputs or outputs
- Transmit and receive interrupt logic triggers on left/right data pairs
- Receive and transmit data registers have two locations to hold left and right data

7.2 Serial communication interface (SCI)

The serial communication interface provides a full duplex port for serial communication to other DSPs, microprocessors, and peripherals like modems.

The interface supports the following features:
- No additional logic for connection to other TTL level peripherals
- Asynchronous bit rates and protocols "High speed" synchronous data transmission.
- Asynchronous protocol includes Multidrop mode for master/slave operation with wake-up on Idle line and wake-up on address bit capability, permitting the SCI to share a single line with multiple peripherals
- Transmit and receive logic can operate asynchronously from each other.
- A programmable baud-rate generator which provide the transmit and receive clocks or functions as a general purpose timer.

7.3 I²C interface

The inter integrated-circuit bus is a simple bi-directional two-wire bus used for efficient inter IC control. All I²C bus compatible devices incorporate an on-chip interface which allows them to communicate directly with each other via the I²C bus.

Every component connected to the I²C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on its functionality.

7.4 Host interface (HI)

The host interface is a system-on-chip module that permits connection to the data bus of a host processor. The HI is capable of driving 16 programmable external pins which can be configured as an 8 bit parallel port for direct connection to a host processor.
The key features of the host interface are:
- 8 bit parallel port "Full-duplex" dedicated host register bank
- Dedicated Mozart™ core DSP register core bank.
- Register banks map directly into Mozart X memory space
- 3 transfer modes:
  - host command
  - Host to Mozart core DSP
  - Mozart core DSP to host
- Access protocols:
  - Software polled
  - Interrupt
  - DMA access by the Mozart core DSP core
- 2+ wait states clock cycles per transfer
- Supported instructions:
  - Data transfer between Mozart core and external host using Mozart MOVE instruction
  - Simple I/O service routine with bit addressing instructions
  - IO service using fast interrupts with MOVEP instructions.

7.5 ESSI

The ESSI peripheral enables serial-port communication between the DSP core and external devices including Codecs, DSP, microprocessors. The ESSI is capable of driving 12 programmable external pins which can be configured as GPIO ports C and D or ESSI pins.

The key features of the ESSI are:
- Independent receiver and transmitter
- Synchronous or asynchronous channel modes synchronous. Receiver and transmitter use same clock/sync asynchronous. Receiver and transmitter may use separate clock/sync up to one transmitter enabled in asynchronous channel mode.
- Up to three transmitters enabled in synchronous channel mode.
- Normal mode. One word per period.
- Network mode. Up to 32 words per period.

7.6 EOC

The Salieri extended on-chip memory interface provides access to 40 kB of on-chip memory. The Mozart core will treat this memory as if it were external. Access by off-chip expansion bus masters is permitted. All accesses to the extended on-chip RAM are controlled by the extended on-chip memory control register. This register determines which combinations of the Address attribute pins should be interpreted as accesses to the 40 kB of RAM.
7.7 **Timers and watchdog block**

The timers and watchdog block consists of a common 21-bit prescaler and three independent and identical general-purpose 24-bit timer/event counters, each with its own register set.

Each timer has the following capabilities:
- Uses internal or external clocking.
- Interrupts the Mozart after a specified number of events (clocks).
- Signals an external device after counting internal events.
- Triggers DMA transfers after a specified number of events (clocks) occurs.
- Connects to the external world through designated pins TIO[0-2] for timers 0-2.

When TIO is configured as an
- Input: timer functions as an external event counter. Timer measures external pulse width/signal period.
- Output: timer functions as a:
  - Timer
  - Watchdog timer
  - Pulse-width modulator.

7.8 **PLL**

The PLL generates the following clocks:
- DCLK: DSP core clock
- DACLK: ADC and DAC clock
- LRCLK: left/right clock for the SAI and the CODEC
- SCLK: shift serial clock for the SAI and the CODEC

7.9 **CODEC cell**

The main features of the CODEC cell are listed below:
- 20 bits stereo DAC, and 18 bits ADC
- I²S format
- Oversampling ratio: 512
- Sampling rates of 8 kHz to 48 kHz

The analog interface is in the form of differential signals for each channel. The interface on the digital side has the form of an SAI interface and can interface directly to an SAI channel and then to the DSP core.

DCLK can be supplied either by the internal PLL or by external, to allow synchronization with external analog digital sources.
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

Figure 3. TQFP144 mechanical data and package dimensions

<table>
<thead>
<tr>
<th>DIM.</th>
<th>mm</th>
<th>inch</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MIN</td>
<td>TYP</td>
<td>MAX</td>
</tr>
<tr>
<td>A</td>
<td>1.20</td>
<td>0.047</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>0.05</td>
<td>0.15</td>
<td>0.002</td>
</tr>
<tr>
<td>A2</td>
<td>0.95</td>
<td>1.05</td>
<td>0.907</td>
</tr>
<tr>
<td>B</td>
<td>0.17</td>
<td>0.22</td>
<td>0.27</td>
</tr>
<tr>
<td>C</td>
<td>0.09</td>
<td>0.20</td>
<td>0.003</td>
</tr>
<tr>
<td>D</td>
<td>21.80</td>
<td>22.00</td>
<td>22.20</td>
</tr>
<tr>
<td>D1</td>
<td>19.80</td>
<td>20.00</td>
<td>20.20</td>
</tr>
<tr>
<td>D2</td>
<td>2.00</td>
<td></td>
<td>0.079</td>
</tr>
<tr>
<td>D3</td>
<td></td>
<td></td>
<td>0.689</td>
</tr>
<tr>
<td>E</td>
<td>21.80</td>
<td>22.00</td>
<td>22.20</td>
</tr>
<tr>
<td>E1</td>
<td>19.80</td>
<td>20.00</td>
<td>20.20</td>
</tr>
<tr>
<td>E2</td>
<td>2.00</td>
<td></td>
<td>0.079</td>
</tr>
<tr>
<td>E3</td>
<td>17.50</td>
<td></td>
<td>0.689</td>
</tr>
<tr>
<td>e</td>
<td>0.50</td>
<td></td>
<td>0.020</td>
</tr>
<tr>
<td>L</td>
<td>0.45</td>
<td>0.60</td>
<td>0.75</td>
</tr>
<tr>
<td>L1</td>
<td>1.00</td>
<td></td>
<td>0.035</td>
</tr>
<tr>
<td>K</td>
<td>0° (min.), 3.5° (typ.), 7° (max.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>cc</td>
<td>0.08</td>
<td></td>
<td>0.03</td>
</tr>
</tbody>
</table>

Note 1: Exact shape of each corner is optional.
Appendix 1

9 Benchmarking program

9.1 Benchmarking program

;*******************************************************************************
;*********************************** Equates ***********************************
;*******************************************************************************

Npts     equ 20
Ntaps    equ 4

;*******************************************************************************
;*******************************************************************************

M_HDR EQU $FFFFC9 ; PS- Host port GPIO data Register
M_HDRR EQU $FFFFC8 ; PS- Host port GPIO direction Register
M_PCRC  EQU $FFFFBF ; Port C Control Register
M_PRCR  EQU $FFFFBE ; Port C Direction Register
M_PDRC  EQU $FFFFBD ; Port C GPIO Data Register
M_PCDR  EQU $FFFFAF ; Port D Control register
M_PDDR  EQU $FFFFAE ; Port D Direction Data Register
M_PDCR  EQU $FFFFAD ; Port D GPIO Data Register
M_PCRD  EQU $FFFFAF ; Port E Control register
M_PPERD EQU $FFFFAE ; Port E Direction Register
M_PPOR  EQU $FFFFAE ; Port E Data Register
M_OGDB  EQU $FFFFFC ; OnCE GDB Register

;*******************************************************************************
;*******************************************************************************

IPR_C EQU $FFFFFF ; Interrupt Priority Register Core
Appendix 1

IPR_P EQU $FFFFFE ; Interrupt Priority Register Peripheral

; SAI interrupt Vectors
SAI_ROF EQU $070 ; Receiver Overflow
SAI_TUF EQU $072 ; Transmitter Underflow
SAI_RDR EQU $074 ; Receiver Data Ready
SAI_TDE EQU $076 ; Transmitter Data Empty

; Timer interrupt Vector
Timer0_tcf equ $24 ; Timer0 Compare
Timer0_tof equ $26 ; Timer0 Overflow
Timer1_tcf equ $28 ; Timer1 Compare
Timer1_tof equ $2A ; Timer1 Overflow
Timer2_tcf equ $2C ; Timer2 Compare
Timer2_tof equ $2E ; Timer2 Overflow

; SCI Interrupt Vectors
SCI_REC EQU $000050 ; SCI receive data
SCI_REC_E EQU $000052 ; SCI receive data with exception status
SCI_TRANS EQU $000054 ; SCI transmit data
SCI_IDLE EQU $000056 ; SCI idle line
SCI_TIMER EQU $000058 ; SCI timer

;; Bit Definition for SCI_SSR
FRAMING EQU 6
RESET EQU $000000 ; Reset address location

; ------------------------------------------------------------------------
; EQUATES for SAI (y memory)
; ------------------------------------------------------------------------
SAI_RCS EQU $FFFFFF ; SAI Receive Control/Status Register
SAI_RX2 EQU $FFFFFE ; SAI Channel 2 Receiver Data
SAI_RX1 EQU $FFFFFD ; SAI Channel 1 Receiver Data
SAI_RX0 EQU $FFFFFC ; SAI Channel 0 Receiver Data
SAI_TCS EQU $FFFFFB ; SAI Transmit Control/Status Register
SAI_TX2 EQU $FFFFFA ; SAI Channel 2 Transmitter Data
SAI_TX1 EQU $FFFFF9 ; SAI Channel 1 Transmitter Data
SAI_TX0 EQU $FFFFF8 ; SAI Channel 0 Transmitter Data

;; Bit Definitions for M_RCS
ROFCL EQU 16 ; Receiver Data Overflow Clear
RDR EQU 15 ; Receiver Data Ready
ROFL EQU 14 ; Receiver Data Overflow
RXIE EQU 12 ; Receiver Interrupt Enable
RXJ EQU 11 ; Receiver Data Word Justification
RXEL EQU 10 ; Receiver Relative Timing
RCEP EQU 9 ; Receiver Clock Polarity
RLBS EQU 8 ; Receiver Left Right Selection
RDRI EQU 7 ; Receiver Data Shift Direction
RMLL EQU 6 ; Receiver Word Length Control 1
RMLO EQU 5 ; Receiver Word Length Control 0
RMME EQU 3 ; Receiver Master Mode Enable
R2EN EQU 2 ; Receiver 2 enable
R1EN EQU 1 ; Receiver 1 enable
R0EN EQU 0 ; Receiver 0 enable
Bit Definitions for M_TCS

TUFCL EQU 16 ; Transmitter Data Overflow Clear
TDE EQU 15 ; Transmitter Data Ready
TUFL EQU 14 ; Transmitter Data Overflow
; Reserved
TXIE EQU 12 ; Transmitter Interrupt Enable
TDWE EQU 11 ; Transmitter Data Word Justification
TREL EQU 10 ; Transmitter Relative Timing
TCKP EQU 9 ; Transmitter Clock Polarity
TLRS EQU 8 ; Transmitter Left Right Selection
TDIR EQU 7 ; Transmitter Data Shift Direction
TMLC EQU 6 ; Transmitter Word Length Control 1
TMLO EQU 5 ; Transmitter Word Length Control 0
; Reserved
TMME EQU 3 ; Transmitter Master Mode Enable
T2EN EQU 2 ; Transmitter 2 enable
T1EN EQU 1 ; Transmitter 1 enable
T0EN EQU 0 ; Transmitter 0 enable

Bit Definitions for CODEC

GADCL_0 EQU 0 ; ADC Left  Gain Bit 0
GADCL_1 EQU 1 ; ADC Left  Gain Bit 1
GADCL_2 EQU 2 ; ADC Left  Gain Bit 2
GADCR_0 EQU 3 ; ADC Right Gain Bit 0
GADCR_1 EQU 4 ; ADC Right Gain Bit 1
GADCR_2 EQU 5 ; ADC Right Gain Bit 2
GDACL_0 EQU 6 ; DAC Left  Gain Bit 0
GDACL_1 EQU 7 ; DAC Left  Gain Bit 1
GDACL_2 EQU 8 ; DAC Left  Gain Bit 2
GDACR_0 EQU 9 ; DAC Right Gain Bit 0
GDACR_1 EQU 10; DAC Right Gain Bit 1
GDACR_2 EQU 11; DAC Right Gain Bit 2
MUTEDAC EQU 12; Mute DAC - Active Hi, Reset Val = 1
PDNDAC EQU 13; Power down DAC - Active Hi, Reset Val = 0
PDNADC EQU 14; Power down ADC - Active Hi, Reset Val = 0
N_RST EQU 15; Asynchronous Reset - Active Lo, Reset Val = 1

Bit Definitions for PLL

IDP0 EQU 0 ; Input Divide Factor 0
IDP1 EQU 1 ; Input Divide Factor 1
IDP2 EQU 2 ; Input Divide Factor 2
IDP3 EQU 3 ; Input Divide Factor 3
IDP4 EQU 4 ; Input Divide Factor 4
; Reserved
LOCK EQU 6 ; PLL Lock Indication bit
OUTLOCK EQU 7 ; PLL Lost Lock bit
MF0 EQU 8 ; Multiplication bit 0
MF1 EQU 9 ; Multiplication bit 1
MF2 EQU 10 ; Multiplication bit 2
MF3 EQU 11 ; Multiplication bit 3
MF4 EQU 12 ; Multiplication bit 4
MF5 EQU 13 ; Multiplication bit 5
MF6 EQU 14 ; Multiplication bit 6
PLLIE EQU 15 ; PLL interrupt enable
PWRDN EQU 16 ; PLL power down
DITEN EQU 17 ; Dither Enable
FRACEN EQU 18 ; PLL Fractional-N function enable
PEN EQU 19 ; PLL Enable

;;; Bit Definitions for PLL_CLK_CNTL
DSPDF0 EQU 0 ; DSP clock divider factor 0
DSPDF1 EQU 1 ; DSP clock divider factor 1
DSPDF2 EQU 2 ; DSP clock divider factor 2
DSPDF3 EQU 3 ; DSP clock divider factor 3
; Reserved
DCKSRC EQU 6 ; DSP clock source 0->XTI/(DSPDF3:0 + 1)
; 1->VCO/(DSPDF3:0 + 1)
DACLEN EQU 7 ; Enable bit for oversampling clock
MFSDF0 EQU 8 ; Oversampling multiple bit 0
MFSDF1 EQU 9 ; Oversampling multiple bit 1
MFSDF2 EQU 10 ; Oversampling multiple bit 2
MFSDF3 EQU 11 ; Oversampling multiple bit 3
MFSDF4 EQU 12 ; Oversampling multiple bit 4
MFSDF5 EQU 13 ; Oversampling multiple bit 5
MFSDF6 EQU 14 ; Oversampling multiple bit 6
SEL0 EQU 15 ; Sampling multiple select bit 0
SEL1 EQU 16 ; Sampling multiple select bit 1
SEL2 EQU 17 ; Sampling multiple select bit 2
DSP_XTI EQU 18 ; DSP_XTI =0 -> Use VCO/DSPDF for DCLK
; DSP_XTI =1 -> Use XTI for DCLK
DAC_SEL EQU 19 ; Selects between VCO and ext_dac_clk
XTLD EQU 20 ; Disables the external crystal when set

;------------------------------------------------------------------------
; EQUATES for I/O Port Programming
;------------------------------------------------------------------------
; Register Addresses
HDR RQU SFFFFC9 ; PS- Host port GPIO data Register
HDDR RQU SFFFFCA ; PS- Host port GPIO direction Register
PCRC RQU SFFFFBF ; Port C Control Register
PRRC RQU SFFFFBE ; Port C Direction Register
PBC RQU SFFFFBD ; Port C GPIO Data Register
PCBD RQU SFFFFBF ; Port D Control register
PRBD RQU SFFFFBE ; Port D Direction Data Register
PBRD RQU SFFFFAD ; Port D GPIO Data Register
PCRE RQU SFFFFAE ; Port E Control register
PREE RQU SFFFFAE ; Port E Direction Register
PORE RQU SFFFFAD ; Port E Data Register
OGDB RQU SFFFFFC ; OnCE GDB Register
EQUATES for GPIOs

--- Register Addresses ---
GPIOCTRL EQU $FFFFc4    ; Host Port Control Register
GPIODIR EQU $FFFFc8     ; GPIODIR register. [HI - HDIR]
GPIODAT EQU $FFFFc9     ; GPIODAT register. [HI - HDR]

--- Bit Definitions for GPIO Direction Register ---
GPIO0_DIR EQU $0
GPIO1_DIR EQU $1
GPIO2_DIR EQU $2
GPIO3_DIR EQU $3
GPIO4_DIR EQU $4
GPIO5_DIR EQU $5
GPIO6_DIR EQU $6
GPIO7_DIR EQU $7
GPIO8_DIR EQU $8

--- Bit Definitions for GPIO Data Register ---
GPIO0_DAT EQU $0
GPIO1_DAT EQU $1
GPIO2_DAT EQU $2
GPIO3_DAT EQU $3
GPIO4_DAT EQU $4
GPIO5_DAT EQU $5
GPIO6_DAT EQU $6
GPIO7_DAT EQU $7
GPIO8_DAT EQU $8

--- EQUATES for Timer ---

--- EQUATES for Enhanced Synchronous Serial Interface (ESSI) ---

;ESSI 0 interrupt equates
essi0_rdf equ $30
essi0_roe equ $32
essi0_rls equ $34
Appendix 1

Appendix 1

essi0_tde equ $36
essi0_tue equ $38
essi0_tls equ $3a

; ESSI 1 interrupt equates
essi1_rdf equ $40
essi1_roe equ $42
essi1_rls equ $44
essi1_tde equ $46
essi1_tue equ $48
essi1_tls equ $4a

; Register Addresses of ESSI0
M_TX00 EQU $FFFFBC ; SSI0 Transmit Data Register 0
M_TX01 EQU $FFFFBB ; SSI0 Transmit Data Register 1
M_TX02 EQU $FFFFBA ; SSI0 Transmit Data Register 2
M_TSR0 EQU $FFFFB9 ; SSI0 Time Slot Register
M_RX0 EQU $FFFFB8 ; SSI0 Receive Data Register
M_SSISR0 EQU $FFFFB7 ; SSI0 Status Register
M_CRB0 EQU $FFFFB6 ; SSI0 Control Register B
M_CRA0 EQU $FFFFB5 ; SSI0 Control Register A
M_TSMA0 EQU $FFFFB4 ; SSI0 Transmit Slot Mask Register A
M_TSBM0 EQU $FFFFB3 ; SSI0 Transmit Slot Mask Register B
M_RSMA0 EQU $FFFFB2 ; SSI0 Receive Slot Mask Register A
M_RSMB0 EQU $FFFFB1 ; SSI0 Receive Slot Mask Register B

; Register Addresses of ESSI1
M_TX10 EQU $FFFFAC ; SSI1 Transmit Data Register 0
M_TX11 EQU $FFFFAB ; SSI1 Transmit Data Register 1
M_TX12 EQU $FFFFAA ; SSI1 Transmit Data Register 2
M_TSR1 EQU $FFFFA9 ; SSI1 Time Slot Register
M_RX1 EQU $FFFFA8 ; SSI1 Receive Data Register
M_SSISR1 EQU $FFFFA7 ; SSI1 Status Register
M_CRB1 EQU $FFFFA6 ; SSI1 Control Register B
M_CRA1 EQU $FFFFA5 ; SSI1 Control Register A
M_TSMA1 EQU $FFFFA4 ; SSI1 Transmit Slot Mask Register A
M_TSBM1 EQU $FFFFA3 ; SSI1 Transmit Slot Mask Register B
M_RSMA1 EQU $FFFFA2 ; SSI1 Receive Slot Mask Register A
M_RSMB1 EQU $FFFFA1 ; SSI1 Receive Slot Mask Register B

; EQUATES for SCI
PCRE_ADR EQU $FFFF9F ; Serial Port Control Register
PRRE_ADR EQU $FFFF9E ; Serial Port Direction Register
PDDR_ADR EQU $FFFF9D ; Serial Port Direction Register
SCHD_ADR EQU $FFFF9C ; SCI Control Register
SCCB_ADR EQU $FFFF9B ; SCI Clock Control Register
SKH_ADR EQU $FFFF9A ; Serial Receive Register high
SKM_ADR EQU $FFFF99 ; Serial Receive Register mid
SKL_ADR EQU $FFFF98 ; Serial Receive Register low
STMH_ADR EQU $FFFF97 ; Serial Transmit Register high
STMB_ADR EQU $FFFF96 ; Serial Transmit Register mid
STML_ADR EQU $FFFF95 ; Serial Transmit Register low
STKA_ADR EQU $FFFF94 ; Serial Transmit Address Register
SSR_ADR EQU $FFFF93 ; Serial Status Register
EQUATES for Expansion Port

EXP_BCR EQU $FFFFFB ; Bus Control Register address
EXP_AAR0 EQU $FFFFF9 ; Address Attribute Register (AAR0) address
EXP_AAR1 EQU $FFFFF8 ; Address Attribute Register (AAR1) address
EXP_AAR2 EQU $FFFFF7 ; Address Attribute Register (AAR2) address
EXP_AAR3 EQU $FFFFF6 ; Address Attribute Register (AAR3) address
EXT_RAM_START EQU $C00000

EQUATES for Extended Memory

EDC_ADR EQU $FFFFCA

--------------------------------------------------------------------------------
//*********************************************************
//********** Initialisation Values ***********************
//*********************************************************
--------------------------------------------------------------------------------

CODEC Initialisation values

--- INIT_CODEC_CSR ---
settings for the CODEC Control Register

INIT_CODEC_CSR EQU %000000001110011011011011  ; $00E6DB  DACgain = 0dB - ADCgain = +0dB

BDCL[0:2] = 321098765432109876543210

GADCL[0:2] = 011

GADCR[0:2] = 011

GDACL[0:2] = 011

GDACR[0:2] = 011

GADAC[0:2] = 011

MUTEDAC = 0

PDNDAC = 1

PDNADC = 1

NRST = 1

SAI Initialisation values

--- INIT_SAI_RCS ---
settings for the SAI Control/Status Register

INIT_SAI_RCS EQU %000000000001000010100101  ; $000149

R0EN = 1

R1EN = 0

R2EN = 0

RMSE = 1

RCLR[0:1] = 00

RDIR = 0

RLRS[0:1] = 1

RCKP = 0

RXE = 0

RDIRJ = 0

RXIE = 1

ROFL = 0

29/42
### Appendix 1: TDA7590

--- INIT_TCS ---

settings for the Transmitter Control/Status Register

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Binary</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RDR</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>ROFCL</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

INIT_TCS_EQU $000549

--- PLL CSR ---

settings for the PLL control register

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Binary</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>IDFE = 0 (actual = IDFE + 1 = 1)</td>
<td>0000</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>RESERVED</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>LOCK (read only; 0: out of lock)</td>
<td>0001</td>
<td>011</td>
</tr>
<tr>
<td>0</td>
<td>OUTLOCK (read only; 0: in lock)</td>
<td>0001</td>
<td>011</td>
</tr>
<tr>
<td>0</td>
<td>MF + 12 (actual = MF + 1 = 13)</td>
<td>0001100</td>
<td>001</td>
</tr>
<tr>
<td>0</td>
<td>PLLIE (0: intr disable)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>PWRDN (1: power down mode)</td>
<td>0</td>
<td>011</td>
</tr>
<tr>
<td>0</td>
<td>DITEN (0: disable)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>FRACTN (0: disable)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>PEN (1: PLL enable)</td>
<td>0</td>
<td>011</td>
</tr>
</tbody>
</table>

PLL_CSR_EQU $0E0C00

--- FRACT ---

settings for the Fractional N part of the PLL

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Binary</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>MF + 12 (actual = MF + 1 = 13)</td>
<td>00010000</td>
<td>001</td>
</tr>
<tr>
<td>0</td>
<td>PWRDN (1: power down mode)</td>
<td>0</td>
<td>011</td>
</tr>
<tr>
<td>0</td>
<td>DITEN (0: disable)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>FRACTN (0: disable)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>PEN (1: PLL enable)</td>
<td>0</td>
<td>011</td>
</tr>
</tbody>
</table>

FRACT_EQU $0034bd

--- CLKCTL ---

settings for the Fractional N part of the PLL

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
<th>Binary</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PEN (1: PLL enable)</td>
<td>0</td>
<td>011</td>
</tr>
</tbody>
</table>

CLKCTL_EQU $0034bd
; settings for the clock control register
; 321098765432109876543210

;INIT_PLL_CLKCTL EQU $018cc1

;INIT_PLL_CLKCTL EQU $000000010000000100000001 ; $018cc1
;
; 001 --- DSPDF =1 (actual = DSPDF+1=3)
;
; 00 --------- TESTSEL
;
; 1 --------- DCKSRC (0:XTI; 1:FVCO)
;
; 1 -------------- DACLEN (1: enable CODEC clocks)
;
; 000010 -------- MFSDF =2 (actual =MFSDF+1 = 3 )
;
; 011 ------------------ SEL (000:128,001:256, 010:384, etc)
;
; 0 ------------------------- DSP_XTI (0:vco/DSPDF; 1:stl)
;
; 0 -------------------------- DAC_SEL (0:vco/MFSDF; 1:ext_dac_clk)
;
; 0 -------------------------- XTLD (0:Enabled; 1:Disabled)

ENDIF ; Settings per sci 115200

;------------------------------------------------------------------------
; Timer Initialisation values
;------------------------------------------------------------------------

--- TCSR0 --------------------------------------------------------------------

settings for the Timer Control/Status Register
; 321098765432109876543210

INIT_TCSR0 EQU %000000001000101000000100 ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out
INIT_TCSR1 EQU %000000001000101000000100 ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out
INIT_TCSR2 EQU %000000001000101000000100 ; $8A04    mode0 / trm=1 / tce=1 / pce=1/ dir=out

; xx ----------------------->[23-22]; unused
; 0 --------------------->[21] TCF ; Timer Compare Flag
; 0 --------------------->[20] TOF ; Timer Overflow Flag
; xxxx ------------------>[19-16]; unused
; 0 ---------------------->[15] PCE ; Prescaler Clock Enable
; x ---------------------->[14]; unused
; 0 ---------------------->[13] DO ; Data Output
; 0 ---------------------->[12] DI ; Data Input
; 1 ---------------------->[11] DIR ; Direction
; x ---------------------->[10]; unused
; 1 ------------------------>[ 9] TRM ; Timer Reload Mode
; 0 ------------------------>[ 8] INV ; Inverter
; 0000 ---------------->[7-4] Tc[3-0] ; Timer Control = Mode0
; x ---------------->[3]; unused
; 1 ---------------->[ 2] TCIE ; Timer Compare Interrupt Enable
; 0 -->[ 1] TOIE ; Timer Overflow Enable
; 0 -->[ 0] TE ; Timer Enable

--- TLR0 --------------------------------------------------------------------

; settings for the Timer Load Register

INIT_TLR0 EQU $000000
INIT_TLR1 EQU $000000
INIT_TLR2 EQU $000000

--- TCPR0 --------------------------------------------------------------------

; settings for the Timer Compare Register

;INIT_TCPR0 EQU $000002
;INIT_TCPR1 EQU $000004
;INIT_TCPR2 EQU $000008
INIT_TCPR0 EQU $000000
INIT_TCPR1 EQU $000000

31/42
Appendix 1

INIT_TCPR2 BQU $000000

;--- TPLR -----------------------------------------------
; settings for the clock control register
; 321098765432109876543210
;INIT_TPLR BQU $00100000000000001111100111 ; $2003E7 source TIO0 / divider = 999+1
INIT_TPLR BQU $000000000000111110011111 ; $0003E7 source internal / prescaler 999

;------------------------> Reserved. Write to zero for future compatibility.
; 01----------------------> PS[1-0] ; Prescaler Source [00 internal / 01 internal TIO0 /
; 10  external TIO0 / 11  external TIO0]
; 000000000001000000000000-> PL[20-0] ; Prescaler Preload Value 20400

;------------------------> PS[1-0] ; Prescaler Source [00 internal / 01 internal TIO0 /
; 10  external TIO0 / 11  external TIO0]
; 000000000001000000000000-> PL[20-0] ; Prescaler Preload Value 20400

;--- INIT_IPR_C --------------------------------------------------
; settings for the Interrupt priority register - Core
; 321098765432109876543210
INIT_IPR_C BQU $000000000000000000000000 ; $000000

;--- INIT_IPR_P --------------------------------------------------
; settings for the Interrupt priority register - peripherals
; 321098765432109876543210
INIT_IPR_P BQU $00000000000011111001000100 ; $29C4 glitch sull'uscita del dac
; 00----- HI
; 11----- ESSI0
; 00----- ESSI1
; 11------- SCI
; 11-------- SCI
; 11--------- SCI
; 11---------- SCI
; 11------------ SCI
; 11 ------------- SAI
; 11 --------------- SAI
; 11 ---------------- CODEC
; 00 ----------------- PLL
; 00 ------------------- Unknow
; 00 ---------------------- I2C
; 00 ----------------------- SPI
; 00 ------------------------ EMI

;--- INIT_AAR0 --------------------------------------------------
; settings for the Address Attribute Register1
; 321098765432109876543210
INIT_AAR0 BQU $110000000000000100000000000000000 ; C04410
; 00 ---- BAT (00: Synchronous SRAM; 01: DRAM; 10: DRAM; 11: Reserved)
; 0 ---- BAAP (0:AA1 active low; 1:AA1 active high)
; 0 ---- BPEN (0: P space disabled; 1: P space enabled)
; 1 ---- BXEN (0: X data space disabled; 1: X data space enabled)
; 0 ---- BYEN (0: Y data space disabled; 1: Y data space enabled)
; 0 ---- BAM (0: 8 LSB of address will appear on A0-A7; 1: 8 LSB of address will appear on A16-A23)
; 0 ---- BPAC (0: packing disabled; 1: packing enabled)
; 0100 ---- BNC (Number of bits to compare; 1111, 1110, 1101 reserved)
; 110000000000000000 ---- BAC (Address to compare; BAC most significant)

;--- INIT_BCR --------------------------------------------------
; settings for the Bus Control Register

; INIT_BCR EQU $001100000010010000100001 ; 306E10
; INIT_BCR EQU $00000011111111111100110111 ; 30FE07
;
; 00111 ---- BAW (Area 0 wait states)
; 00000 ------- BA1W (Area 1 wait states)
; 111 --------- BA2W (Area 2 wait states)
; 111 ------------ BA3W (Area 3 wait states)
; 00000 -------------- BDPM (Default area wait states)
; 0 ----------------- BBS (0: ; 1: DSP is bus master READ ONLY)
; 0 ----------------- BLH (0: ; 1: BLN always asserted)
; 0 ----------------- BRH (0: ; 1: BRN always asserted)

; definitions added by Paul Cassidy for salieri testbench
TRIGGER_TUBE EQU $12002
M_BCR EQU $FFFFFB ; Bus Control Register
M_AAR0 EQU $FFFFF9 ; Address Attribute 0
M_AAR1 EQU $FFFFF8 ; Address Attribute 1
M_AAR2 EQU $FFFFF7 ; Address Attribute 2
M_AAR3 EQU $FFFFF6 ; Address Attribute 3

;*******************************************************************************
;************************** Main Prog Starts Here ****************************
;*******************************************************************************
startp
org p:$0
jmp start

sci_int
org p:SCI_REC ; Interrupt SCI receive
jsr INT_SCIR

org p:SCI_TRANS ; Interrupt SCI transmit
jsr INT_SCIT

org p:SCI_REC_E ; Interrupt SCI framing error
jsr INT_SCIE

sai_int
org p:SAI_RDR
jsr INT_RDR

org p:SAI_TDE
jsr INT_TDE

org p:SAI_ROF
jsr INT_ROF

org p:SAI_TUF
jsr INT_TUF

essi_int
org p:essi0_rdf
jsr Comp_0
nop
org p:essi0_roe


```assembly
movep x:M_SSISR, a0
move x:M_RX0, y:(r0)+
org p:essi0_rls
nop
org p:essi0_tde
jra clr_tde0
nop
org p:essi0_tue
jra clr_tue0
nop
org p:essi0_tls
nop
nop

timer_int
  org p:Timer0_tcf
  jra INT_TMR0_tcf
  org p:Timer0_tof
  jra INT_TMR0_tof
  org p:Timer1_tcf
  jra INT_TMR1_tcf
  org p:Timer1_tof
  jra INT_TMR1_tof
  org p:Timer2_tcf
  jra INT_TMR2_tcf
  org p:Timer2_tof

  org x:0
  states dsm ntaps

  org y:0
coef  do .1,.3,-.1,.2

org p:$100
start
; setup external memory for sync with testbench
;------------------------------------------------------------------------
;   Initialise Core
;------------------------------------------------------------------------
clr     a
clr     b
move    #$0,r0
move    #$fff,m0
ori     #$3,mr ; mask interrupts
movep   #INIT_IPR_C,x:IPR_C ; set CORE interrupt priorities
movep   #INIT_IPR_P,x:IPR_P ; set PERIPHERAL interrupt priorities

;------------------------------------------------------------------------
;   Initialise PLL
;------------------------------------------------------------------------
init_pll
movep   #INIT_PLL_CSR,x:PLL_CSR ; enable the pll.
jclr    #LOCK,x:<<PLL_CSR,* ; wait for lock.
```
movep #INIT_PLL_FCR,x:PLL_FCR          ; set fract value.
bset    #FRACEN,x:<<PLL_CSR              ; enable fractional-n operation.
movep   #INIT_PLL_CLKCTL,x:PLL_CLKCTL   ; setup the clock generation.

IF 1
;------------------------------------------------------------------------
; Initialise CODEC
;------------------------------------------------------------------------
init_codec
movep   #INIT_CODEC_CSR,x:CODEC_CSR     ; initialise CODEC control/status reg

;------------------------------------------------------------------------
; Initialise SAI
;------------------------------------------------------------------------
; The receiver and transmitter control/status register are configured the same for simplicity only.
; Master mode , 24-bit word-size , MSB first , Low word clock = left word , Neg bit-clk polarity ,
; Non i2s format , (For 32-bit words) First bit x 8 , Interrupts enabled.
init_sai
movep   #INIT_SAI_TCS,y:SAI_TCS         ; initialise transmit control/status reg
movep   #INIT_SAI_RCS,y:SAI_RCS         ; initialise receiver control/status reg

;------------------------------------------------------------------------
; Enable gpios for HI
;------------------------------------------------------------------------
bset  #GPIO0_DIR,x:GPIOCTRL     ; Setup HI pin for GPIO mode
bset  #GPIO0_DIR,x:GPIODIR      ; Setup GPIO as output
bset  #GPIO1_DIR,x:GPIOCTRL     ; Setup HI pin for GPIO mode
bset  #GPIO1_DIR,x:GPIODIR      ; Setup GPIO as output
ENDIF

;------------------------------------------------------------------------
; Initialize ESSI0
;------------------------------------------------------------------------
IF 1
init_essi
movep #2181801,x:M_CRAS          ; cra0_addr, 24'b010110000001100000011110
         ; The divider control is set to 1 (2 words per frame)
         ; for Normal mode, bits are left aligned to bit 23. Word
         ; length is set to 24 bits.PM = 1 -> Fcore/4.
movep #0fc113e,x:M_CRBS          ; crb0_addr, 24'b11111111000001010101011110
         ; The receive exception and transmit exception interrupts
         ; are enabled as are receive last slot and transmit last
         ; slot. It is set in the synchronous normal mode. Data and
         ; frame sync are clocked out on the rising edge of the clock.
         ; Frame sync polarity is positive and occurs together with the
         ; the first bit of data from the first slot. MSB is shifted
         ; first. SC2 o/p SC1 o/p SC0 o/p
Enable_pins

movep #0000000f,x:M_PCRC         ; // ALL Pins are ESSI.
         ; check that all pins are enabled
rep   #005
ncp
movep b1,x:M_CRB0
ENDIF

IF 1
------------------------------------------------------------------------
; Enable gpios for TIMER
------------------------------------------------------------------------
init_gpio
; movep #$000000,x:<<PCRC ; ESSI0 port as GPIO
; movep #$0000ff,x:<<PCRC ; ESSI0 port as OUT
Movep #$000000,x:<<PRRD ; ESSI1 port as TIMER(INPUT)
Movep #$000000,x:<<PRRD ; ESSI1 port as GPIO

;------------------------------------------------------------------------
; Initialise Timer
;------------------------------------------------------------------------
init_timer
bclr #0,x:M_TCSR0 ; Disable Timer0
bclr #0,x:M_TCSR1 ; Disable Timer1
bclr #0,x:M_TCSR2 ; Disable Timer2
movep MINIT_TCSR0,x:<<M_TCSR0 ; Timer0 enable at mode 0 + reload
movep MINIT_TPLR,x:<<M_TPLR ; Initial value of the timer counter
movep MINIT_TLR0,x:<<M_TLR0 ; Initial value of the timer counter
movep MINIT_TCPR0,x:<<M_TCPR0 ; Number of CLK/2 cycles until a trigger is generated
movep MINIT_TCSR1,x:<<M_TCSR1 ; Timer1 enable at mode 0 + reload
movep MINIT_TPLR,x:<<M_TPLR ; Initial value of the timer counter
movep MINIT_TLR1,x:<<M_TLR1 ; Initial value of the timer counter
movep MINIT_TCPR1,x:<<M_TCPR1 ; Number of CLK/2 cycles until a trigger is generated
movep MINIT_TCSR2,x:<<M_TCSR2 ; Timer2 enable at mode 0 + reload
movep MINIT_TPLR,x:<<M_TPLR ; Initial value of the timer counter
movep MINIT_TLR2,x:<<M_TLR2 ; Initial value of the timer counter
movep MINIT_TCPR2,x:<<M_TCPR2 ; Number of CLK/2 cycles until a trigger is generated

;------------------------------------------------------------------------
; Initialise Expansion Port and Flex Memory
;------------------------------------------------------------------------
init_expport
movep #INIT_AAR0,x:EXP_AAR0 ; initialise AAR0 control/status reg
movep #INIT_BCR,x:EXP_BCR ; initialise BCR reg
ENDIF

;------------------------------------------------------------------------
; Initialise SCI
;------------------------------------------------------------------------
init_sci
movep #$E,x:SCCR_ADR
movep #$7,x:PCRE_ADR
movep #$1b02,x:SCR_ADR
Andi #$fc,mr            ; set DSP interrupt priority level to 0
; Sets the Interrupt Mask bits in the SR
; to [00] (No exceptions masked)

IF 1
Bset #0,x:M_TCSR0       ; Enable Timer0
Bset #0,x:M_TCSR1       ; Enable Timer1
Bset #0,x:M_TCSR2       ; Enable Timer2
ENDIF

move    #states,r3
move    #ntaps-1,m3
move    #coef,r4
move    #ntaps-1,m4

;------------------------------------------------------------------------
; Processor Loop
;------------------------------------------------------------------------

IF 0
LOOP
    bset    #12,x:SCR_ADR                           ; start SCI transmit
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    jmp LOOP
ENDIF

IF 1
LOOP
    bset    #12,x:SCR_ADR                           ; start SCI transmit
    mac     x0,y0,a     x:(r3)+,x0      y:(r4)+,y0   ; generates variations on mean value of DAC
    move    #$AAAAAA,x0
    move    x0,x:$CAAAAA                             ; send data to expansion port
    move    x0,x:GPIODAT                             ; move PORTB pins
    jmp LOOP
ENDIF

IF 1
LOOP
    bset    #12,x:SCR_ADR                           ; start SCI transmit
    mac     x0,y0,a     x:(r3)+,x0      y:(r4)+,y0   ; generates variations on mean value of DAC
    move    #$555555,x0
    move    x0,x:$C55555                             ; send data to expansion port
    move    x0,x:GPIODAT                             ; move PORTB pins
Appendix 1

TDA7590

bset #12,x:SCR_ADR ; start SCI transmit
mac x0,y0,a x:(r3)+,x0 y:(r4)+,y0 ; generates variations on mean value of DAC
move #AAAAAAA,x0
move x0,x:SCAAAAAA ; send data to expansion port
move x0,x:GPIODAT ; move PORTB pins

bset #12,x:SCR_ADR ; start SCI transmit
mac x0,y0,a x:(r3)+,x0 y:(r4)+,y0 ; generates variations on mean value of DAC
move #555555,x0
move x0,x:SC55555 ; send data to expansion port
move x0,x:GPIODAT ; move PORTB pins

jmp LOOP
endif

------------------------------------------------------------------------
| Interrupt Service Routines |
------------------------------------------------------------------------

; SAI

INT_TDE ; The transmitter data empty flag is cleared as soon
; as the last move is performed
movep a,y:<<SAI_TX0 ; Load LEFT transmit data register for channel 0
nop
nop
movep b,y:<<SAI_TX0 ; Load RIGHT transmit data register for channel 0
rti

INT_RDR ; The receiver data ready flag is cleared as soon
; as the last move is performed
move y:<<SAI_RX0,a ; Move Channel 0 received LEFT data to x-memory.
move a,x:(r0)
nop
nop
move y:<<SAI_RX0,b ; Move channel 0 received RIGHT data to y-memory.
move b,y:(r0)+
rti

INT_ROF
bset #16,y:SAI_RCS
bclr #16,y:SAI_RCS
rti

INT_TUF
bset #16,y:SAI_TCS
bclr #16,y:SAI_TCS
rti

; TIMER
```assembly
;------------------------------------------------------------------------
; INT_TMR0_tcf
;   bchg #0,x:PDRC              ; toggle pin12 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
   bchg #13,x:M_TCSR0            ; toggle TIO0 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
  nop
  rti

INT_TMR0_tof
  nop
  nop
  rti

INT_TMR1_tcf
;    bchg #1,x:PDRC               ; toggle pin4 Fout=Fin/((TPLR+1)*(TCPR+1)*2)
   bchg #13,x:M_TCSR1            ; toggle TIO1 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
  nop
  rti

INT_TMR1_tof
  nop
  nop
  rti

INT_TMR2_tcf
;    bchg #2,x:PDRC               ; toggle pin3  Fout=Fin/((TPLR+1)*(TCPR+1)*2)
   bchg #13,x:M_TCSR2            ; toggle TIO2 Fout=(XTI/2)/((TPLR+1)*(TCPR+1)*2)
  nop
  rti

INT_TMR2_tof
  nop
  nop
  rti

; ESSI
;------------------------------------------------------------------------
clr_tde0
  movep r1,x:M_TX00
  move (r1)+
  movep r1,x:M_TX01
  move (r1)+
  movep r1,x:M_TX02
  move (r1)+
  rti

clr_tue0
  movep x:M_SSISR0,a0
  movep r1,x:M_TX00
  move (r1)+
  movep r1,x:M_TX01
  move (r1)+
  movep r1,x:M_TX02
  move (1)+
  rti

Comp_0
  rti
```
Appendix 1

Clr_gpio
bclr #0,x:M_PDRE
rti

Comp_1
rti

;SCI

INT_SCIR
  move x:SKXL_ADR,x0
  movep #$3f02,x:SCR_ADR
  move x0,x:(r1)+
  move x0,x:$C00000
  rti

INT_SCIT
  movep x0,x:STXA_ADR
  movep #$000041,x:STXA_ADR
  movep #$000061,x:STXA_ADR
L3
  jclr #0,x:<<SSR_ADR,L3
  movep #$12f02,x:SCR_ADR
  rti

INT_SCIE
  jclr #FRAMING,x:SSR_ADR,NO_FRA
L2
  jclr #0,x:<<SSR_ADR,L2
  movep #$21,x:STXA_ADR
NO_FRA
  nop
  move x:SKXL_ADR,x0
  rti
## Revision history

Table 8. Document revision history

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>11-Apr-2006</td>
<td>1</td>
<td>Initial release.</td>
</tr>
<tr>
<td>26-Jan-2009</td>
<td>2</td>
<td>Document status promoted from preliminary data to datasheet. Updated Section 8: Package information on page 22.</td>
</tr>
<tr>
<td>23-Sep-2013</td>
<td>3</td>
<td>Updated Disclaimer.</td>
</tr>
</tbody>
</table>