RM0345
Reference manual

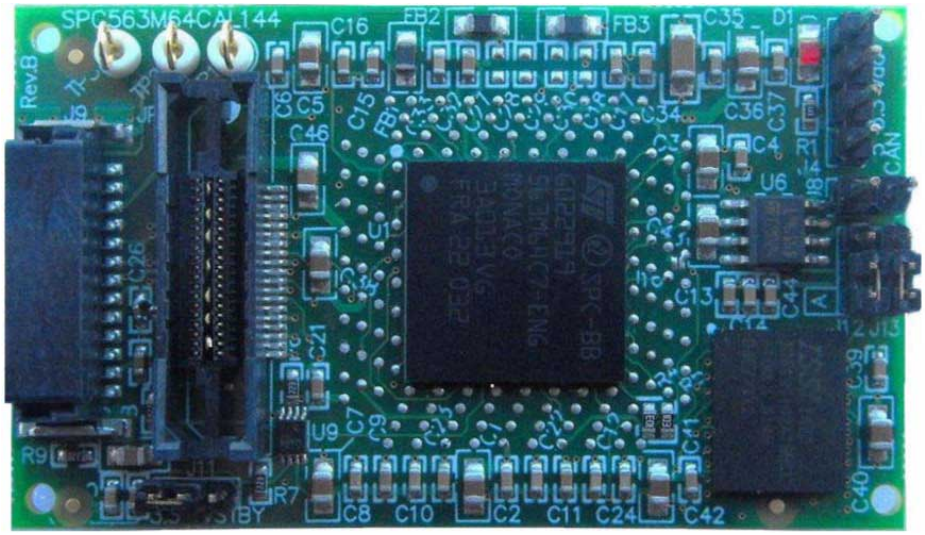
SPC563M64CAL144
calibration adapter board for SPC563M64xx devices

Introduction

The SPC563M64CAL144 (rev.B) system is designed to enable the use of new enhanced automotive calibration and debug tools on the SPC563M64xx family of automotive microcontrollers.

The SPC563M64CAL144 (rev.B) can be fitted onto the application printed circuit board (PCB) in place of the standard SPC563M64xx family microcontroller in LQFP144 package. SPC563M64CAL144 (rev.B) hardware is designed to support two standardized tool connectors, allowing a variety of calibration and debug hardware to be connected and reused

Figure 1. SPC563M64CAL144 (rev.B)



GAPGRI0039

Table 1. Board summary

Order code	On board device	Target footprint
SPC563M64CAL144	SPC563M64xx	QFP144

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1 Calibration system overview

The Calibration Adapter board features 2 Mbytes of SRAM in order to substitute to the SPC563M64xx internal Flash during calibration.

A voltage regulator is also integrated upon the board to generate, from selectable 5 V source, the 3.3 V voltage for the RAM and the calibration bus interface.

Development connector (Mictor AMP38) is providing the interface for the debug and trace tools.

A calibration connector (ERNI 154819) is providing an interface optimized for calibration usage.

A high speed CAN transceiver is connected to the FlexCAN of the mcu device.

The components chosen in the design of this board are automotive qualified to allow system evaluation over the full automotive evaluation range (-40 °C to 125 °C).

1.1 Features overview

calibration systems include these distinctive features:

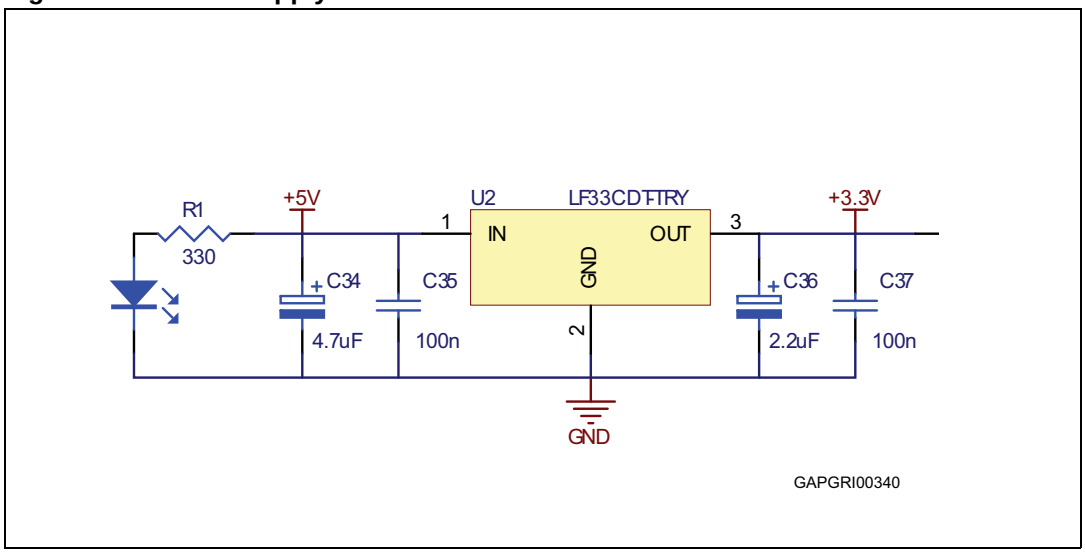
- Use 100% production silicon, ensuring full hardware and software compatibility between production and calibration systems;
- Support LQFP144 MCU production package allowing calibration systems to be built without requiring modifications to the standard production system housing;
- 2MByte static RAM organized as 1024K words by 16 bits;
- On-board latch providing a 16-bit de-multiplexed bus interface from the SPC563M64xx 16-bit multiplexed calibration interface;
- Support for Nexus-based debug tools even if application PCB does not include Nexus connector;
- Nexus functionality with 12 Message Data Out (MDO) signals;
- Support for full-feature calibration tools, via availability of comprehensive set of device signals available on the connectors;
- ERNI 154819 connector optimized for calibration;
- High speed CAN transceiver with signals protection;
- Allows system calibration without impacting standard MCU I/O resources;
- Allows system calibration regardless of availability of standard MCU external bus;
- Uses tried and tested technology.

2 Power supply

The Calibration boards requires a +5 V to supply the on board CAN transceiver and a +3.3 V to supply the SPC563M64xx calibration bus interface and for the external RAM.

The 3.3 V supply is generated on the SPC563M64CAL144 (rev.B) via the very low drop voltage regulator by using the +5V. A LED (D1) will light when the board is powered.

Figure 2. Power supply



By default the 5V is taken from the target application through the VDDREG supply level (supply input for the internal voltage regulators of the SPC563M64xx). Gauge J14 enables the powering from the application board. *Table 2* shows its option configuration.

In case that no additional power loading could be applied to the application system during calibration, the +5V can be supplied externally via J4 connector (+5V test point, see *Figure 4*) and the gauge J14 (see *Figure 3*) must be open.

Figure 3. Supply signals from the QFP144 footprint

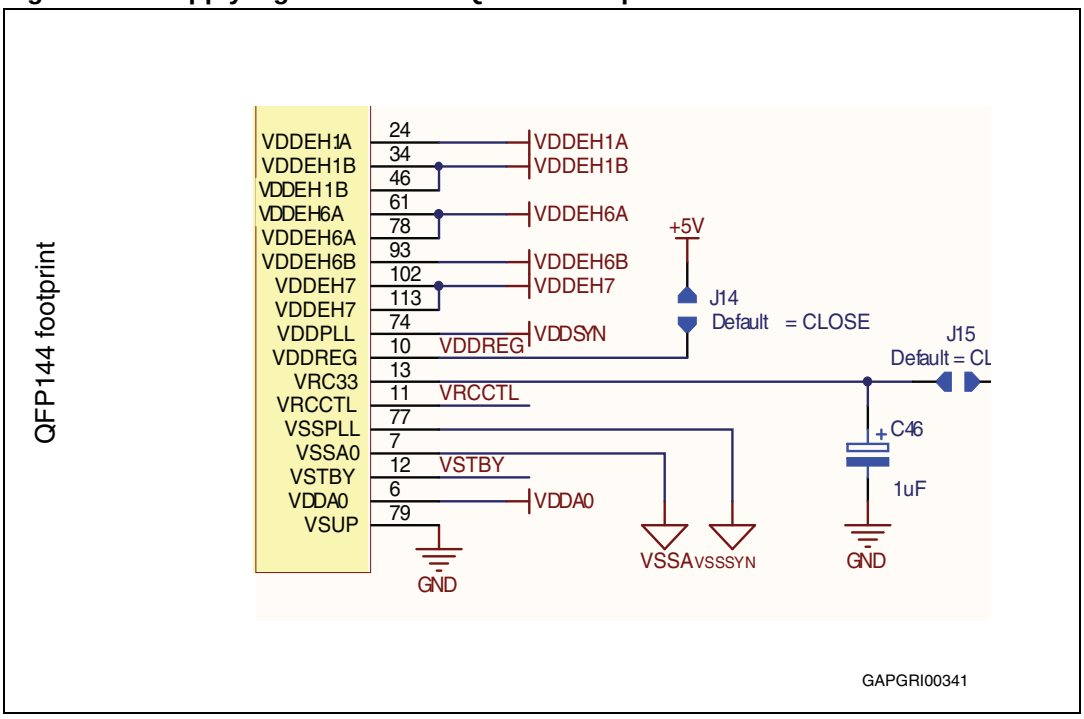
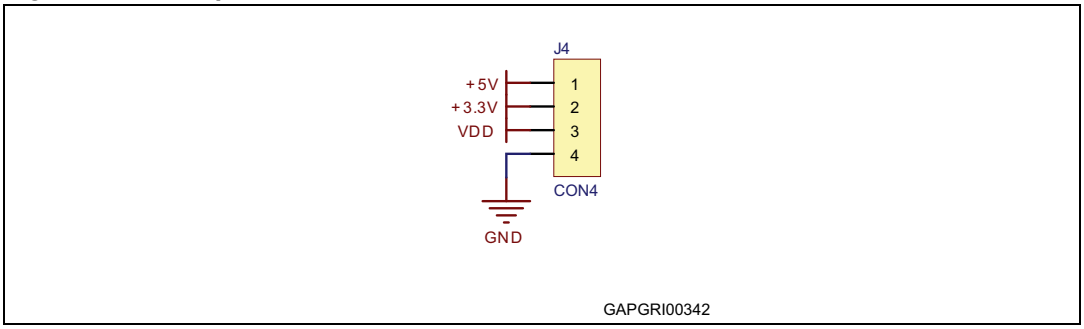


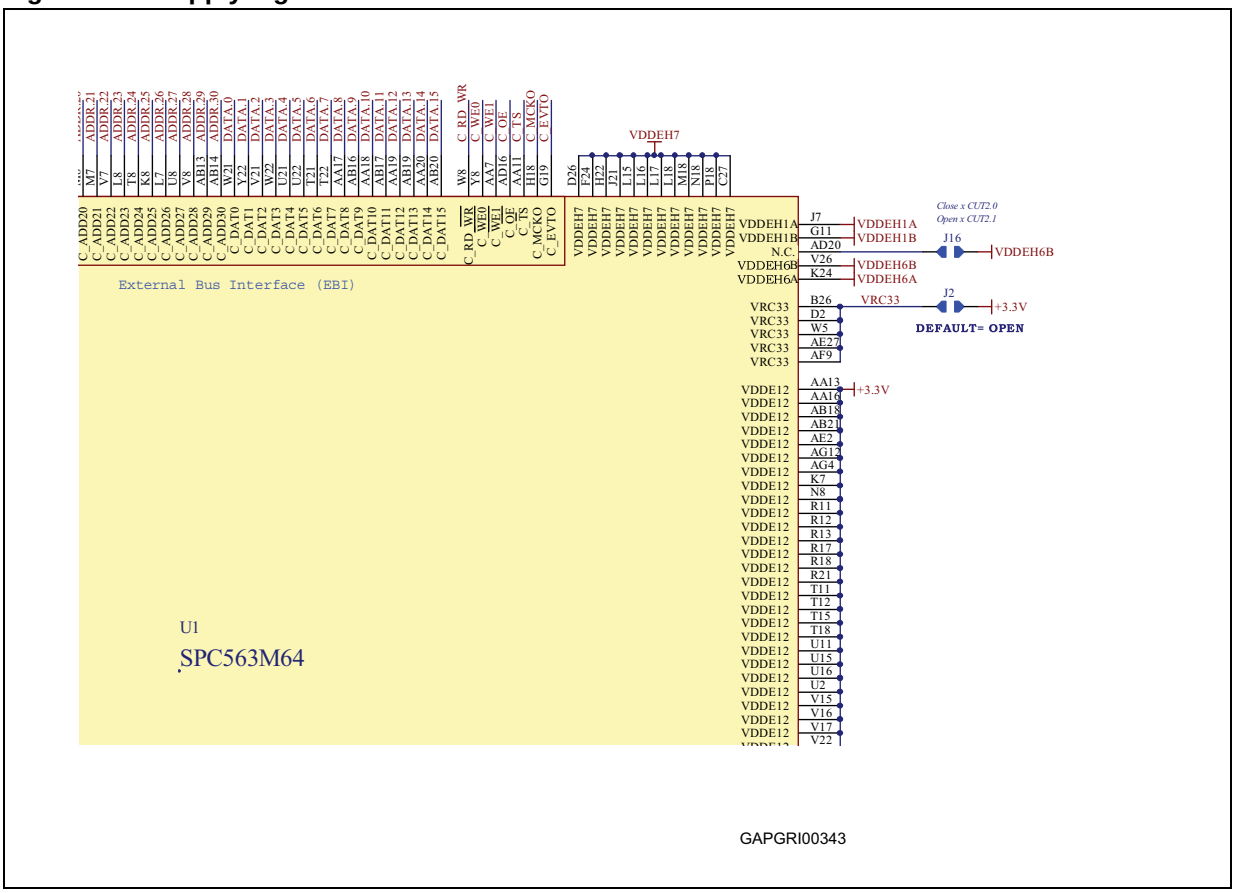
Figure 4. Test points on J4 connector



All power signals and voltage references of the SPC563M64xx QFP144 footprint from the application board are directly connected to the respective calibration device signals.

The VDDE12 supply used to power the dedicated SPC563M64xx calibration bus interface is connected to the upon board +3.3 V voltage regulator.

Figure 5. Supply signals on SPC563M64xx CSP496



The VRC33 signal of the CSP496 is connected to its respective signal of the QFP144 target application via the J15 cut trace option.

The VRC33 can be also connected to the on board +3.3V by closing the J2 gauge. In this case the gauge J15 must be open (*Table 2*).

Table 2. J15, J2 and J14 option cut traces(1)

Option name	Function	Value	Note
J15	VRC33	open	VRC33 signal is disconnected from the target application board
		close (default)	VRC33 signal is connected to the target application board
J2	VRC33	open (default)	VRC33 signal is disconnected from the on board +3.3V signal
		close	VRC33 signal is connected to the on board +3.3V signal
J14	+5V supply	open	+5V is powered from J4 connector
		close (default)	+5V is powered from target application via VDDREG pin of the QFP144 target footprint

1. Refer to *Chapter Appendix D: Options placement* for layout Jumper placement

3 Reset and configuration signals

Calibration and debug tools may use the reset signals included in the connectors to have visibility of when the SPC563M64xx device has been reset. Debug tools may also require the ability to force device reset.

All signals of the SPC563M64xx QFP144 footprint from the application board are directly connected to the respective calibration device signals. This includes the following signals on the *Table 3*.

Table 3. Reset and configuration signals

Signal name	Function	Notes
Reset / Configuration (5)		
/RESET	External reset input	The /RESET pin is an active low input. The RESET pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the RESET pin asserts for 10 clock cycles. Assertion of the RESET pin while the device is in reset causes the reset cycle to start over.
/RSTOUT	External reset output	The RSTOUT pin is an active low output that uses a push/pull configuration. The RSTOUT pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the RSTOUT pin.
BOOTCFG[1]	Boot configuration input	The BOOTCFG field holds the value of the BOOTCFG[1] pin that was latched on the last negation of the RSTOUT pin. The BOOTCFG field is used by the BAM program to determine the location of the Reset Configuration Word.
PLLREF	FMPLL Mode Selection	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. If RSTCFG is 0, External reference clock selected. If RSTCFG is 1, Xtal oscillator mode is selected
WKPCFG	Weak Pull Configuration	The signal on the WKPCFG pin determines whether weak pull up or pull down devices are enabled after reset on the eTPU and eMIOS pins. 0: Weak pulldown applied to eTPU and eMIOS pins at reset 1: Weak pullup applied to eTPU and eMIOS pins at reset.

4 Calibration bus interface and External Memory

The SPC563M64xx features a 16-bit de-multiplexed calibration bus interface that is connected to an external 2Mbyte SRAM thanks to an on board latch.

4.1 External memory specification

The calibration board provides a SRAM with the following characteristics:

- 2Mbyte static RAMs organized as 1024K words by 16 bits;
- 16-bit data width;
- Fully static operation: no clock or refresh required;
- 3.3V input supply;
- /CE power-down;
- High-speed access time (10ns);
- Full automotive temperature range;
- Lead-free.

When /CE is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

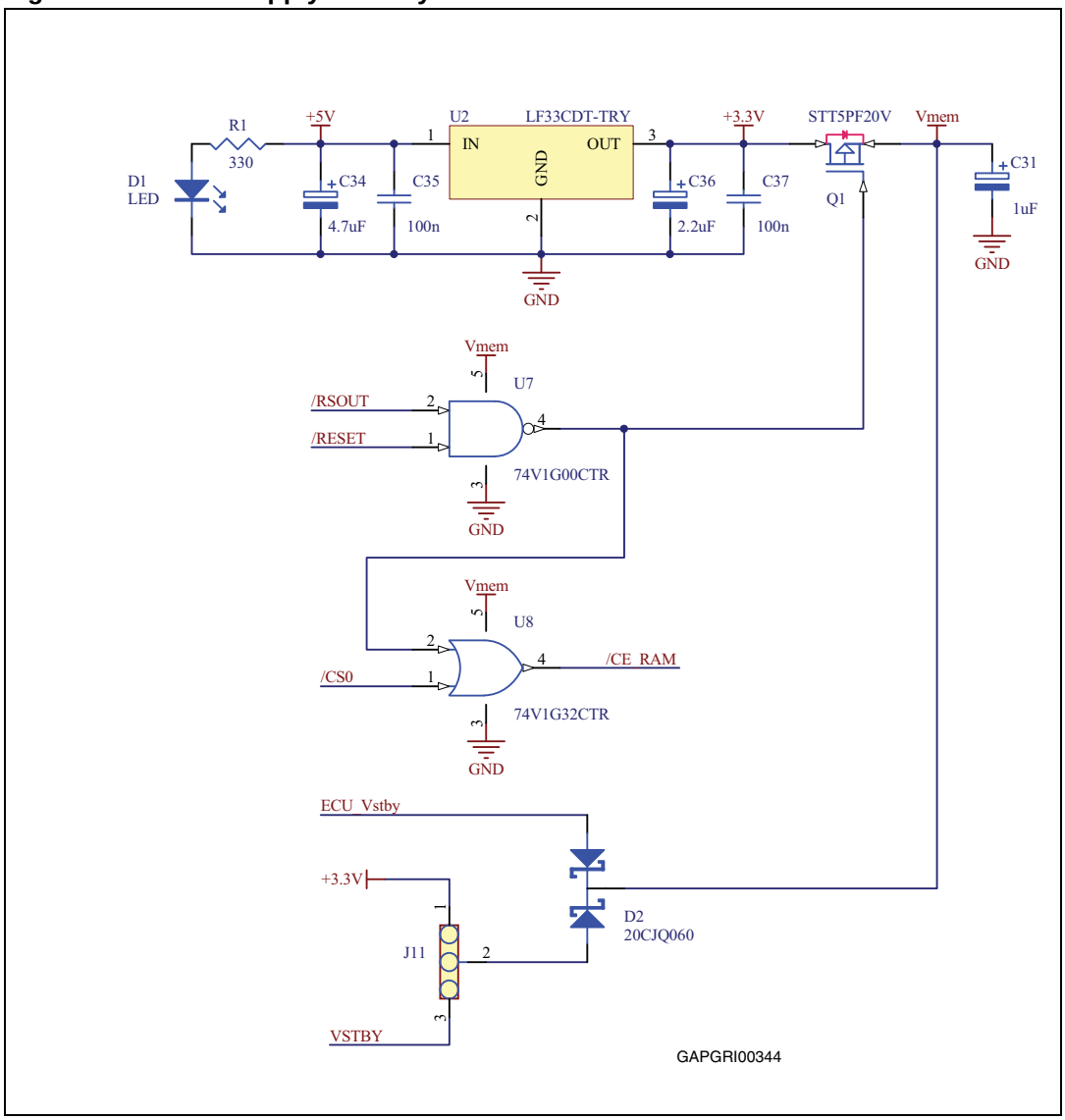
4.2 SRAM supply and data retention function

The circuitry in *Figure 6* has been implemented on the calibration board to protect the memory and to guarantee that the Working Page is valid after a power fail of the target application by putting the SRAM in standby powered.

The 3.3 V supply of the SRAM (Vmem) is gated by the RESET and RSTOUT signals of the SPC563M64xx.

The memory enable is driven via the SPC563M64xx chip select C_CS0 “and” the RESETs signals combination.

Figure 6. SRAM supply circuitry



The jumper J11 (see *Figure 6*) allows to select the standby operation of the SRAM.

The standby voltage can be selected between:

- SPC563M64xx Vstby pin: same standby voltage as the internal RAM;
- the 3.3V generated on the calibration board;
- ECU_Stby supplied by the calibration connector J9 (see *Figure 10*).

Table 4. J11 configuration of SRAM supply for retention mode

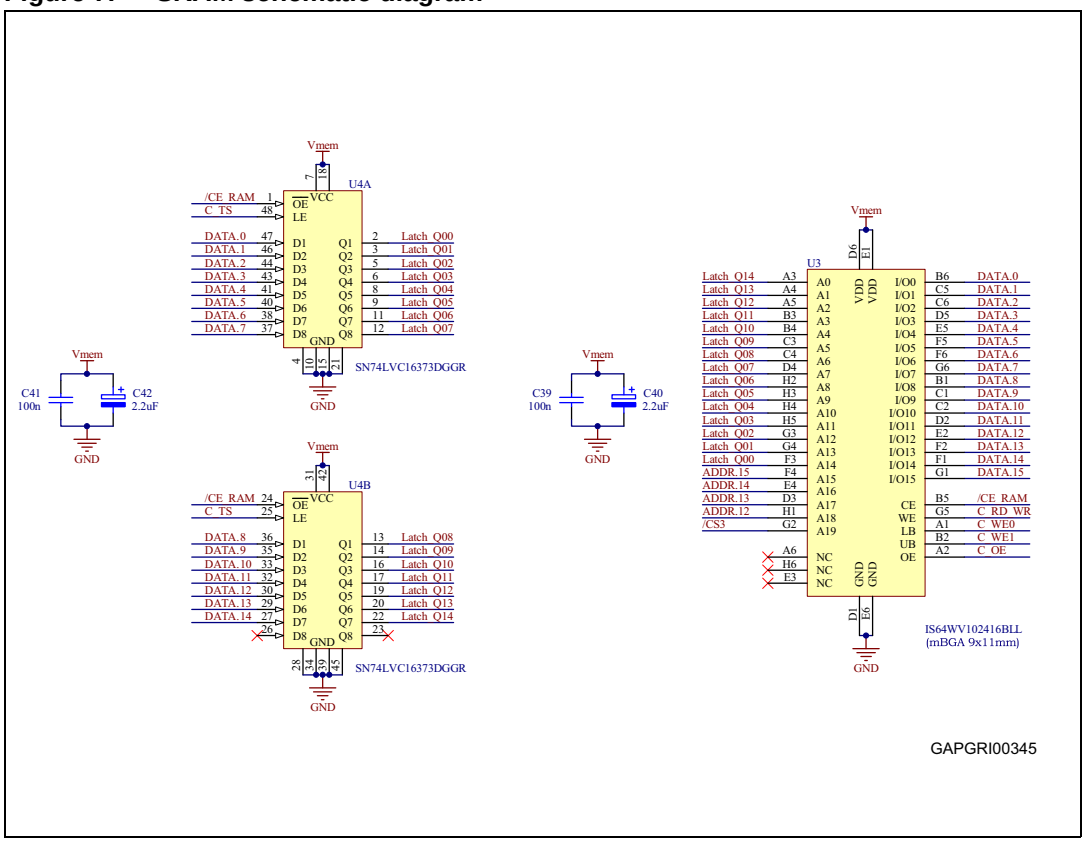
J11	SRAM standby supply source
all open	ECU_Stby: standby voltage on J9 calibration connector
1-2 closed	Upon the board +3.3V generated
2-3 closed	VSTBY input pin of the SPC563M64xx from the target application

4.3 Calibration bus interface

The calibration bus is made up of address bus, data bus, and bus control signals, and is used on the calibration board to access the upon board memory.

The calibration board supports a 16-bit de-mulitplexed calibration bus. This is derived from the multiplexed bus on the SPC563M64xx, where the majority of address lines are derived from the data lines (CAL_DATA on SPC563M64 device), by using an onboard external latch controlled by the C_TS signal. The ALE functionality of this signal indicates to the external latch when to capture the address signals

Figure 7. SRAM schematic diagram



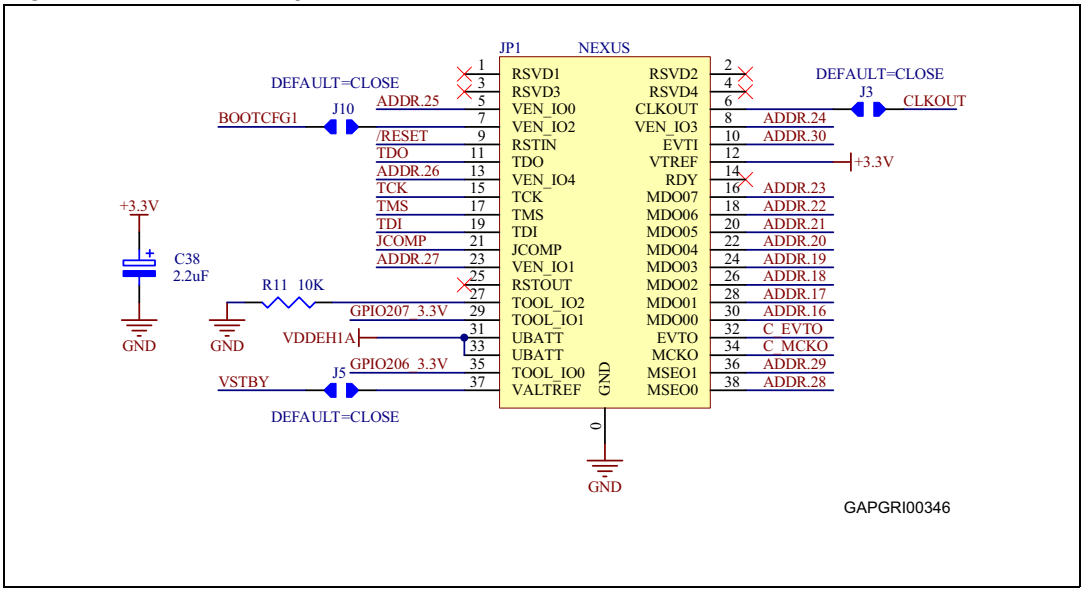
The *Section 9: Calibration software compatibility and configuration* shows the necessary software configuration of the SPC563M64xx calibration interface.

5 Development connector

The JTAG signals and Nexus functionality with 12 Message Data Out (MDO) signals are available on the JP1 development connector (Nexus connector).

A hardware control bit in the SPC563M64xx Nexus port controller, is used to control whether the added signals for full width trace port are routed to the MDO[4:11] signals, or the CAL_MDO[4:11] signals. This control bit is set by the cut trace J1 (default close) on the NEXUSCFG pin of the SPC563M64xx device, as on the calibration board the CAL_MDO[4:11] signals are routed to the JP1 development connector.

Figure 8. JP1 development connector



The option cut trace J3, J5 and J10 are listed on *Figure 5*.

Table 5. J3, J5 and J10 option cut traces

option name	Function	Value	Note
J3	CLKOUT	open	CLKOUT signal is disconnected to the Nexus JP1 connector
		close (default)	CLKOUT signal is connected to the Nexus JP1 connector
J5	VSTBY	open	VSTBY signal is disconnected to the Nexus JP1 connector
		close (default)	VSTBY signal is connected to the Nexus JP1 connector
J10	BOOTCFG1	open	BOOTCFG1 signal is disconnected to the Nexus JP1 connector
		close (default)	BOOTCFG1 signal is connected to the Nexus JP1 connector

Figure 6 shows the mapping of the development connector that provides Debug, Nexus trace and calibration signals. The port connector is an AMP 38 pin Mictor style.

Figure 9. AMP 38 Mictor

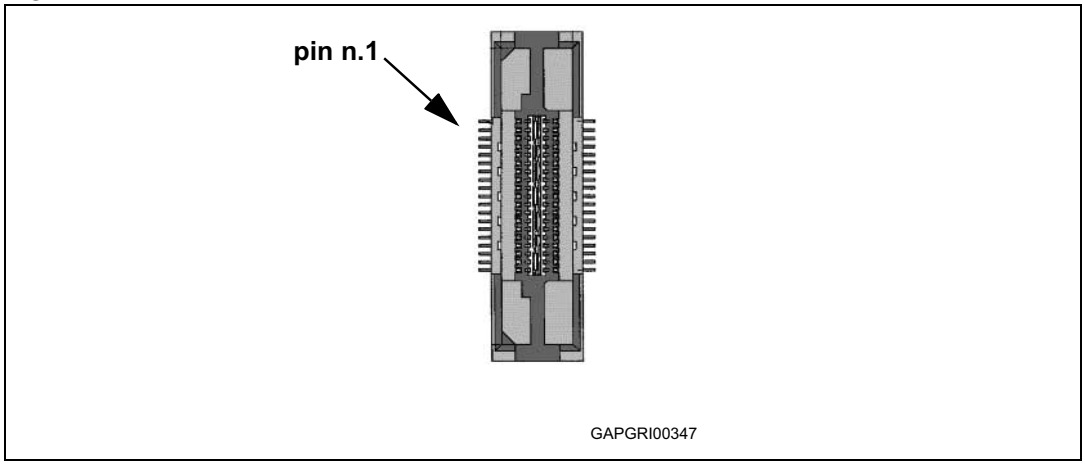


Table 6. Nexus signals on AMP 38 Mictor connector

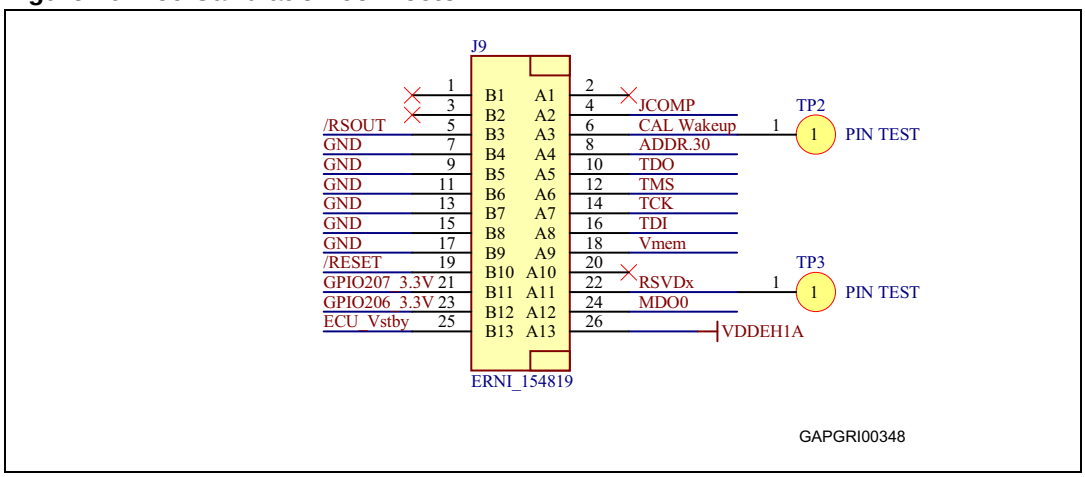
Pin	Description	Pin	Descriptio
1	nc	2	nc
3	nc	4	nc
5	C_MDO9	6	CLKOUT*
7	BOOTCFG1*	8	C_MDO8
9	/RESET	10	C_$\overline{\text{EVTI}}$
11	TDO	12	+3.3V
13	C_MDO10	14	RDY
15	TCK	16	C_MDO7
17	TMS	18	C_MDO6
19	TDI	20	C_MDO5
21	JCOMP	22	C_MDO4
23	C_MDO11	24	C_MDO3
25	nc	26	C_MDO2
27	10K pull down resistor	28	C_MDO1
29	TOOL_IO1	30	C_MDO0
31	VDDEH1A	32	C_$\overline{\text{EVTO}}$
33	VDDEH1A	34	C_MCKO
35	TOOL_IO0	36	C_$\overline{\text{MSEO1}}$
37	VSTBY*	38	C_$\overline{\text{MSEO0}}$

*) signal is connected via cut trace option

6 Calibration connector

The board is equipped with an ERNI connector to give a more robust solution in terms of physical connectivity for Calibration purpose.

Figure 10. J9 Calibration connector



The *Table 7* shows the mapping of the calibration connector that provides Debug and calibration signals. The port connector is an ERNI 154819 style.

Table 7. Nexus signals on AMP 38 Mictor connector

Pin	SPC563M64xx routing	standard function
B1	nc	nc
B2	nc	nc
B3	/RSOUT	/RSOUT
B4	GND	GND
B5	GND	GND
B6	GND	GND
B7	GND	GND
B8	GND	GND
B9	GND	GND
B10	/RESET	/RESET
B11	GPIO[207] (@3.3V)	GPIO Pins for startup handshake and triggering

Pin	SPC563M64xx routing	standard function
A1	nc	nc
A2	JCOMP	JTAG interface
A3	CAL Wakeup	12V output for Wakeup functionality
A4	C_$\overline{\text{EVTI}}$	JTAG interface
A5	TDO	JTAG interface
A6	TMS	JTAG interface
A7	TCK	JTAG interface
A8	TDI	JTAG interface
A9	Vmem	VDDSBRAM (Backup Voltage of ECU Standby RAM)
A10	nc	nc
A11	RSVDx	reserved Input, connect pin to a solder pad

Table 7. Nexus signals on AMP 38 Mictor connector (continued)

Pin	SPC563M64xx routing	standard function
B12	GPIO[207] (@3.3V)	GPIO Pins for startup handshake and triggering
B13	ECU_Vsby	VDDSBRAM Supply (Backup Voltage of ECU Standby RAM)

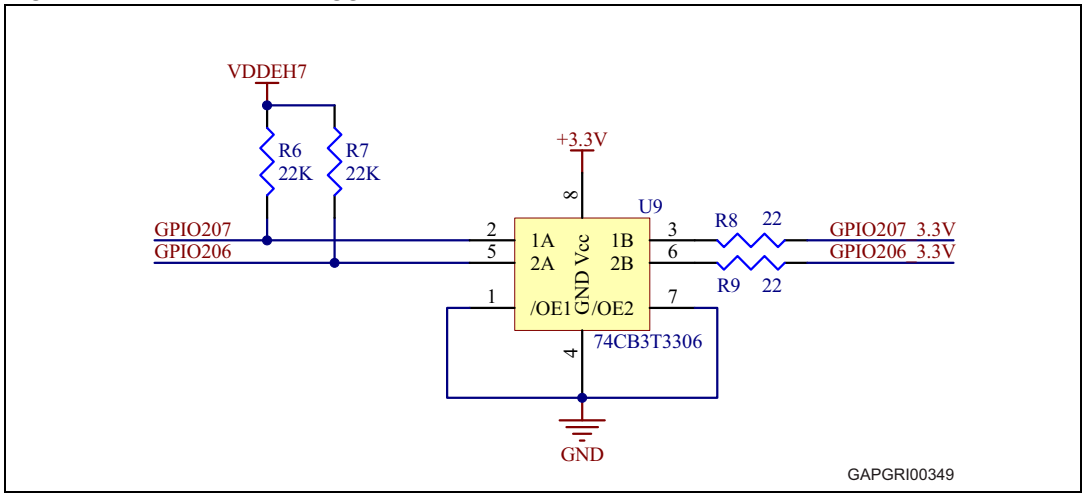
Pin	SPC563M64xx routing	standard function
A12	MDO 0	Detect that the PLL is locked
A13	+5V	VDDP Comparator Input (Supply of microcontroller Interface Pins)

7 Tool IO

The SPC563M64xx in CSP496 package provides 2 signals, GPIO[206] & GPIO[207], that are not available in the QFP144 standard production package. They can be used by the calibration tools to implement triggers and handshakes. On the calibration board, these signals are available on the JP1 development connector and J9 calibration connector.

By default GPIO[206] & GPIO[207] are powered by VDDEH at 5V. A level shifter (see *Figure 11*) does the translation between the 5v and the 3.3V. This is because the calibration tools operates at 3.3V that is the voltage level of the JTAG and Nexus interfaces.

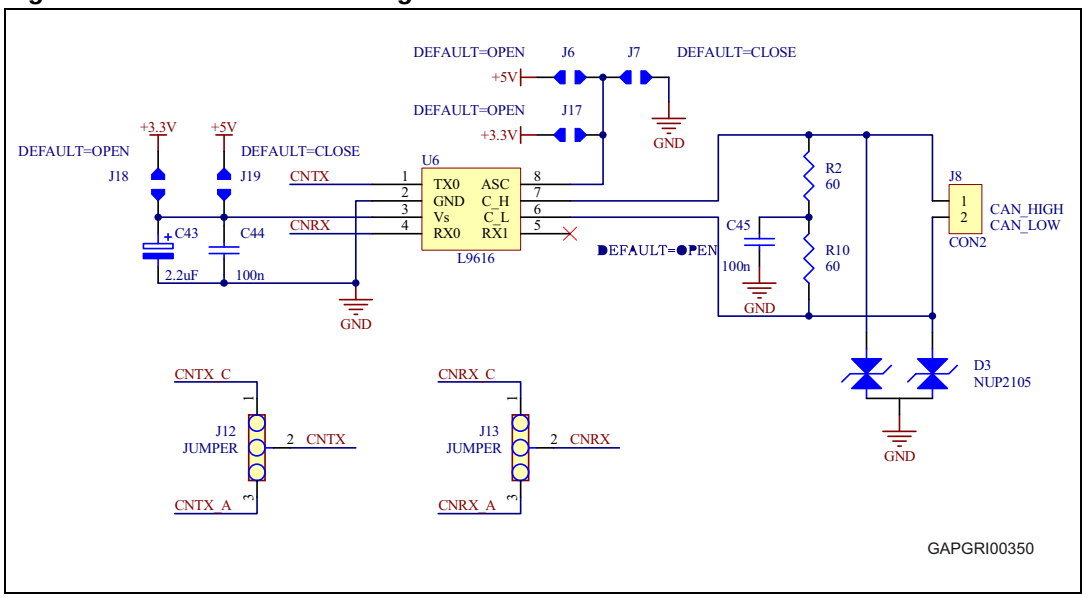
Figure 11. Calibration triggers TOOL_IO



8 CAN interface

The calibration board is equipped with one ST L9616 High-Speed Transceiver. It provides the Controller Area Network (CAN) communication interface through the SPC563M64xx CAN interface for calibration via CAN. This serial communication can reach speeds up to 1Mbps.

Figure 12. CAN schematic diagram



Two jumpers (J12 and J13), allow to select between the two FlexCAN interfaces of the SPC563M64xx mcu.

Table 8. J12, J13 FlexCAN interface selection

FlexCAN interface	J12 pin configuration TX select	J13 pin configuration RX select
FlexCAN A	2 - 3	2 - 3
FlexCAN C	2 - 1	2 - 1

The CAN channel is terminated with a 120 ohms resistor. Moreover, a protection circuitry has been designed to protect the CAN transceiver in high-speed and fault tolerant networks from ESD and other harmful transient voltage events (see *Figure 12*).

The L9616 CAN transceiver has an Adjustable Slope Control (ASC) feature that sets the slope speed using its ASC pin. This feature select the modes of operation:

- low speed (CAN baud rate up to 250kBaud)
- high speed (CAN baud rate from 250kBaud to 1000kBaud)

This pin can be put to high or to low by the cut trace options J6, J17 & J7 as described in *Table 9*.

Table 9. J6, J17 and J7 FlexCAN interface selection

J6 (or J17 if 3.3V)	J7	FlexCAN interface
closed	open	low speed operation (default) (CAN baud rate up to 250kBaud)
open	closed	high speed operation (CAN baud rate from 250kBaud to 1000kBaud)

The cut trace options J6, J17, J18 and J19 has been put in the design of this board to select the supply of the CAN transceiver between 5 V and 3.3 V. By this option is possible to replace the ST L9616 High-Speed Transceiver mounted on board by default, with a different transceiver that operates at 3.3 V.

Table 10. CAN transceiver operating voltage selection

CAN Transceiver	J6	J17	J18	J19
5V - ST L9616 High-Speed Transceiver	Adjustable Slope Control	open	open	close
3.3V - CAN transceiver	open	Adjustable Slope Control	close	open

Note: Refer to Section Appendix D: Options placement for layout options placement.

9 Calibration software compatibility and configuration

The calibration board uses standard production silicon packaged in the CSP (Chip Scale Package). Therefore, all production silicon features exist and are identical on the calibration board.

The required initialization code may be as simple as the configuration of the EBI and its related pins in the SIU, and it could be integrated into standard application software.

The calibration bus and the SIU can also be configured by an external tool connected to the debug port, removing the need of specific configuration functions in the application software.

9.1 Calibration bus sw configuration

A 16-bit calibration bus is implemented on the board. In multiplexed mode the CAL_DATA signals will output the address signals during the address phase by using an onboard external latch controlled by the CAL_TS signal. The CAL_ALE may be used to drive an external latch when an asynchronous memory is in use.

There are few steps to configure the SPC563M64xx Calibration Bus

- SIU PCR (Pad Configuration Register)
- SIU ECCR (External Clock Control Register)
- External Bus Interface (EBI)

9.1.1 Cal Bus PCR Settings

The SIU PCR registers used to configure the calibration bus are shown in the*Table 11* The table also shows the recommended PA field setting.

Table 11. Calibration bus signals configuration

signal name	SPC563M64xx mcu signal name	Function	PAG (1)	PCR PA field (2)	PCR (3)	Notes
Address/Data Bus (44)						
C_DATA[0:15]	CAL_DATA[0:15]	Calibration data bus	-	-	341	
C_ADDR[12:15]	CAL_ADDR[12:15]	Calibration address bus	-	-	340	
C_ADDR[16:31]	CAL_ADDR[16:31]	Calibration address bus	-	-	345	
C_CS[0]	CAL_CS[0]	Calibration chip select	-	-	336	
C_CS[1]	Not Connected					
C_CS[2]	CAL_CS[2] CAL_ADDR[10]	Calibration chip select Calibration address bus	P A	1 0	338	

Table 11. Calibration bus signals configuration (continued)

signal name	SPC563M64xx mcu signal name	Function	PAG (1)	PCR PA field (2)	PCR (3)	Notes
C_CS[3]	CAL_CS[3] CAL_ADDR[11]	Calibration chip select Calibration address bus	P A	1 0	339	
C_OE	CAL_OE	Calibration Output enable	-	-	342	
C_RD_WR	CAL_RD_WR	Calibration Read/write	-	-	342	
C_WE[0:1]	CAL_WE[0:1]	Calibration write/byte enable	-	-	342	
C_TS	CAL_TS CAL_ALE	Calibration transfer start Address Latch enable	P A	1 0	343	
Clock Synthesizer (1)						
C_CLKOUT	CLKOUT	System clock output	P	01	229	Clock output signal from MCU

Note: 1 The P/A/G column indicates the position a signal occupies in the muxing order for a pin: Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 -0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.

2 The Pad Configuration Register (PCR) PA field is used by software to select pin function.

3 Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is "SIU_PCR" suffixed by the PCR number.

9.1.2 Cal Bus ECCR Settings

The SIU ECCR registers used to control the timing relationship between the system clock and the external clock CLKOUT.

The external bus clock (CLKOUT) divider can be programmed to divide the system clock by one, two or four based on the settings of the EBDF bit field.

Table 12. EBDF field definition

Register	EBDF field	External Bus Division Factor
SIU_ECCR	00	1
	01	2
	10	reserved
	11	4

9.1.3 Cal Bus EBI Settings

For using the calibration bus with an external memory the user must configure the bus for multiplexed operation. These settings are located in two registers:

- EBI Module Configuration Register (EBI_MCR)
- EBI Calibration Base Register (EBI_CAL_BRx)
- EBI Calibration Option Register (EBI_CAL_ORx)

The EBI Module Configuration Register contains bits which configure various attributes associated with EBI operation. In the EBI_MCR register, the D16_31, AD_MUX and DBM fields need to be configured.

Table 13. EBI_MCR register setting

bit field	Name	Description	value
29	D16_31 Data Bus 16_31 Select	The D16_31 bit controls whether the EBI uses the DATA[0:15] or DATA[16:31] signals, when in 16-bit Data Bus Mode (DBM=1) or for chip-select accesses to a 16-bit port (PS=1). 1 = DATA[16:31] signals are used for 16-bit port accesses 0 = DATA[0:15] signals are used for 16-bit port accesses	0b0
30	AD_MUX Address on Data Bus Multiplexing Mode	The AD_MUX bit controls whether non-chip-select accesses have the address driven on (or sampled from for external master transfers) the data bus in the address phase of a cycle. 1 = Address on Data Multiplexing Mode is used for non-CS accesses. 0 = Only Data on data pins for non-CS accesses.	0b1
31	DBM Data Bus Mode	The DBM bit controls whether the EBI is in 32-bit or 16-bit Data Bus Mode. 1 = 16-bit Data Bus Mode is used 0 = 32-bit Data Bus Mode is used	0b1

In the EBI_CAL_BRx register there are few fields that need to be configured, these are detailed in the *Table 14* .

Table 14. EBI_CAL_BRx register setting

bit field	Name	Description	value
0-16	BA Base address	These bits are compared to the corresponding unmasked address signals among ADDR[0:16] of the internal address bus to determine if a memory bank controlled by the memory controller is being accessed by an internal bus master Note: An MCU may have some of the upper bits of the BA field tied to a fixed value internally in order to restrict the address range of the EBI for that MCU. Refer to the device-specific documentation to see which bits are tied off, if any, for a particular MCU. Tied-off bits can be read but not written. These bits are ignored by the EBI during the chip-select address comparison. However, the internal bridge of the MCU most likely requires that the chipselect banks be located in memory regions corresponding to the fixed values chosen	-
20	PS Port Size	The PS bit determines the data bus width of transactions to this chip-select bank. Note: In the case where the DBM bit in EBI_MCR is set for 16-bit Data Bus Mode, the PS bit value is ignored and is always treated as a '1' (16-bit port). 1 = 16-bit port 0 = 32-bit port	0b1
24	AD_MUX Address on Data Bus Multiplexing	The AD_MUX bit controls whether accesses for this chip select have the address driven on the data bus in the address phase of a cycle 1 = Address on Data Multiplexing Mode is enabled for this chip select. 0 = Address on Data Multiplexing Mode is disabled for this chip select.	0b1
26	WEBS Write Enable / Byte Select	This bit controls the functionality of the WE[0:3]/BE[0:3] signals. 1 = The WE[0:3]/BE[0:3] signals function as BE[0:3] 0 = The WE[0:3]/BE[0:3] signals function as WE[0:3]	0b1
30	BI Burst Inhibit	This bit determines whether or not burst read accesses are allowed for this chipselect bank. The BI bit is ignored (treated as 1) for chip-select accesses with external TA (SETA=1). 1 = Disable burst accesses for this bank. This is the default value out of reset (or when SETA=1). 0 = Enable burst accesses for this bank]	0b1

Table 14. EBI_CAL_BRx register setting

bit field	Name	Description	value
31	V Valid bit	The user writes this bit to indicate that the contents of this Base Register and Option Register pair are valid. The appropriate CS signal does not assert unless the corresponding V-bit is set. 1: This bank is valid 0: This bank is not valid	0b1

The EBI Option Registers are used to define the address mask and other attributes for the corresponding chip select.The SCY field of the EBI_CAL_BOx register is detailed in the *Table 15*.

Table 15. EBI_CAL_BOx register setting

bit field	Name	Description	value
0-16	AM Address Mask	This field allows masking of any corresponding bits in the associated Base Register. Masking the address independently allows external devices of different size address ranges to be used. Any clear bit masks the corresponding address bit. Any set bit causes the corresponding address bit to be used in comparison with the address pins. Address mask bits can be set or cleared in any order in the field, allowing a resource to reside in more than one area of the address map. This field can be read or written at any time.	-
24-27	SCY Cycle length in clocks	This field represents the number of wait states (external cycles) inserted after the address phase in the single transfer case, or in the first beat of a burst, when the memory controller handles the external memory access. Values range from 0 to 15 and its depends on the RAM connected on top board. This is the main parameter for determining the length of the cycle. These bits are ignored when SETA=1. The total cycle length for the first beat (including the TS cycle) = (2+SCY) external clock cycles.	-
29-30	BSCY Burst beats length in clocks	This field determines the number of wait states (external cycles) inserted in all burst beats except the first, when the memory controller starts handling the external memory access and thus is using SCY[0:3] to determine the length of the first beat. These bits are ignored when SETA=1. The total memory access length for each beat is (1 + BSCY) external clock cycles. The total cycle length (including the TS cycle) = (2+SCY) + (#beats(h)-1) * (BSCY+1).	-

9.2 Example Configuration CODE

The following code is used to configure the calibration bus for 16bit de-multiplexed mode.

```
//-------------------------------------------------
// SIU PCR (Pad Configuration Register) setup
// (Cal BUS bommon drive strength = 20pF, DSC = 0b01)
//-------------------------------------------------


SIU.PCR[336].R = 0x0040;//CAL_CS[0]DSC=20pF (0b01)

SIU.PCR[338].R = 0x0440;//CAL_CS[2] (PA=0b1),DSC=20pF (0b01)

SIU.PCR[339].R = 0x0040;//CAL_ADDR[11] (PA=0b0), DSC=20pF (0b01)

SIU.PCR[340].R = 0x0040;//CAL_ADDR[12..15], DSC=20pF (0b01)

SIU.PCR[345].R = 0x0040;//CAL_ADDR[16..30], DSC=20pF (0b01)

SIU.PCR[341].R = 0x0040;//CAL_DATA[0..15], DSC=20pF (0b01)

SIU.PCR[342].R = 0x0040;//CAL_RD/WR, CAL_WE[0-1], CAL_OE, DSC=20pF
(0b01)

SIU.PCR[343].R = 0x0040;//CAL_ALE, DSC=20pF (0b01)


//-------------------------------------------------
// SIU ECCR (External Clock Control Register) setup
//-------------------------------------------------

SIU.ECCR.R = 0x1000//External Bus Division Factor = 1 (EBDF=0b00)


//-------------------------------------------------
// EBI Registers setup
//-------------------------------------------------

//-----------------------------------------------------------------
// EBI MCR setup for 16-bit bus configuration:
//
// EARP = 01 (Equal priority);
// D16_31 = 0 (DATA[0:15] signals are used for 16-bit port accesses);
// AD_MUX = 1 (Addr on Data Multiplexing Mode is used for non-CS acc.);
// DBM = 0 (32-bit Data Bus Mode is used);

EBI.MCR.R = 0x802;


//-------------------------------------------------------
// EBI Base Register setup for 16-bit bus configuration:
//
// Base Address = 0x20000000;
// PS = 1 (16-bits port size)
// AD_MUX = 1 (Address on Data Multiplexing Mode is enabled for this chip select);
// WEBS = 1 (Use BE function);
// BI = 1 (Disable burst accesses for this bank);
// V = 1 (Valid CS Bank)

EBI.CAL_CS[0].BR.R = 0x200008A3;
```

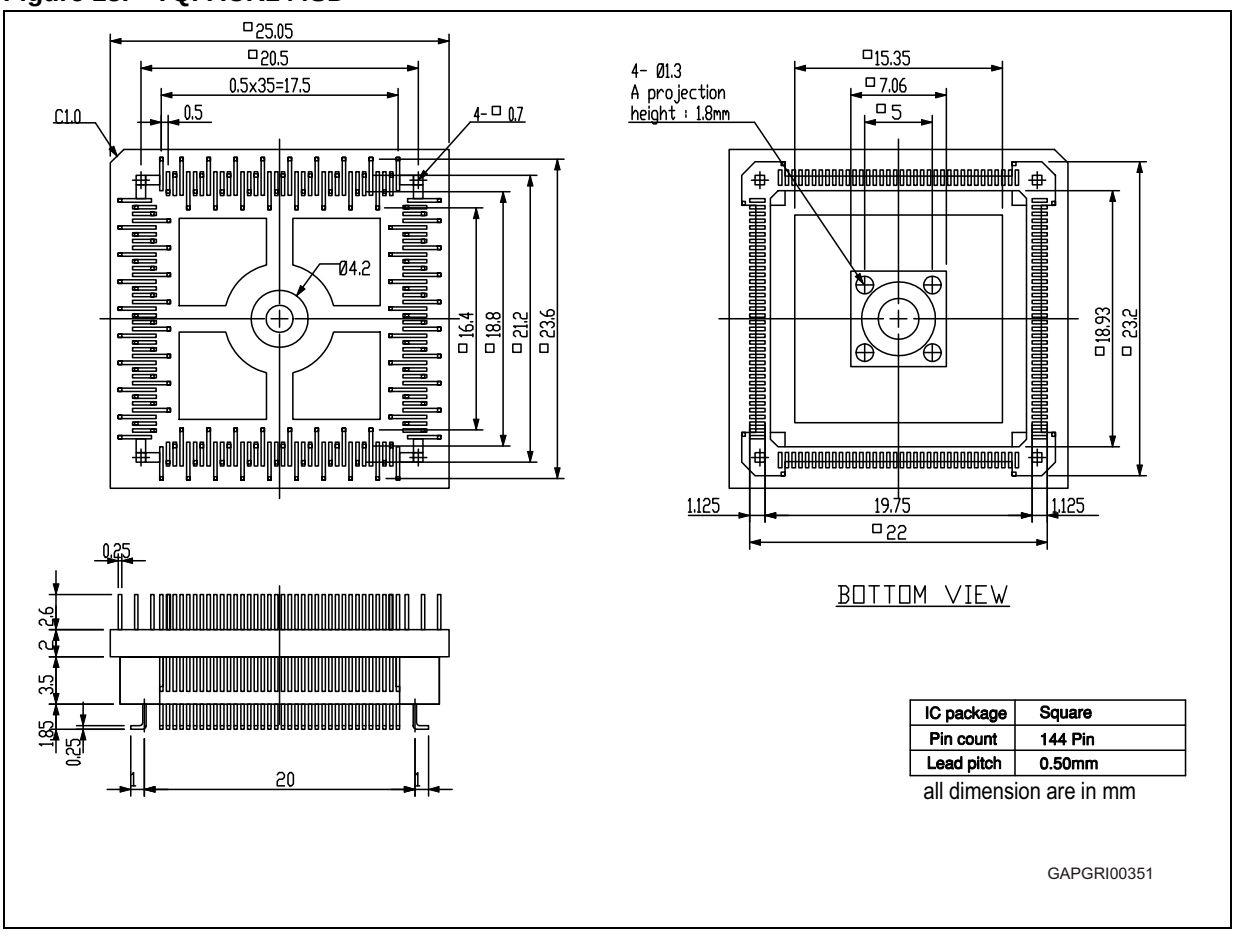
```
//----------------------------------------
// EBI Option Register setup:
//
// Address mask = 0xefe00000;
// Wait state = 0 (set 0 wait states);

EBI.CAL_CS[0].OR.R = 0xffe00000;
```

Appendix A Calibration base footprints

SPC563M64CAL144 (rev.B) calibration board had footprint compatible with QFP144 production package version of SPC563M64xx devices, ensuring that they can be fitted to an application PCB that has been designed to accept standard QFP144 packaged SPC563M64xx devices.

Bases can be supplied with solder footprints, to allow direct and permanent soldered connection to an application PCB, or with pin adapter connectors fitted, allowing connection and removal from an application PCB that is fitted with a compatible receiver socket.

Figure 13. TQPACK144SD



Appendix B Mechanical constrains

Figure 14. Top and side view drawing

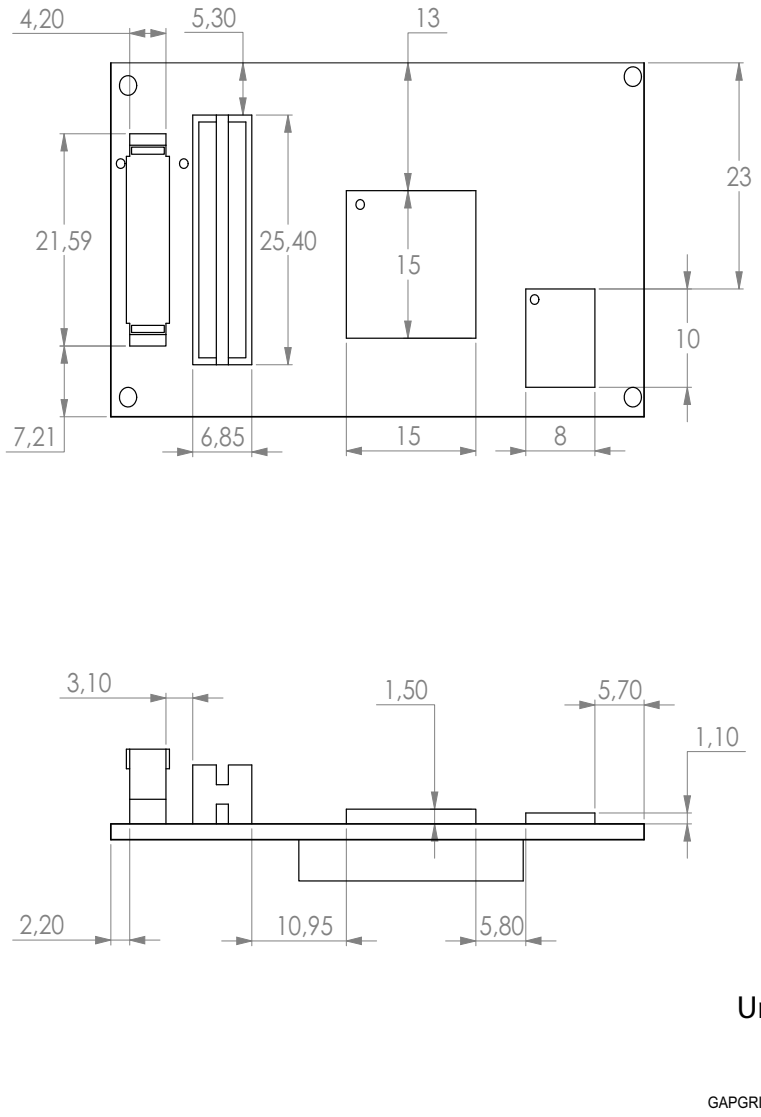


Figure 15. Side and bottom view drawing

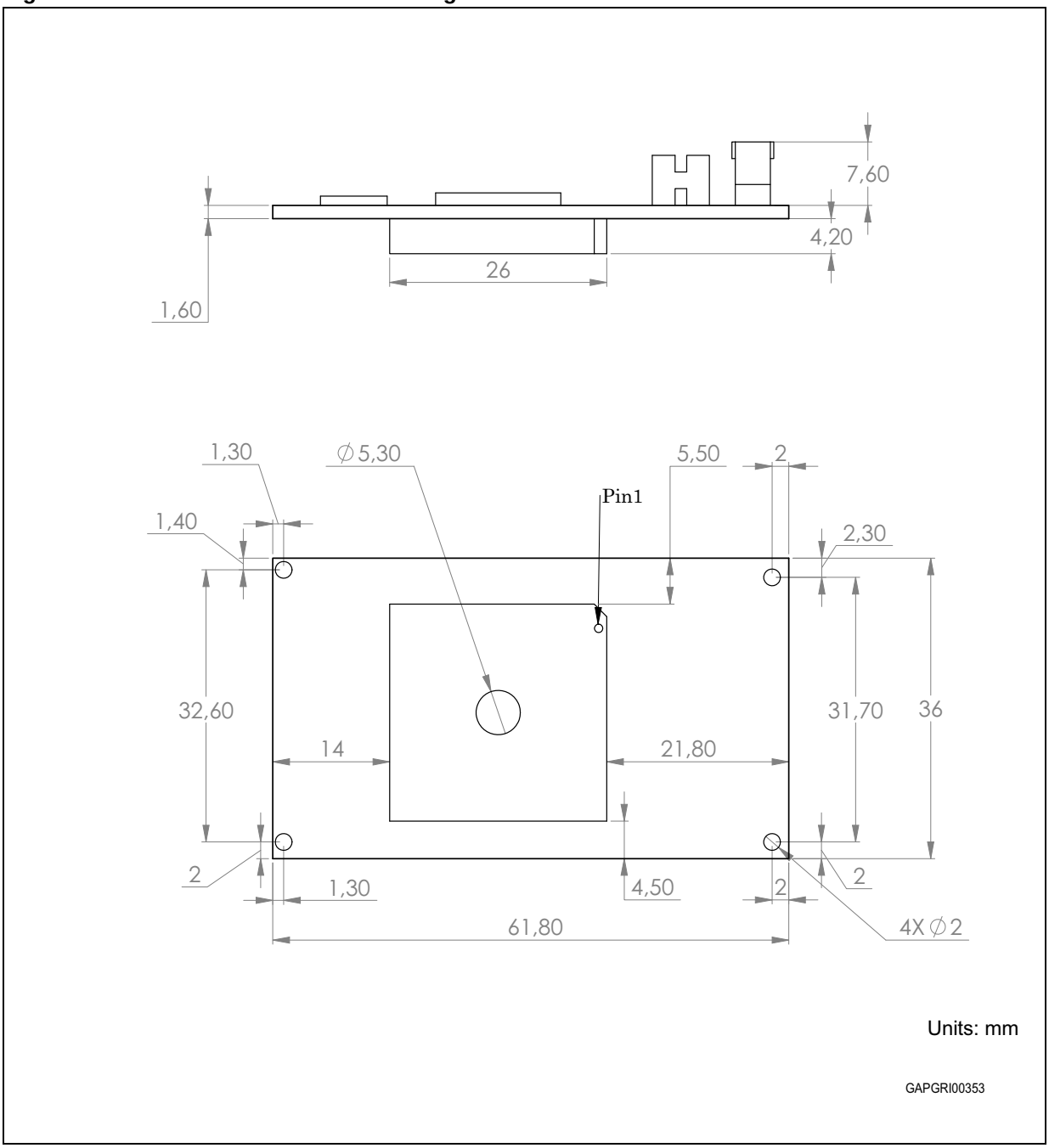
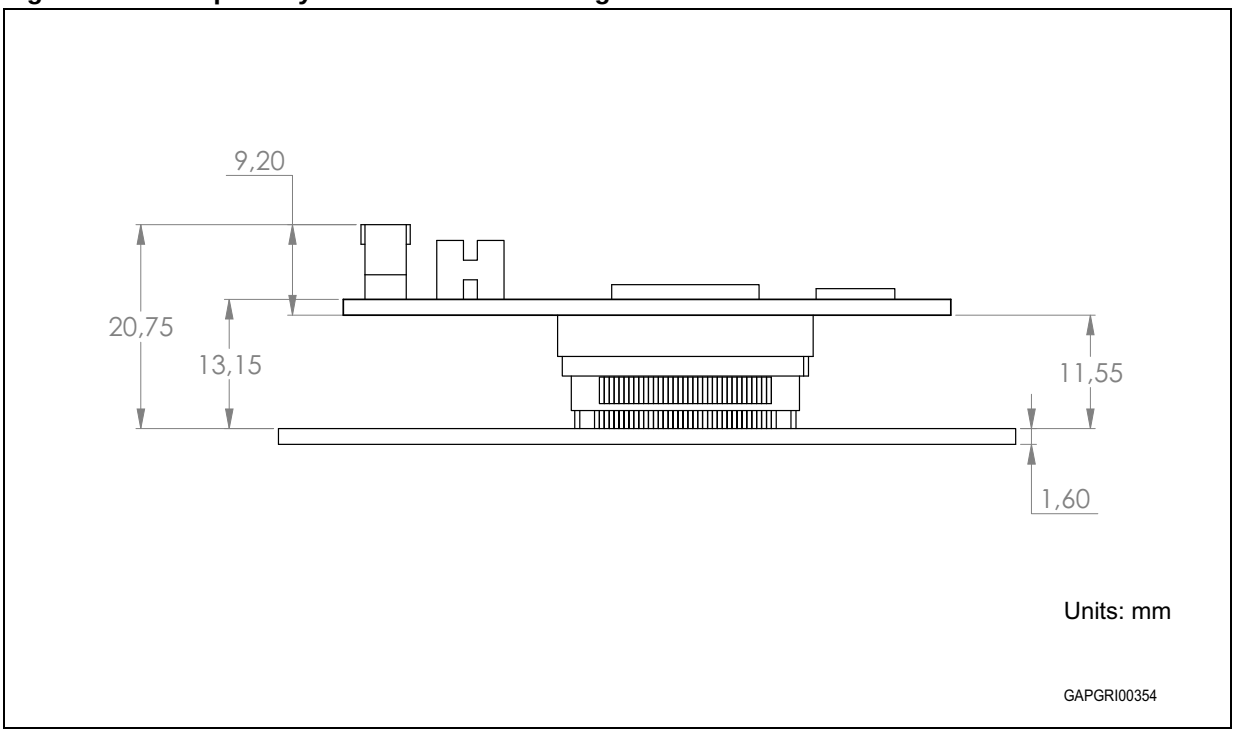


Figure 16. Complete system side view drawing



Appendix C Schematic

Figure 17. SPC563M64xx in CSP package schematic

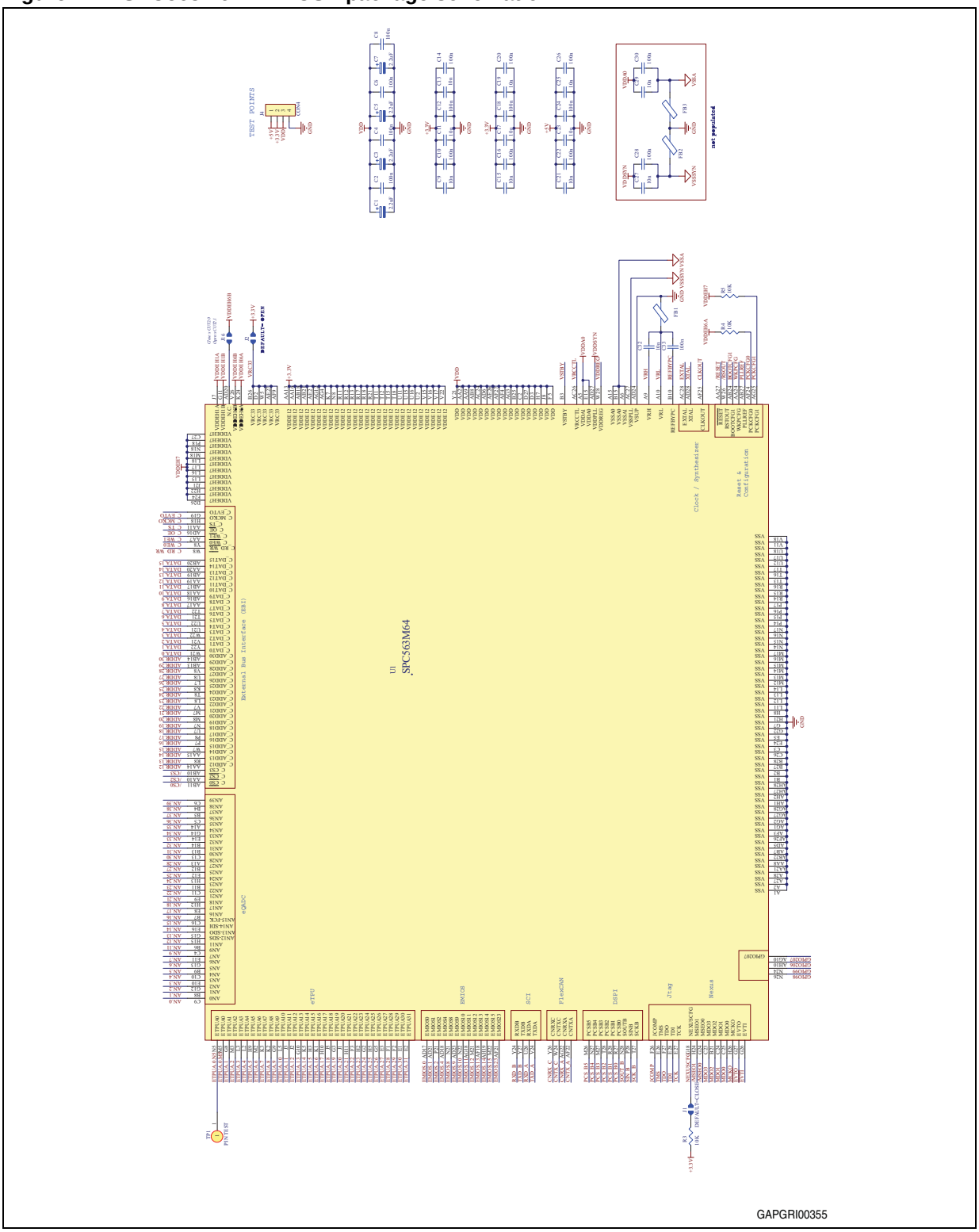
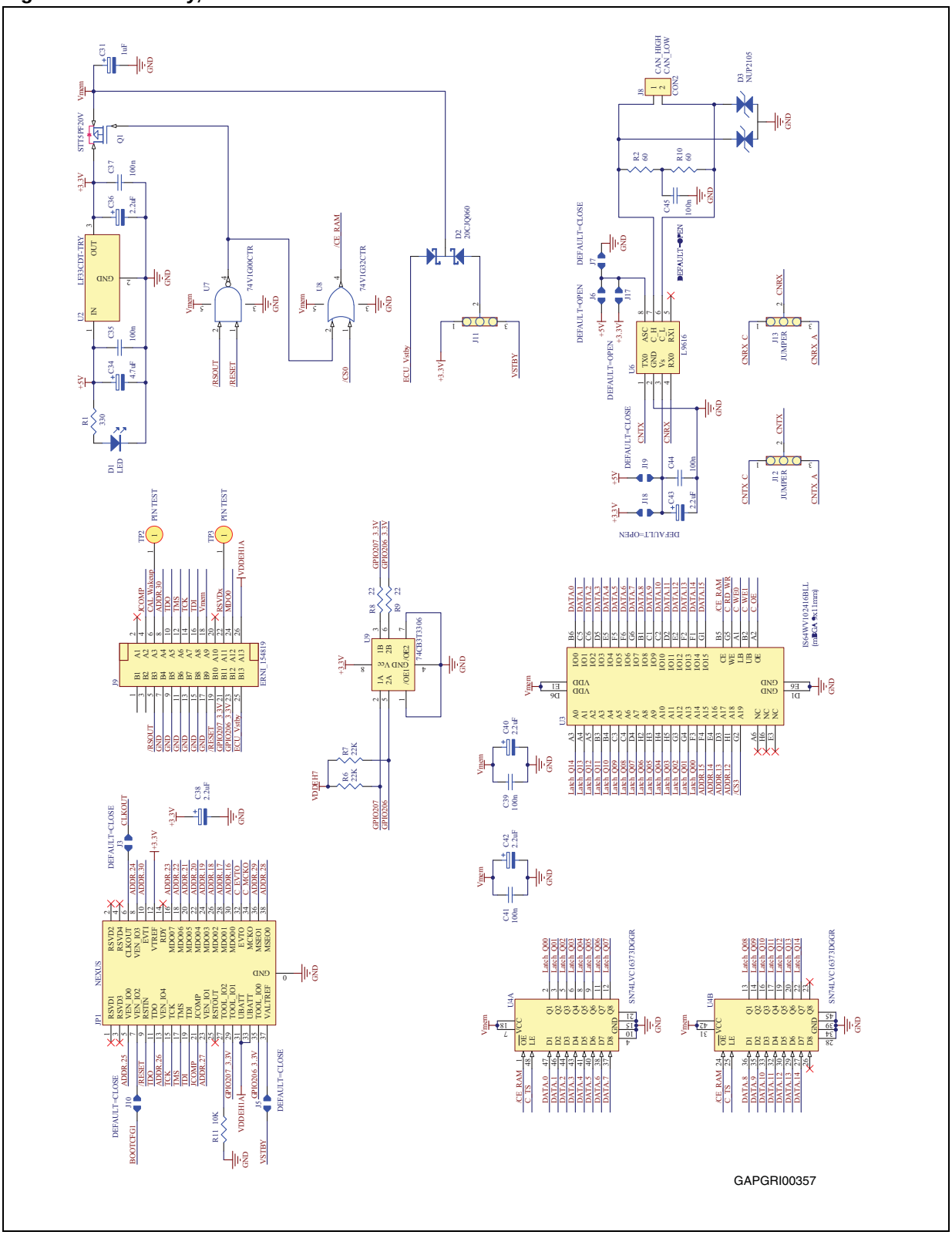


Figure 18. Polypod-TQ144 connector schematic

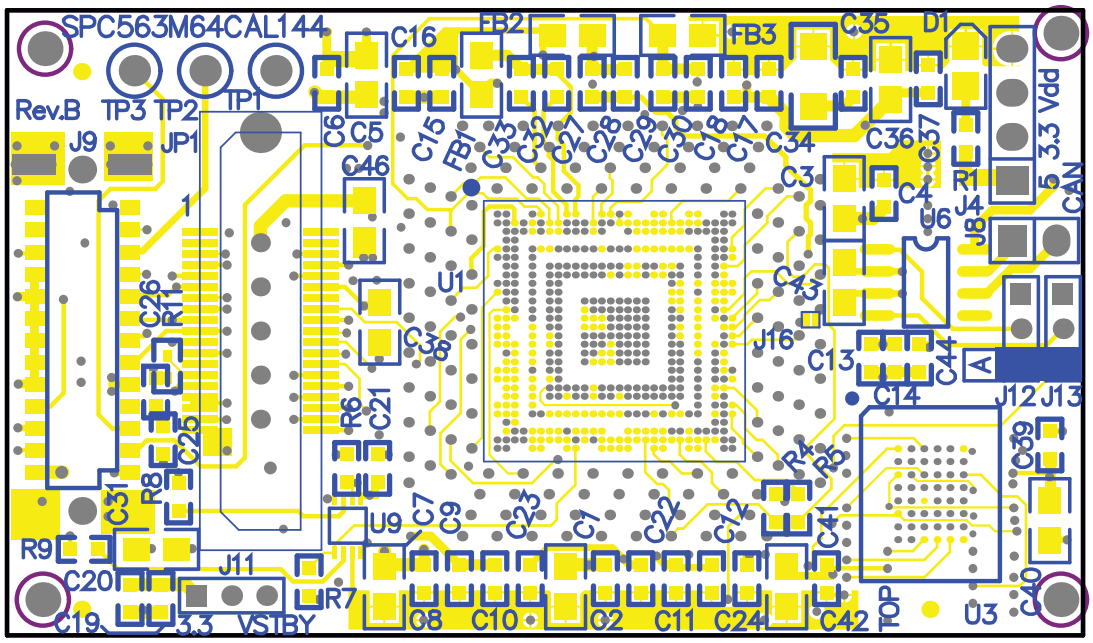
Figure 19. Memory, CAN and connectors schematic



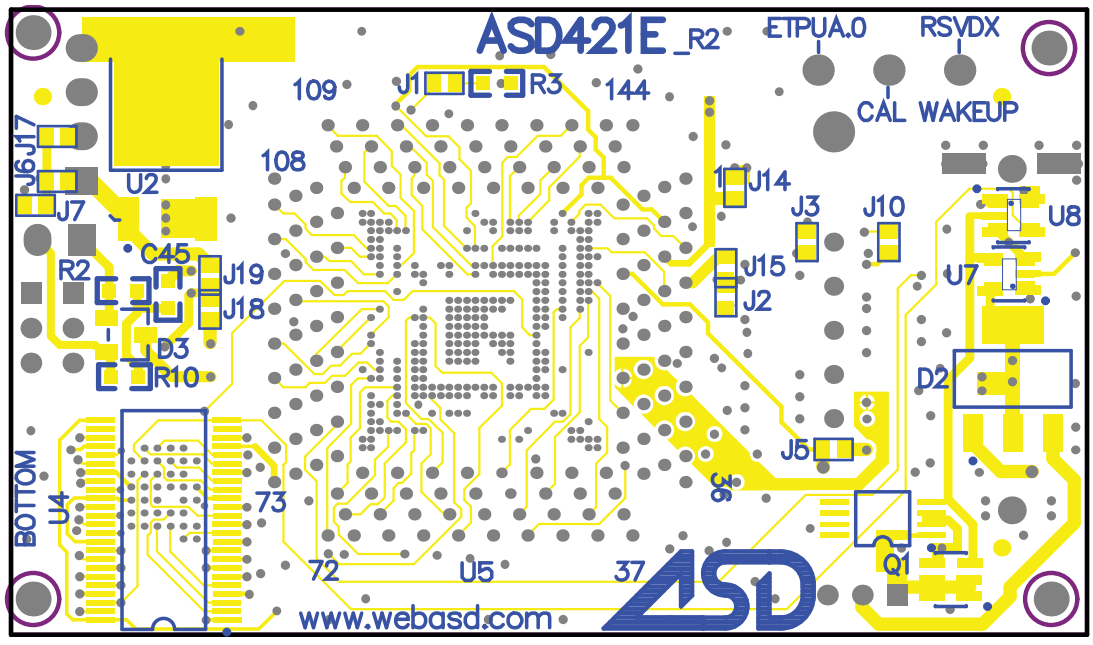
Appendix D Options placement

Figure 20. Options placement

TOP view



Bottom view



GAPGBI00358

Revision history

Table 16. Document revision history

Date	Revision	Changes
18-Jan-2013	1	Initial release.
13-Feb-2013	2	Modified *Figure 14*.
17-Sep-2013	3	Updated Disclaimer.

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