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TN1176
Technical note

Migrating from STM32L15xx6/8/B to STM32L15xx6/8/B-A and from STM32L100x6/8/B to STM32L100x6/8/B-A

Introduction

To ease the development of STM32 microcontroller applications, it is important to be able to smoothly replace one microcontroller type with another from the same product family. The purpose of this technical note is to help the users with the migration from an existing STM32L15xx6/8/B device to an STM32L15xx6/8/B-A device and from an existing STM32L100x6/8/B device to an STM32L100x6/8/B-A. This document includes the relevant information for the users.

Prior to migrating an application, the users need to analyze the hardware migration, the peripheral migration and the firmware migration. To best understand the information included in this technical note, the user should be familiar with the STM32L1 microcontroller family.

For additional information, please refer to the STM32L100xx, STM32L151xx, STM32L152xx and STM32L162xx advanced ARM®-based 32-bit MCUs reference manual RM0038 in which STM32L15xx6/8/B is ‘Cat.1’ device, STM32L15xx6/8/B-A is ‘Cat.2’ device, STM32L100x6/8/B is ‘Cat.1’ device, STM32L100x6/8/B-A is ‘Cat.2’ device and to the STM32L15xx6/8/B-A, STM32L15xx6/8/B, STM32L100x6/8/B-A, STM32L100x6/8/B datasheets. Documents are available for download from the company website at *www.st.com/stm32*.

Table 1 lists the STM32 microcontrollers concerned by this technical note.

Table 1. Applicable products

Type	Reference products
Microcontrollers	STM32L100C6, STM32L100R8, STM32L100RB, STM32L100C6-A, STM32L100R8-A, STM32L100RB-A, STM32L151C6, STM32L151C8, STM32L151CB, STM32L151C6-A, STM32L151C8-A, STM32L151CB-A, STM32L151R6, STM32L151R8, STM32L151RB, STM32L151R6-A, STM32L151R8-A, STM32L151RB-A, STM32L151V8, STM32L151VB, STM32L151V8-A, STM32L151VB-A, STM32L152C6, STM32L152C8, STM32L152CB, STM32L152C6-A, STM32L152C8-A, STM32L152CB-A, STM32L152R6, STM32L152R8, STM32L152RB, STM32L152R6-A, STM32L152R8-A, STM32L152RB-A, STM32L152V8, STM32L152VB, STM32L152V8-A, STM32L152VB-A,

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1 Codification/packages changes

Table 2 presents the list of references, part numbers and packages for the STM32L15xx6/8/B and STM32L15xx6/8/B-A products.

Table 2. STM32L15x device summary

Device description	Reference	Part number	Package
Up to: STM32L15x - 128KB Flash 16KB RAM	STM32L15xx6/8/B	STM32L15xCBxx STM32L15xC8xx STM32L15xC6xx STM32L15xRBxx STM32L15xR8xx STM32L15xR6xx STM32L15xVBxx STM32L15xV8xx	LQFP100, LQFP64, LQFP48, UFBGA100, TFBGA64, UFQFPN48
Up to: STM32L15x - 128KB Flash 32KB RAM	STM32L15xx6/8/B-A	STM32L15xCBxxA STM32L15xC8xxA STM32L15xC6xxA STM32L15xRBxxA STM32L15xR8xxA STM32L15xR6xxA STM32L15xVBxxA STM32L15xV8xxA	LQFP100, LQFP64, LQFP48, UFBGA100, TFBGA64, UFQFPN48

Table 3 presents the list of references, part numbers and packages for the STM32L100x6/8/B and STM32L100x6/8/B-A products.

Table 3. STM32L100 device summary

Device description	Reference	Part number	Packages
Up to: STM32L100 - 128KB Flash 10KB RAM	STM32L100x6/8/B	STM32L100CBxx STM32L100RBxx	LQFP64, UFQFPN48
Up to: STM32L100 - 128KB Flash 16KB RAM	STM32L100x6/8/B-A	STM32L100CBxxA STM32L100RBxxA	LQFP64, UFQFPN48

The changes and similarities in the codification/packages in STM32L15xx6/8/B-A versus STM32L15xx6/8/B and STM32L100x6/8/B-A versus STM32L100x6/8/B are the following:

- The related reference number ends with -A,
- The packages are the same,
- The pinout is the same.

2 Hardware migration

The STM32L15xx6/8/B and STM32L15xx6/8/B-A devices are pin-to-pin compatible. All peripherals share the same pins. Both devices are produced in the same packages.

The STM32L100x6/8/B and STM32L100x6/8/B-A devices are pin-to-pin compatible. All peripherals share the same pins. Both devices are produced in the same packages.

The transition from the STM32L15xx6/8/B device to the STM32L15xx6/8/B-A device and the transition from the STM32L100x6/8/B device to the STM32L100x6/8/B-A device is therefore very simple and device can be replaced without any hardware changes on the application PCB.

3 Peripheral migration

Table 4 and *Table 5* list the main product peripherals and system features for both product pairs. The common peripherals are supported with the dedicated firmware library without any modification. The users can change the instance and all the related features (clock configuration, pin configuration, interrupt/DMA request).

Peripherals such as Touch sensing, Backup registers are different in the STM32L15xx6/8/B device and must be updated by software to benefit from the latest enhancements and correct functionality of STM32L15xx6/8/B-A device.

The extended peripherals such as: RTC, LCD rail decoupling, PCROP (Proprietary code read out protection), clock (CSS on LSE) are fully backward compatible with no need to firmware update.

The main peripherals changes are described in *Section 3.1: Main peripheral/system changes*. The changes which are also needed in the development tools configuration are described in *Section 4: Development tool adaptations*.

Table 4 presents the differences between STM32L15xx6/8/B and STM32L15xx6/8/B-A devices regarding the peripherals and system differences, as well as the impact to needed software changes. The differences are highlighted in gray.

Table 4. STM32L15xx6/8/B and STM32L15xx6/8/B-A device difference summary(1)

Function	STM32L15xx6/8/B	STM32L15xx6/8/B-A	Behavior / impact to software
Core @ 32MHz	ARM Cortex™-M3	ARM Cortex™-M3	
Max DMIPS/MHz	1.25	1.25	
Flash [KB]	up to 128	up to 128	
RAM [KB]	up to 16	up to 32	Enhancement. the application can use larger RAM memory space.
EEPROM [KB]	4	4	
Backup registers [B]	80	20	Software can store only up to 20 bytes into backup registers. See STM32L15xx6/8/B-A errata sheet for details.
Flash interface [bits]	64/32	64/32	
Bootloader	USART1/2	USART1/2	
DMA / channels	1 / 7ch	1 / 7ch	
USART	3	3	
SPI / I2S	2 / 0	2 / 0	
I2C	2	2	
USB 2.0	1 x FS	1 x FS	
LCD [seg x com]	8 x 40	8 x 40	

Table 4. STM32L15xx6/8/B and STM32L15xx6/8/B-A device difference summary(1) (continued)

Function	STM32L15xx6/8/B	STM32L15xx6/8/B-A	Behavior / impact to software
LCD rails decoupling	NO	YES	Better LCD contrast for larger displays (if used external LCD rails decoupling capacitors). If not used no software change is required.
TIMER [32-bit/16-bit/Lite]	0/6/2	0/6/2	
IWDG/WWDG	1/1	1/1	
Clock	HSI/HSE/LSI/LSE CSS on HSE	HSI/HSE/LSI/LSE CSS on HSE/LSE	Extension of CSS to LSE. Backward compatible. If not used then no software change is needed.
HSI/HSI clock trimming	+/- 1%	+/- 1%	
RTC version	RTC V1.0	RTC V2.0	New RTC as in whole L1 family - with subsecond resolution. If not used then no software change is needed.
DAC	2	2	
ADC (total / fast channels)	1 (24 / 6)	1 (24 / 6)	
Comparator	2	2	
Touch sensing [channels]	20	20	The touch sensing interface has been modified - no different features but new SW library is needed to handle the new device (download on www.st.com/stm32).
Temperature sensor	YES	YES	
Internal voltage reference	YES	YES	
Unique ID	YES	YES	
MCO	YES	YES	
PCROP	NO	YES	New memory protection feature implemented: Proprietary code read out protection (only its execution is allowed). If not used then no software change is needed (only added extension of existing protections).

1. The grayed cells highlight the differences between the device sets.

Table 5 presents the differences between STM32L100x6/8/B and STM32L100x6/8/B-A devices regarding the peripherals and system differences, as well as the impact to needed software changes. The differences are highlighted in gray.

Table 5. STM32L100x6/8/B-A and STM32L100x6/8/B device difference summary(1)

Function	STM32L100x6/8/B	STM32L100x6/8/B-A	Behavior / impact to software
Core @ 32MHz	ARM Cortex™-M3	ARM Cortex™-M3	
Max DMIPS/MHz	1.25	1.25	
Flash [KB]	up to 128	up to 128	
RAM [KB]	up to 10	up to 16	Enhancement: the application can use larger RAM memory space.
EEPROM [KB]	2	2	
Backup registers [B]	20	20	
Flash interface [bits]	64/32	64/32	
Bootloader	USART1/2	USART1/2	
DMA / channels	1 / 7ch	1 / 7ch	
USART	3	3	
SPI / I2S	2 / 0	2 / 0	
I2C	2	2	
USB 2.0	1 x FS	1 x FS	
LCD [seg x com]	8 x 28	8 x 28	
LCD rails decoupling	NO	YES	Better LCD contrast for larger displays (if used external LCD rails decoupling capacitors). If not used no software change is required.
TIMER [32-bit/16-bit/Lite]	0/6/2	0/6/2	
IWDG/WWDG	1/1	1/1	
Clock	HSI/HSE/LSI/LSE CSS on HSE	HSI/HSE/LSI/LSE CSS on HSE/LSE	Extension of CSS to LSE. Backward compatible. If not used then no software change is needed.
HSI/HSI clock trimming	Trimming by customer (default +/- 10%)	Trimming by customer (default +/- 10%)	
RTC version	RTC V1.0	RTC V2.0	New RTC as in whole L1 family - with subsecond resolution. If not used then no software change is needed.
DAC	2	2	
ADC (total / fast channels)	1 (24 / 6)	1 (24 / 6)	
Comparator	2	2	
Touch sensing [channels]	NO	NO	
Temperature sensor	NO	NO	

Table 5. STM32L100x6/8/B-A and STM32L100x6/8/B device difference summary(1) (continued)

Function	STM32L100x6/8/B	STM32L100x6/8/B-A	Behavior / impact to software
Internal voltage reference	YES	YES	
Unique ID	NO	NO	
MCO	YES	YES	
PCROP	NO	NO	

1. The grayed cells highlight the differences between the device sets.

Note: For additional information, please refer to the STM32L100xx, STM32L151xx, STM32L152xx and STM32L162xx advanced ARM®-based 32-bit MCUs reference manual RM0038 in which STM32L15xx6/8/B is 'Cat.1' device, STM32L15xx6/8/B-A is 'Cat.2' device, STM32L100x6/8/B is 'Cat.1' device, STM32L100x6/8/B-A is 'Cat.2' device and to the STM32L15xx6/8/B-A, STM32L15xx6/8/B, STM32L100x6/8/B-A, STM32L100x6/8/B datasheets. Documents are available for download from the company website at www.st.com/stm32.

3.1 Main peripheral/system changes

Some system properties and peripherals configurations were changed in the STM32L15xx6/8/B-A and STM32L100x6/8/B-A devices. The following sections describe these changes.

3.1.1 RAM space increase

The RAM area was increased in the STM32L15xx6/8/B-A device as follows:

- from 10 kB to 16 kB for STM32L15xx6-A,
- from 10 kB to 32 kB for STM32L15xx8-A,
- from 16 kB to 32 kB for STM32L15xxB-A.

The RAM area was increased in the STM32L100x6/8/B-A device:

- from 10 kB to 16 kB for STM32L100xB-A

This increase permits the applications to use more RAM variables (larger buffers).

3.1.2 Extended RTC version

The RTC version V2.0, the same in the whole L1 family is used in the STM32L15xx6/8/B-A and STM32L100x6/8/B-A devices. The new RTC is backward compatible with RTC version V1.0 used in STM32L15xx6/8/B and STM32L100x6/8/B devices. To use the new RTC features, it is necessary to use updated version of STM32L1xx Standard Peripherals Library.

The main features added into new RTC are the following:

- the subsecond resolution,
- the more accurate digital calibration,
- three improved tamper detection inputs (instead of one input in the previous version).

Note: For additional information, please refer to the STM32L100xx, STM32L151xx, STM32L152xx and STM32L162xx advanced ARM® -based 32-bit MCUs reference manual RM0038 in which STM32L15xx6/8/B is 'Cat.1' device, STM32L15xx6/8/B-A is 'Cat.2' device, STM32L100x6/8/B is 'Cat.1' device, STM32L100x6/8/B-A is 'Cat.2' device.

3.1.3 CSS on LSE

The Clock Security System (CSS) has been extended to LSE clock in the STM32L15xx6/8/B-A and STM32L100x6/8/B-A devices, while in STM32L15xx6/8/B and STM32L100x6/8/B, the CSS was only for HSE clock.

The enhanced CSS is backward compatible. To use the new CSS feature, it is necessary to use the updated version of STM32L1xx Standard Peripherals Library.

3.1.4 LCD rail decoupling

The external decoupling capability of LCD rails was implemented to improve the LCD contrast (for example for large LCD displays with higher segments capacity). On STM32L15xx6/8/B-A or STM32L100x6/8/B-A, specific pins can be connected to external capacitors that maintain a stable LCD rail voltage while driving the LCD segments.

The backward compatibility is fulfilled, there is not need of any software change. To use the new feature, the dedicated pins must be configured as input, the external capacitors should be connected and the LCD_CAPA[4:0] bits in the SYSCFG_PMC register must be configured.

For more details about LCD rail decoupling please refer to the STM32L100xx, STM32L152xx and STM32L162xx advanced ARM® -based 32-bit MCUs reference manual RM0038 in which STM32L15xx6/8/B is 'Cat.1' device, STM32L15xx6/8/B-A is 'Cat.2' device, and to the STM32L15xx6/8/B and STM32L100x6/8/B datasheets.

3.1.5 Proprietary code protection (PCROP)

The read protection of a given Flash area is implement in STM32L15xx6/8/B-A device, but not in STM32L100x6/8/B-A device. The Flash area cannot be read by any access (including software), it can be only executed. It can be used as intellectual property read protection of proprietary third party code which can be executed on customer side.

The implementation of this proprietary code read out protection (PCROP) is backward compatible. To use the PCROP feature it is necessary to correctly program the added option bytes (SPRMOD and WRPx option bytes).

For additional information, please refer to the STM32L100xx, STM32L151xx, STM32L152xx and STM32L162xx advanced ARM®-based 32-bit MCUs reference manual RM0038 in which STM32L15xx6/8/B is 'Cat.1' device, STM32L15xx6/8/B-A is 'Cat.2' device, STM32L100x6/8/B is 'Cat.1' device, STM32L100x6/8/B-A is 'Cat.2' device.

3.1.6 Number of backup registers

The number of backup registers has been decreased in STM32L15xx6/8/B-A device. The number of backup registers in the respective devices is as follows:

- STM32L15xx6/8/B: 80 backup registers,
- STM32L15xx6/8/B-A: 20 backup registers
- STM32L100x6/8/B-A and STM32L100x6/8/B: 20 backup registers.

If an existing software uses more than 20 backup registers, it is necessary to apply some changes when using the STM32L15xx6/8/B-A device. In this case the data can be stored alternatively into the EEPROM memory.

If in existing software uses less than 20 backup registers no change is required when using the STM32L15xx6/8/B or STM32L100x6/8/B.

3.1.7 Touch sensing interface change

The touch sensing interface has been modified in the STM32L15xx6/8/B-A device - the features are the same but there is a new software touch library for the STM32L15xx6/8/B-A device, available on the company website at *www.st.com/stm32*.

3.2 Device limitations, changes and/or updates

New revisions of errata sheets have been published for the STM32L15xx6/8/B-A and for the STM32L100x6/8/B-A devices. Several limitations that had been reported for the STM32L15xx6/8/B and for the STM32L100x6/8/B have been solved, while new limitations have been introduced. This section describes the changes in the device limitations.

Please refer to STM32L15xx6/8/B-A errata sheet and STM32L100x6/8/B-A errata sheet for details on the device limitations.

3.2.1 Removed limitations

The following limitations that applied to STM32L15xx6/8/B and STM32L100x6/8/B devices do not apply to STM32L100x6/8/B-A nor STM32L100x6/8/B-A devices:

- Factory trimming values not available (for temperature sensor and internal reference voltage).
- Debug support for low power modes with entry through the WFE instruction.
- Pull-up on PB7 when configured in analog mode.
- HSEBYP bit of Clock control register has an undefined reset value.
- USB line pull-up resistor has a value lower than 1.5kOhm.
- CRC still sensitive to communication clock when SPI is in slave mode even with NSS high.

3.2.2 Newly introduced limitations

The following limitations which were not present in STM32L15xx6/8/B nor STM32L100x6/8/B devices have been introduced for STM32L15xx6/8/B-A and STM32L100x6/8/B-A devices:

- The number of RTC backup registers is 20 bytes instead of 80 bytes.
- The data EEPROM cycling is limited to 100 kcycles instead of 300 kcycles.
- If the debugger is connected in JTAG mode and if JNRST (PB4) pin configuration is changed, the connection is lost.
- The wakeup sequence from Standby mode when using more than one wakeup source requires a special entry into Standby mode.

Please refer to STM32L15xx6/8/B, STM32L100x6/8/B errata sheets and STM32L15xx6/8/B-A, STM32L100x6/8/B-A errata sheets for details on the device limitations.

4 Development tool adaptations

The changes in the device hardware have impacted the development tools. Following the change of device identifier (DEV_ID) and some peripherals changes with the addition of new features, it has been necessary to upgrade the development tools as detailed hereafter.

1. DEV_ID changes:
   In STM32L100x6/8/B and STM32L15xx6/8/B devices, DEV_ID=0x416
   In STM32L100x6/8/B-A and STM32L15xx6/8/B-A devices, DEV_ID=0x429
   If the software or programming tool is using DEV_ID[11:0] field (in DBGMCU_IDCODE register) then the relevant changes must be applied in the software or tool.
2. Changes in the development tool configurations:
   a) IAR - install the latest version or apply the patch provided by ST support team to support the new device, and change the device type in the configuration.
   b) Keil - install the latest version that supports the new device, change the device type in the configuration, and change the ST link programming algorithm.
   c) Others - install the latest version that supports the new device, and change the device type in the configuration.
3. STM32L1xx standard peripherals library update:
   STM32L15xx6/8/B-A and STM32L100x6/8/B devices are supported in the latest version of STM32L1xx standard peripherals library. Make sure to use the latest version of STM32L1xx standard peripherals library to use the new peripheral features.
   a) The STM32L15xx6/8/B-A and STM32L100x6/8/B-A devices are supported from STM32L1xx standard peripheral library version 1.2.0 available from *www.st.com/stm32*.
   b) Define the macro STM32L1XX_MD and use it in the project *startup_stm32l1xx_md.s* file.
   c) Rebuild the existing project with the new library so it can be run on STM32L15xx6/8/B-A or STM32L100x6/8/B-A device.
4. Programming tools adaptation:
   In the programming tool configurations (for example ST link with the related software) the device type must be changed to correctly program the new STM32L15xx6/8/B-A or STM32L100x6/8/B-A device.
   Use the latest ST Visual Programmer (STVP) or the latest ST-link utility which support the new devices (both are available at *www.st.com/stm32*).

5 Consumption comparison

The STM32L15xx6/8/B-A or STM32L100x6/8/B-A devices feature less dynamic consumption than the STM32L15xx6/8/B or STM32L100x6/8/B devices respectively, due to the advanced manufacturing technology. The power consumptions in low-power modes are on similar levels.

Table 6 shows the differences in power consumption between the devices in the various operating modes.

Table 6. Consumption differences summary

Parameters (all at V_{DD}=3V)	STM32L15xx6/8/B STM32L100x6/8/B	STM32L15xx6/8/B-A STM32L100x6/8/B-A
Full speed from flash (32 MHz in HSI)	294 µA/MHz	257 µA/MHz
MSI clock from flash (4.2 MHz)	214 µA/MHz	185 µA/MHz
Low-power Run from RAM @ 32 kHz	9.0 µA	10.9 µA
Low-power sleep from RAM @ 32 kHz	4.4 µA	5.5 µA
Stop mode	500 nA	434 nA
Stop mode with RTC on LSI	1.40 µA	1.38 µA
Standby mode	300 nA	277 nA
Standby mode with RTC on LSI	1.30 µA	1.11 µA

6 Revision history

Table 7. Document revision history

Date	Revision	Changes
09-May-2014	1	Initial release.