
Reset and supervisor ICs: frequently asked questions (FAQ)

Introduction

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- What is the difference between a voltage detector and a reset IC?
- What are the main reset and supervisor IC categories?
- Why should I use a standalone reset IC if one is already integrated in the microcontroller?
- What are the following core features of reset and supervisor ICs used for?
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 - Manual reset (MR)
 - Reset pulse width (t_{REC})
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- What are the following additional options of reset and supervisor ICs used for?
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 - Chip enable gating
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 - Reset input delay time (t_{SRC})
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1 When to and why use reset and supervisor ICs?

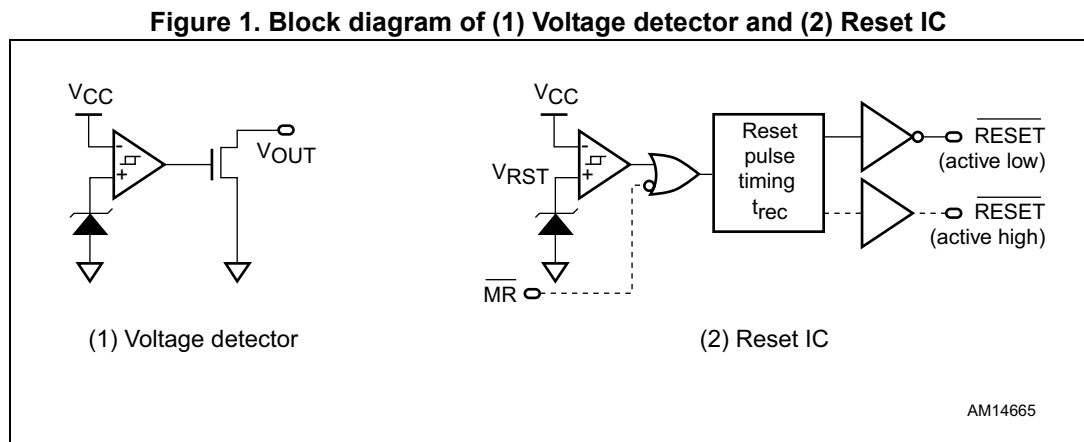
The reset and supervisor functions should be used in complex systems to ensure proper wake-up during power-up, and/or to reboot the system when an application has failed or frozen.

With the increased development and utilization of microprocessing units (example, 8-bit low cost, 32-bit low power, 64-bit high performance, multi-core) in all kind of applications, there is an ever-increasing need for reset and supervision functions.

Reset and supervisor ICs are like the lifeguard of a system: they protect against software and power failure. Using them makes the final product more robust, whatever its complexity, and increases the end-users perception of quality.

2 What is the difference between a voltage detector and a reset IC?

The main difference is the reset pulse width (t_{REC}) feature on the output pin (see [Section 5: What are the following core features of reset and supervisor ICs used for?](#)). Voltage detectors act as comparators and do not have any t_{REC} whereas it is a major feature of a reset IC (see [Figure 1](#)).



Voltage detectors also integrate accurate hysteresis functions (V_{th+}/V_{th-}) whereas only one voltage threshold is usually specified for a reset IC (V_{th}). In addition, the noise immunity of a reset IC is native by design due to the t_{REC} feature.

Suggested products

- For further information on voltage detectors, please refer to **STM1061**
- For further information on reset ICs, please refer to **STM809** and **STM1001**

3 What are the main reset and supervisor IC categories?

3.1 Reset and voltage detectors

These devices provide basic voltage monitoring and reset timing for the power-on reset (POR) and low-voltage detect (LVD) function. Some devices feature an additional input which can be used for push-button reset. Other devices are designed to monitor up to five power supply voltages.

3.2 Microprocessor supervisors

These devices add additional features including a watchdog, early power fail warning, push-button reset, and battery monitoring. Microprocessor supervisors with a switchover function preserve SRAM data in the absence of system power by automatically switching to battery backup when system power fails. A chip enable gate automatically write protects the SRAM when V_{CC} begins to fall.

3.3 Smart resets

Smart resets extend the functional capability of existing buttons so that users can simply reset their frozen device with a long push of one or two buttons simultaneously. Smart Reset™ devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart Reset™ input delay time and combined push-button inputs, which together ensure a safe reset and eliminate the need for a specific dedicated reset button.

3.4 Watchdog timers

Watchdog timers are mandatory products for applications requiring the highest security level. They are a robust and reliable way of monitoring software code execution or hardware failure and taking appropriate action (example, system reboot, high level interrupt generation).

For higher efficiency, the watchdog function is usually not integrated into the microprocessor, but implemented with standalone products. STMicroelectronics offers various watchdog implementations, allowing a match with most application environments.

3.5 Voltage protection

These devices provide the necessary protection that prevent external overvoltage peaks from damaging the internal circuitry. They are commonly implemented on the power charging patch of portable devices, to prevent a USB or an AC charger power failure.

4 Why should I use a standalone reset IC if one is already integrated in the microcontroller?

1. A standalone reset IC has the following advantages over a microcontroller-integrated POR or LVD:
 - a) A reset IC functions while the microcontroller is in low power mode.
 - b) A reset IC has a much lower consumption (10 μ A) than a POR/LVD (100 μ A).
 - c) For a reset IC, the V_{CC} rise rate does not have to be under control, whereas a POR/LVD does not work if the V_{CC} rise rate is not under control.
 - d) The accuracy of the reset voltage threshold, across the temperature range -40 °C to 85 °C, is good for a reset IC (250 mV) whereas it is poor for a POR/LVD (400 mV).
 - e) For a reset IC, a brownout detect cannot be disabled by software.
2. A standalone reset IC can monitor dedicated peripheral voltages
3. Standalone reset ICs can be put in parallel
Example: in an application with a mixture of 1.8 V and 3 V components, including 1.8 V and 3.3 V processors, both processors must be reset even if only one supply drops out of tolerance.
4. A reset IC guarantees a reset that is long enough to stabilize the V_{CC} and ensure that the microcontroller and any peripherals work at power-up.

5 What are the following core features of reset and supervisor ICs used for?

5.1 Power-on reset (POR)

After system startup, a certain period of time is required for the power supply voltage to stabilize. Consequently, ST supervisor devices usually generate a reset pulse after power-up. The t_{REC} is typically 140 ms. Over the t_{REC} period, during which time the reset is asserted, the clock is stabilized and the registers are set to their default values. This function is called POR.

5.2 Low-voltage detect (LVD)

Another major function of reset and supervisor ICs is low voltage detection (LVD), which detects power supply brownouts and glitches. Whenever V_{CC} falls below the reset threshold (V_{RST}), the reset output is asserted and remains so t_{REC} after V_{CC} increases above the V_{RST} threshold. In the case of an RC circuit, no minimum reset pulse width is guaranteed. Also, if the triggering event is a narrow glitch, an RC circuit only generates a poor reset, which may lead to malfunctioning of the microprocessor (example, failure to load registers correctly, execution of invalid instructions, processing incorrect data). In contrast, reset and supervisor ICs are safe and robust by design.

5.3 Manual reset (MR)

Some supervisor devices include a manual reset input (MR) that can be used by the user, or the external device, to generate a reset. Typically, a low cost push-button switch is connected to the MR input, which allows the user to restart the processor without turning off the power. No additional components are needed because supervisor devices already include a debounce IP that filters the noise of contact closure. This function can be used to debug, to perform the final test of a processor, or to restart a processor that is locked. The reset button is also useful in systems where the processor is never turned off, even when the system is in off mode. Some processors include an internal reset that operates correctly under stable power supply conditions, but usually has difficulties in handling voltage drops and transients as well as looser tolerances for V_{RST} . The use of an external reset is therefore recommended.

More details

- See AN1957: Microprocessor Supervisor Functions, page 13
- See AN1772: How to Control Power-up/Reset and Monitor the Voltage in Microprocessor Systems using ST Reset Circuits

5.4 Reset pulse width (t_{REC})

The t_{REC} time defines the pulse width duration when the reset output is asserted. It guarantees that all connected devices are properly reset and that the system restarts synchronously. Typical values are 150 ms or 210 ms, but the ST portfolio offers configurations from 1.4 ms to 1680 ms and even an adjustable configuration.

Suggested products

For further information on t_{REC} times, please refer to the following products:

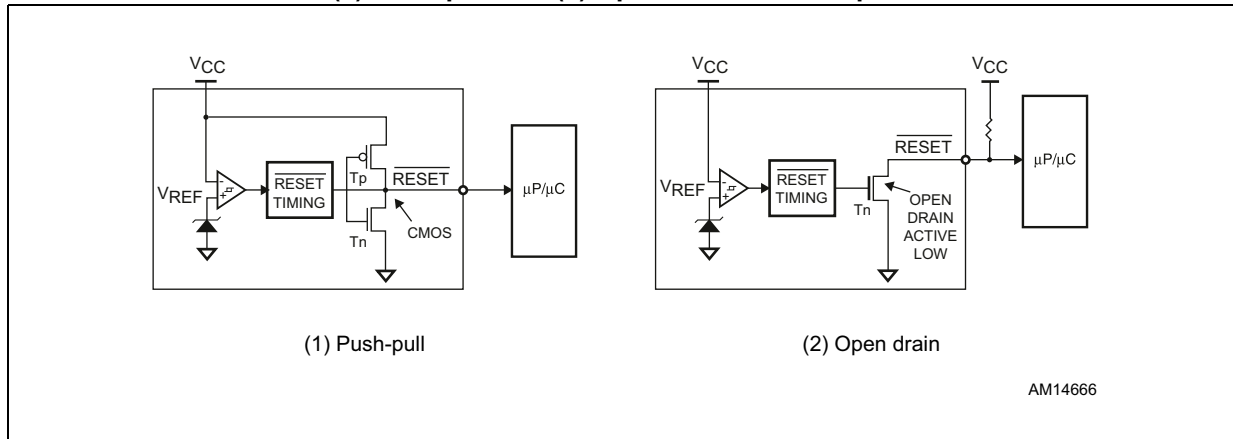
- **STM6321** when $t_{REC} = 1.4$ ms
- **STM6315** when $t_{REC} = 1680$ ms
- **STM1831** when t_{REC} is adjustable

5.5 Push-pull and open drain reset outputs

A push-pull output consists of a pair of complementary MOSFETs. The reset output goes high when the PMOS transistor (T_p) turns on and the NMOS transistor (T_n) turns off. Similarly, the reset output goes low when T_p turns off and T_n turns on (see [Figure 2](#)).

For open drain outputs, the transistor is turned OFF in normal mode. Hence, the reset output is at high level (in the case of an N-channel transistor). In the event that V_{CC} drops below V_{REF} , the transistor is turned ON for a minimum of time. Hence, the reset input of the microprocessor has a low signal and the microprocessor is reset. Conversely, active high resets (a minority) are designed with a P-channel transistor (see [Figure 2](#)).

Figure 2. Reset output block diagram for (1) Push-pull and (2) Open drain reset outputs



[Table 1](#) gives a comparison of a push-pull versus an open drain reset output.

Table 1. Comparison of a push-pull versus an open drain reset output

	Advantages	Drawbacks
Push-pull	<ul style="list-style-type: none"> - Fast rise time - No current is drained at high and low state - current is drained only during transitions. - Almost rail-to-rail response both from low to high and high to low. - Capability to source or sink current 	<ul style="list-style-type: none"> - Not possible to connect to several resets in parallel
Open drain	<ul style="list-style-type: none"> - Wired-OR capability - several resets can be connected in parallel. 	<ul style="list-style-type: none"> - Slow rise time - charge or discharge of an RC circuit. - Current flows in the pull-up (or pull-down) resistance (mA) when the reset is activated.

6 What are the following additional options of reset and supervisor ICs used for?

6.1 Backup battery switchover

A common task of battery switchover devices is to provide an uninterrupted power supply to external devices (SRAM for example) in the event of a power failure (voltage drops, brownout). Battery switchover devices can also be useful in portable devices. When the external power supply (such as the AC power supply adapter) is disconnected, the battery switchover device switches to the internal supply (such as a battery). Battery switchover devices can be used as a main power supply backup for MCUs, memories, and other peripherals, and to prevent system failures.

Advantages of battery switchover devices

- They provide continuous and reliable operation, even if the external supply fails
- They extend the battery lifetime
- They allow debouncing of the power spikes while connecting and disconnecting the AC adapter.

Note: When the battery is first connected without V_{CC} power applied, the device does not immediately provide battery backup voltage on V_{OUT} . Only after V_{CC} exceeds V_{RST} will the switchover operate. This mode allows a battery to be attached during manufacturing but not used until the system has been activated for the first time. As a result, no battery power is consumed by the device during storage and shipment. If the backup battery is not used, connect both V_{BAT} and V_{OUT} to V_{CC} .

More details

See AN1957: Microprocessor Supervisor Functions, page 13

Suggested products

For further information on battery switchover devices, please refer to the following products: **STM690**, **STM704**, **STM795**, **STM802**, **STM804**, **STM805**, **STM806**, **STM817**, **STM818**, and **STM819**.

Design tip

Supervisor circuits are not short-circuit protected. Shorting V_{OUT} to ground - excluding power-up transients such as charging a decoupling capacitor - destroys the device. Therefore, it is recommended to decouple both V_{CC} and V_{BAT} pins to ground by placing the 0.1 μF capacitors as close to the device as possible.

6.2 Battery freshness seal

A battery freshness seal avoids the discharge of leakage current from the battery it is connected to. In practice, it disconnects the backup battery from the supply output voltage and the internal circuitry until it is needed. This allows manufacturers to ensure that the backup battery stays fresh when the final product is put to use.

Once a battery freshness seal is enabled (disconnecting the backup battery from the external world), it remains enabled until V_{CC} is next brought above V_{RST} .

More details

See AN1957: Microprocessor Supervisor Functions, page 20

Suggested products

For further information on battery freshness seals, please refer to the following products on: **STM817**, **STM818**, and **STM819**.

6.3 Watchdog

A watchdog timer is used to protect the system against runaway software. If the system software fails to occasionally reset the watchdog timer, the timer resets the microprocessor thereby restoring the system to proper operation.

In a microcontroller, the embedded watchdog can be usually disabled by software, and its timing is incremented with the microcontroller clock. Hence, it does not provide full protection against hardware and software issues, which can be critical for applications requiring stringent constraints for safety purpose.

Recommended use of standalone watchdogs

- Applications requiring stringent constraints for safety purpose (medical applications, alarms, security equipment).
- Applications that need redundancy
- Applications requiring a longer watchdog than the one provided by the microcontroller

More details

- See AN1957: Microprocessor Supervisor Functions, page 11
- See the STWD100 flyer: Standalone watchdog with chip enable improves system reliability

Suggested products

For further information on watchdogs, please refer to the following products: **STWD100**, **STM6321**, **STM682x**, **STM69x**, **STM70x**, **STM80x**, and **STM81x**.

6.4 Chip enable gating

Internal gating of the memory chip enable signal (E) prevents erroneous data from corrupting the external SRAM in the event of an undervoltage condition. The chip enable signal, which normally goes directly from the microcontroller to the SRAM, is routed instead through the supervisor device. The short propagation delay enables the chip enable gating to be used with most microcontrollers. During normal operation (reset not asserted), the transmission gate is enabled and passes all E transitions. When reset is asserted, this path becomes disabled, preventing erroneous data from corrupting the SRAM.

More details

See AN1957: Microprocessor Supervisor Functions, page 17

Suggested products

For further information on chip enable gating signals, please refer to **STM795** and **STM818**.

6.5 Early power failure

Inadvertent or unexpected power loss can cause a number of malfunctions in a system (example, data loss, uncontrolled program status, and indeterminate processor state). For a reliable design, systems should receive early power failure warnings, to leave enough time for the microprocessor to start a safeguard routine, for backing up crucial data (example, registers). Hence, power fail comparators are used to monitor unregulated or failing power supplies through a voltage divider. Their reaction to power loss is very fast, and can provide enough time to execute all the necessary safeguard processes that precede an expected power failure.

More details

- See AN1957: Microprocessor Supervisor Functions, page 18
- See AN1336: Power-Fail Comparator for NVRAM Supervisory Devices

Suggested products

For further information on early power failures, please refer to the following products on: **STM69x**, **STM70x**, **STM80x**, **STM81x**, and **STM1404**.

Design tip

The power fail comparator input may be connected to a manual reset so that an early low voltage condition generates a reset output.

6.6 Anti-tampering functions

Anti-tampering functions are specific functions especially designed to provide intrusion detection, and to protect against unfriendly or hostile activity. They include:

- Over/under operating temperature detection (customer-selectable and factory trimmed)
- Over/under operating voltage detection
- Four high impedance physical tamper inputs
- Security alarm (SAL) if tampering is detected

Anti-tampering functions mainly address a manufacturer's point of sales (POS) terminals and other systems. They meet physical and/or environmental intrusion monitoring requirements mandated by various standards, such as the **Federal Information Processing Standards (FIPS) Pub 140-1: Security Requirements for Cryptographic Modules**, published by the US Department of Commerce/National Institute of Standards and Technology.

More details

See AN2377: Using the STM1403/1404 security supervisors to clear external SRAM

Suggested products

For further information on anti-tampering functions, please refer to **STM1404**.

6.7 Reset input delay time (t_{SRC})

The t_{SRC} defines the time during which one or several push-buttons must be simultaneously pressed before a reset is asserted. This option is specific to the Smart Reset™ devices. See [Section 7: What is a Smart Reset™ and what is it used for?](#) for more details.

7 What is a Smart Reset™ and what is it used for?

Smart Reset™ devices provide a useful feature that ensures inadvertent short reset push-button closures do not cause system resets. This is done by implementing extended Smart Reset™ input delay time (t_{SRC}) and combined push-button inputs, which together ensure a safe reset and eliminate the need for a specific dedicated reset button.

Such reset configuration provides versatility and allows the application to distinguish between a software generated interrupt and a hard system reset. When input push-buttons are connected to microcontroller interrupt inputs, and are closed for a short time, the processor can only be interrupted. If the system still does not respond properly, keeping the push-buttons closed for the reset input delay time (t_{SRC}) causes a hard reset of the processor through the reset output.

More details

- See AN3261: Dual push-button Smart Reset™ devices with user-adjustable setup delays
- See e-presentation: Smart reset ICs for the STM6519 and STM6524
- See the STM65xx flyer: Smart resets eliminate dedicated reset buttons and prevent accidental resets

Suggested products

For further information on Smart Reset™ devices, please refer to the following products: **STM6503, STM6504, STM6505, STM6510, STM6513, STM6519, STM6520, STM6522, and STM6524.**

8 With Smart Reset™ devices, is the reset asserted repeatedly if a push-button is pressed for a long time?

For Smart Reset™ products with t_{REC} options (fixed reset pulse width durations), only one reset pulse is sent to the system if the push-button(s) is (are) pressed and held. The push-button(s) need(s) to be released and pressed again for t_{SRC} before the reset is asserted again for t_{REC} time.

For Smart Reset™ products without t_{REC} (push-button controlled reset pulse width durations), the reset output is asserted as long as the push-button is pressed (after t_{SRC}). The push-button(s) need(s) to be released to de-assert the reset output.

9 Support material

Application notes

- AN1957: Microprocessor Supervisor Functions
- AN1772: How to Control Power-up/Reset and Monitor the Voltage in Microprocessor Systems using ST Reset Circuits
- AN1336: Power-Fail Comparator for NVRAM Supervisory Devices
- AN2377: Using the STM1403/1404 security supervisors to clear external SRAM
- AN3261: Dual push-button Smart Reset™ devices with user-adjustable setup delays
- AN1790: How to Connect ST Reset Circuits to a Microprocessor
- AN2504: Using STMicroelectronics Voltage Detectors
- AN3050: STBP120 overvoltage protection device
- AN3271: Using the STM6600, STM6601 smart push-button on/off controller

e-presentations

- Smart reset ICs for the STM6519 and STM6524
- STBP110/STBP112: Overvoltage protection devices
- STM6600/STM6601: Smart on/off controller

Flyers

- STWD100: Standalone watchdog with chip enable improves system reliability
- STM65xx: Smart resets eliminate dedicated reset buttons and prevent accidental resets
- STM66xx: Smart on/off controllers for safe and simple control of applications using push buttons
- STM6904 and STM6905: Quad/quintuple, ultra-low current, multiple-voltage supervisors

10 Revision history

Table 2. Document revision history

Date	Revision	Changes
22-Aug-2013	1	Initial release.

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