AN1009
Application note

Negative undershoot NVRAM data corruption

Introduction

Miniaturization in microelectronics has led, inevitably, to the inadvertent appearance of parasitic devices. Adjacent conducting paths end up being separated by a gap that is so narrow that it ceases to isolate them properly from each other. Parasitic tunnelling devices, bipolar transistors, and thyristors end up being formed, with each one causing its own distinctive misbehavior.

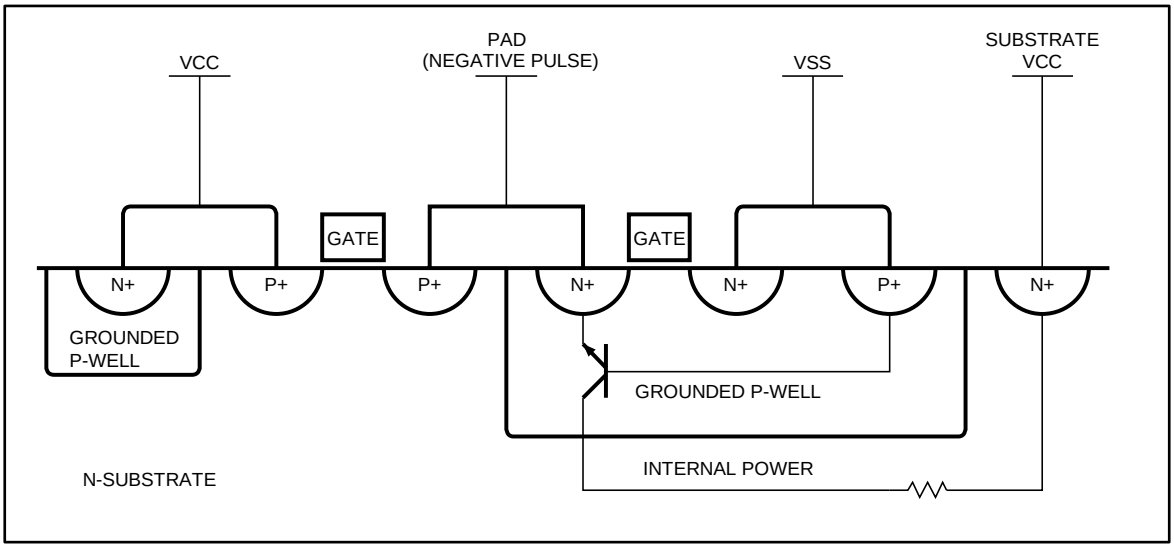
The occurrence of parasitic SCRs (silicon controlled rectifiers) causes the well-studied problem of latchup. The occurrence of parasitic bipolar transistors, such as the one shown in *Figure 1: "Cross-section of an NPN parasitic bipolar transistor"*, is normally less serious, but leads to a particular type of problem in battery-powered circuits. It is this problem that is addressed in this document.

The problem manifests itself in battery-powered memory as data corruption: the unintentional flipping from 1 to 0, or from 0 to 1, of bits of data in the memory array. It is caused when a negative pulse is inadvertently applied to the emitter of an inadvertently formed parasitic bipolar transistor, causing it to go into conduction mode, and to connect two otherwise isolated signal lines.

1 Anatomy of a parasitic bipolar transistor

Figure 1: "Cross-section of an NPN parasitic bipolar transistor" shows the cross-section of a CMOS gate, with one MOSFET formed directly in the N-type substrate, and the other in a P-well. Under certain conditions, the P-well can start to behave as the base region of a parasitic bipolar NPN transistor, with the N-type substrate as its collector region, and the N+ diffusion contact of the MOSFET as its emitter region.

Figure 1: Cross-section of an NPN parasitic bipolar transistor



The P-well is held at ground, so the parasitic NPN transistor should never turn on. If, though, a negative pulse is applied to the pad, and hence to the emitter of the parasitic NPN transistor, the transistor would be put into its conducting mode. Once the pad is taken to $-V_{be}$, the parasitic bipolar transistor turns on, and pulls current from the substrate.

When the memory device is being powered by the external power source, the effect of this extra parasitic current will be negligible, and will be compensated for by the external power source. When the memory device is being powered from the internal battery, though, the battery is unable to compensate for the extra current, and so the supply voltage will fall. As soon as the supply voltage falls below a critical value, SRAM cells in the memory array will cease to hold their stored data reliably.

The parasitic bipolar transistor starts to turn on when the pad is taken to about -0.6 V. In battery mode, the impact on the substrate will start to be felt once the current drain through the bipolar transistor is approximately -0.6 mA. The substrate will be pulled to approximately 1.0 V once the current through the bipolar transistor reaches -1.5 mA. As the magnitude of the negative current increases, it directly reduces the level of internal V_{CC} (the substrate voltage). A current drain of approximately -2.0 mA will bring internal V_{CC} to ground, thus leaving the SRAM array completely unpowered.

Figure 2: Substrate V_{CC} versus negative undershoots

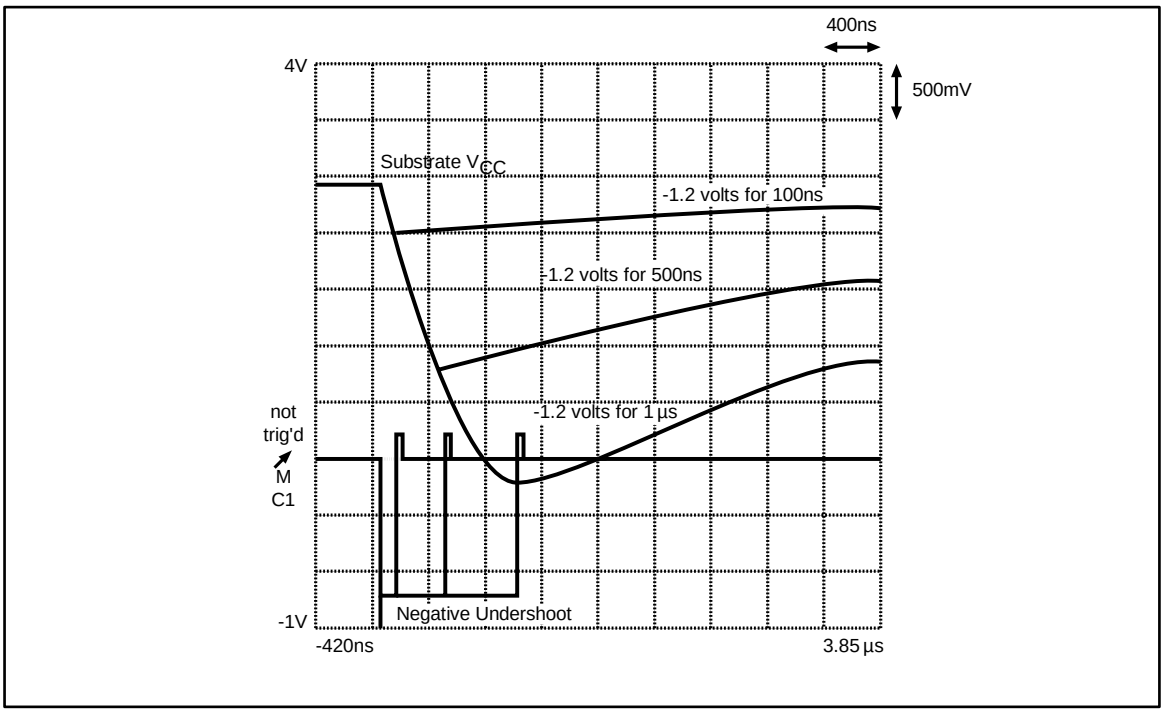


Figure 2: "Substrate V_{CC} versus negative undershoots" superimposes three pairs of curves: three negative undershoot pulses of 100, 500 and 1000 ns duration; and the corresponding effects that are felt by the V_{CC} substrate voltage.

Thus, we see that the effect on the substrate voltage is proportional to the duration of the negative undershoot pulse. It is also proportional to its magnitude (its amplitude). It is also proportional to the number of pins that receive the negative undershoot pulse (the example, above, is the effect of just one pin on the chip going negative).

2 Remedies

ST is continually making design and process modifications to improve the performance of its products. Immunity to negative undershoot will be improved over time, but only where it does not have a negative impact on other performance measures, such as operating speed.

The application designer is, therefore, advised to take steps to avoid negative undershoot pulse from being introduced. The first step is to improve the cleanliness of each of the signals. *Table 1: "List of the pins on devices that are affected by the problem"*lists the pins of ST's NVRAMS that are affected (those that consist of an N+ diffusion in a P-well on an N-type substrate).

Table 1: List of the pins on devices that are affected by the problem

Device	Substrate type	Pins connected to N+ diffusion
M40Z111	N-	13, 16
M40Z300	N-	4, 10, 13, 16, 20, 22, 23
M48Z02, M48Z12	N-	All
M48Z08, M48Z18	P-	None (not applicable)
M48Z58, M48Z58Y	N-	1, 11-13, 15-19, 26, 28
M48Z35, M48Z35Y	N-	All
M48T02, M48T12	N-	All
M48T08, M48T18	P-	(none) not applicable
M48T58, M48T58Y, M48T59, M48T559	N-	1, 11-13, 15-19, 26, 28
M48T35, M48T35Y, M48T35AV	N-	All
M48T37V, M48T37Y	N-	1, 4-10, 13, 15-20, 22-26, 30, 31, 33-39

All pins that are connected to N+ diffusion are susceptible to negative undershoot, but special attention should be given to the V_{CC} pin. This is connected to internal circuitry that increases the pin's sensitivity to negative undershoots, to the extent that pulses of greater than -0.3 V may affect the substrate voltage.

The second step, therefore, is to clamp the power lines (V_{CC} and V_{SS}) with a Schottky diode, to short out any attempt by them to go negative. Its effectiveness depends on its speed of operation set against the speed and energy content of the negative-going pulse (the current sink capability of the pulse). An off-the-shelf diode with a V_{be} of approximately 0.32 V, and a current rating of 100 mA, will generally reduce the occurrence of the problem to negligible proportions. However, the higher the current sink capability of the negative pulse, the more likely an RF Schottky diode is required.

The Schottky diode should be placed as close to the device pin as possible.

V_{CC} can be subject to mechanical noise, the switching of V_{CC} on and off, and to negative spikes coming from the power supply during initial power up. The third step, then, is to clean up the power supply, particularly its behavior at power-on and power-off, where the memory device is expected to continue to power itself from its internal battery. Particular care should be taken when working with programmable power supplies. Forcing a

programmable power supply from a positive voltage to 0 volts without taking care to step down the voltage can generate a negative undershoot pulse.

The fourth step is to protect each of the pins, mentioned in *Table 1: "List of the pins on devices that are affected by the problem"*, by its own individual Schottky diode. No pin should exceed -0.3 V, and their collective reverse current should not be allowed to exceed -1.0 mA, especially when the memory device is being battery-powered.

3 Revision history

Table 2: Document revision history

Date	Revision	Changes
Dec-1998	1	Initial release
24-Oct-2013	2	Updated devices in *Table 1: "List of the pins on devices that are affected by the problem"*