AN2785
Application note

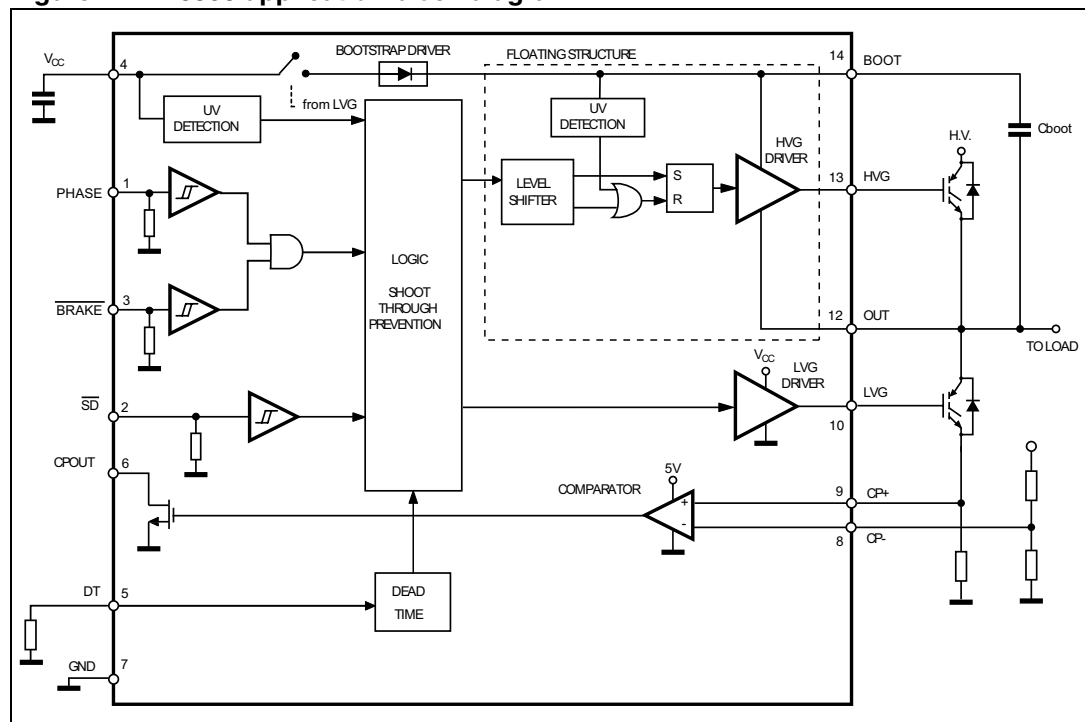## L6393 half bridge gate driver

Introduction

The L6393 is a versatile high-voltage gate driver IC particularly suited to motor driving applications. It simplifies the design of control systems for a wide range of motor applications such as home appliances, industrial drives, DC motors and fans.

Developed using BCD offline technology, the device can operate with voltage rails up to 600 V. The gate driver provides all the functions and current capability necessary for high-side and low-side power MOS and IGBT driving.

The L639x are high voltage half-bridge gate drivers. These devices can be used in all applications where high voltage shifted control is necessary. The devices have a driver current capability best suited for motor driving ratings and they are also equipped with patented internal circuitry which replaces the external bootstrap diode. This feature is achieved by means of a high-voltage DMOS synchronously driven with the low-side gate driver.

The L6393 is an half-bridge driver with several functionalities such as externally adjustable dead-time, shut-down function and an uncommitted comparator. The outputs can be driven by a special logic input interface particularly suitable for phase/brake functions. The device is available in DIP-14 or SO-14 packages.

Figure 1.   L6393 application block diagram

Contents

List of figures

1 Pin description

Table 1. Pin description

Pin n.	Pin name	Type	Function
1	PHASE	I	Driver logic input (active high)
2	$\overline{\text{SD}}$	I	Shut-down logic input (active low)
3	$\overline{\text{BRAKE}}$	I	Driver logic input (active low)
4	VCC	P	Lower section supply voltage
5	DT	I	Dead time setting
6	CPOUT	O	Comparator output (open drain)
7	GND	P	Ground
8	CP-	I	Comparator negative input
9	CP+	I	Comparator positive input
10	LVG [1]	O	Low side driver output
11	NC		Not connected
12	OUT	P	High side (floating) common voltage
13	HVG [1]	O	High side driver output
14	BOOT	P	Floating section (bootstrap) supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (at Isink = 10 mA), with V_{CC} > 3 V. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver also ensures low impedance in SD condition.

2 Logic inputs

In the L6393 IC the two input signals (PHASE and $\overline{\text{BRAKE}}$) are fed into an AND logic port and the resulting signal is in phase with the high-side output HVG and in opposition of phase with the low-side output LVG. This means that if $\overline{\text{BRAKE}}$ is held high, the PHASE signal drives the half bridge in phase with the HVG output and in opposition of phase with the LVG output. If $\overline{\text{BRAKE}}$ is set to low, the low-side output LVG is always ON and the high-side output HVG is always OFF, regardless of the PHASE signal. This kind of logic interface provides the possibility of controlling the power stages using the PHASE signal to select the current direction in the bridge and the $\overline{\text{BRAKE}}$ signal to perform current slow decay on the low sides or even a brake function on the low-side power transistors in case of multi-phase power bridges (for example, full or 3-phase bridges).

From the point of view of logic operations, the two signals PHASE and $\overline{\text{BRAKE}}$ are completely equivalent, meaning that the two signals can be exchanged without changing the behavior on the resulting output signals (see the block diagram in *Figure 1 on page 1*).

Note: *The dead time between the turn OFF of one power switch and the turn ON of the other power switch is defined by the resistor connected between the DT pin and ground.*

Figure 2.   Input configurations
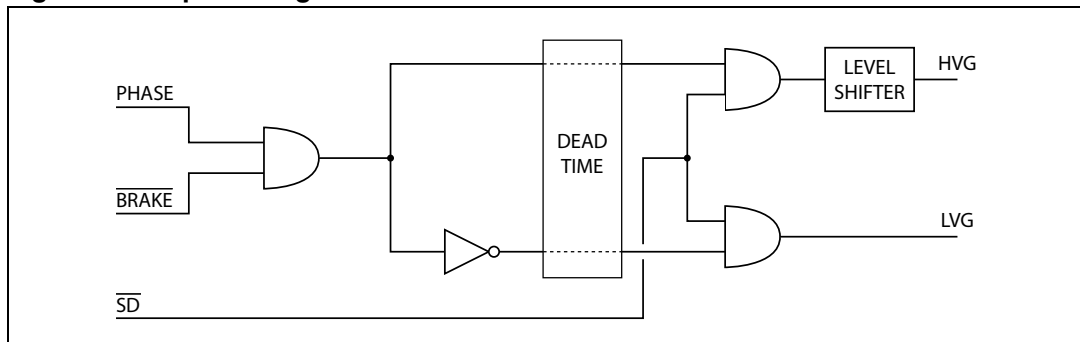
All the logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL//CMOS 3.3 V-compatible. Thanks to this low voltage interface logic compatibility, the L6393 can be used with any kind of high performance controller, such as microcontrollers, DSPs or FPGAs.

As shown in the block diagram of *Figure 1* the logic inputs have internal pull-down resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption of the logic lines or the controller outputs are in tri-state conditions: if logic inputs are left floating, the gate driver outputs LVG and HVG are set high and low respectively. The internal resistors are:

● PHASE logic input: 375 kΩ (typ.) pull-down.

● $\overline{\text{BRAKE}}$ logic input: 375 kΩ (typ.) pull-down.

● $\overline{\text{SD}}$ logic input: 500 kΩ (typ.) pull-down.

Table 2.   L6393 truth table

Inputs			Outputs	
$\overline{SD}$	Phase	$\overline{BRAKE}$	LVG	HVG
L	X	X	L	L
H	L	L	H	L
H	L	H	H	L
H	H	L	H	L
H	H	H	L	H

Note: *X: don't care.*

3 UVLO function

The L6393 supply voltage V_{CC} is continuously monitored by an under-voltage lock-out (UVLO) circuitry, which turns off the IC outputs when the supply voltage goes below the V_{CC_thOFF} threshold (see L6393 datasheet for values) and turns on the device when the supply voltage goes above the V_{CC_thON} voltage. A hysteresis of about 1.5 V is provided for noise rejection purposes. The high voltage floating supply BOOT is also provided with a similar under-voltage lock-out circuitry. When the L6393 is in a UVLO condition, both gate driver outputs are set to low, setting the half-bridge power switches to high impedance. *Figure 3* shows the I-V characteristics of the output buffers at different V_{CC} values.

Figure 3. L6393 gate driver outputs in UVLO condition
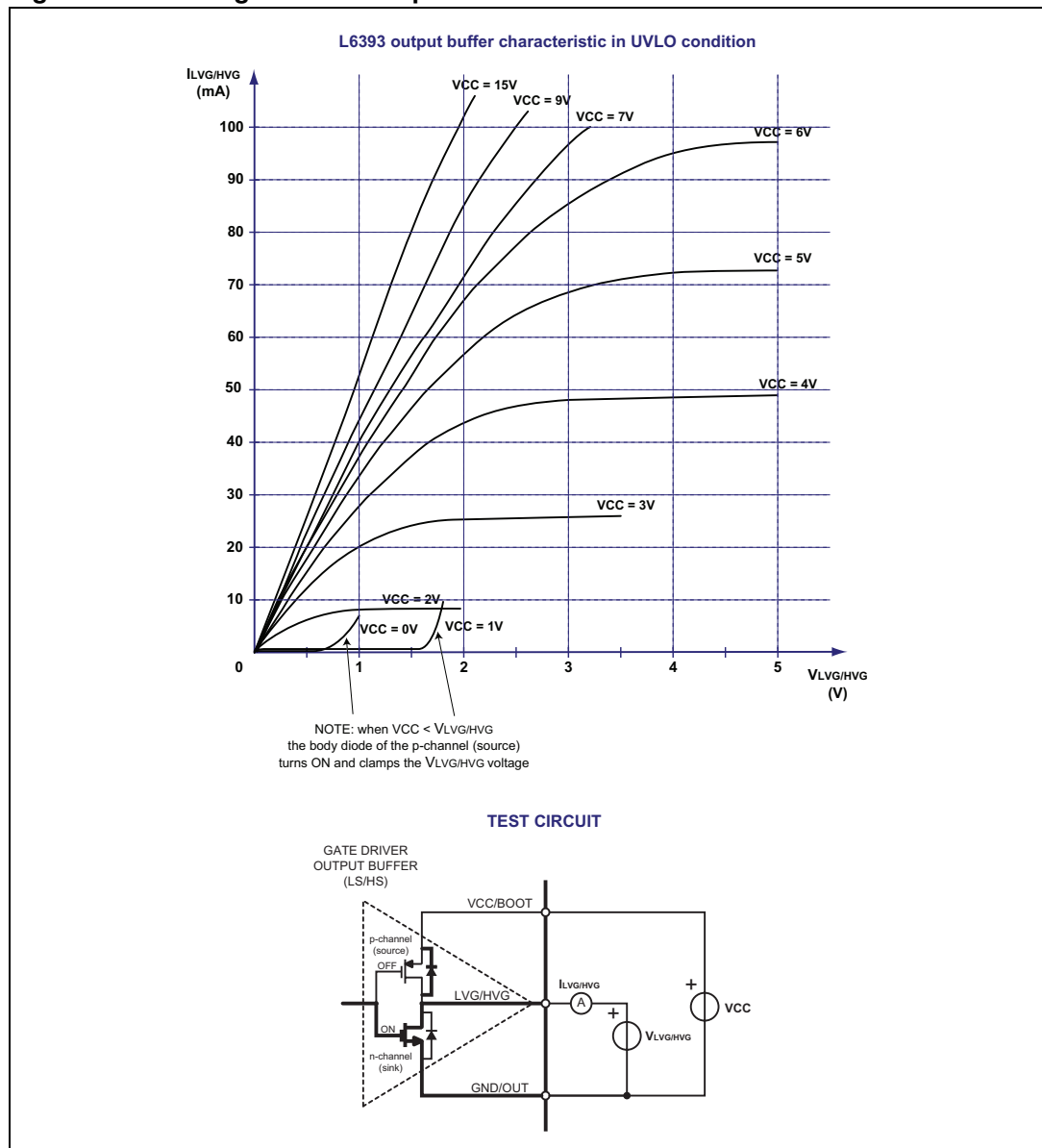
4 Dead time function

To avoid any possible cross-conduction between the power MOSFETs/IGBTs of the half bridge, the L6393 provides a dead time. The dead time function is a safety time introduced by the device between the falling edge transition of one driver output and the rising edge of the other output. The dead time can be adjusted externally through the value of the DT resistor connected between pin 5 and pin 7 as indicated in *Figure 5*. A 100 nF ceramic capacitor in parallel to this resistor is recommended for noise immunity. *Figure 4* provides details of the dead time.

Figure 4.   Timing waveforms
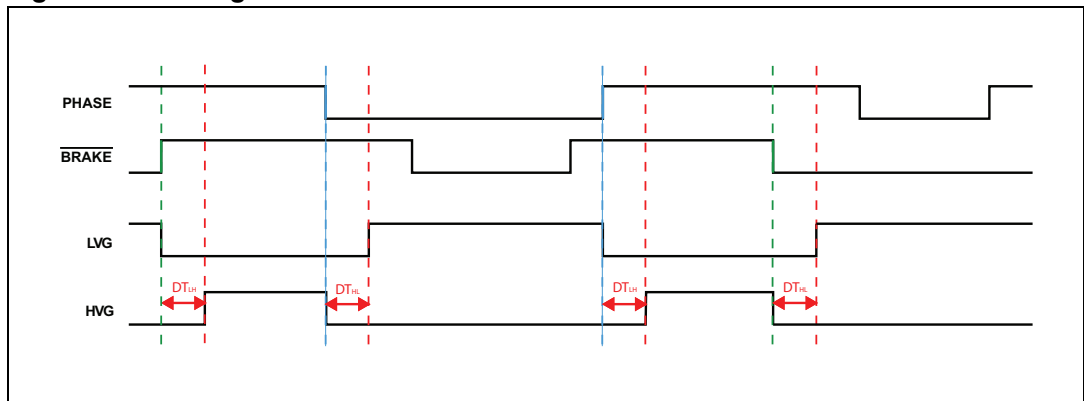
Figure 5.   Typical dead time vs DT resistor value
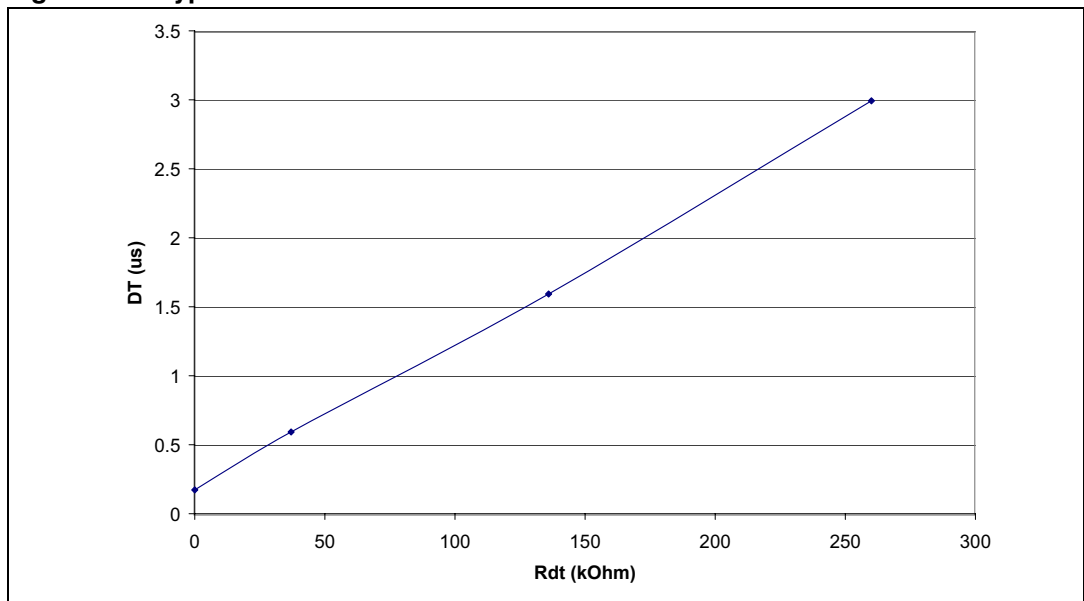
5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high-voltage fast recovery diode (*Figure 6* a). In the L6393 a patented integrated structure replaces the external diode. It is realized with a high-voltage DMOS driven synchronously with the low-side driver (LVG), with a diode in series, as shown in the *b* part of *Figure 6 on page 11*. An internal charge pump (*Figure 6* b) provides the DMOS driving voltage.

5.1 C$_{BOOT}$ selection and charging

To choose the proper C$_{BOOT}$ value the external MOS can be seen as an equivalent capacitor. This capacitor CEXT is related to the total gate charge of the MOS.

Equation 1

$$C_{EXT} = \frac{Q_{GATE}}{V_{GATE}}$$

The ratio between the capacitors C$_{EXT}$ and C$_{BOOT}$ is proportional to the cyclical voltage loss. It must be:

Equation 2

$$C_{BOOT} >> C_{EXT}$$

For example, if *Qgate* is 30 nC and *Vgate* is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF, the drop would be 300 mV.

If HVG has to be supplied for a long time, the C$_{BOOT}$ selection must also take into account the leakage and quiescent losses.

For example, since the HVG steady state consumption is lower than 200 µA, if HVG T$_{ON}$ is 5 ms then C$_{BOOT}$ has to supply 1 µC to C$_{EXT}$. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast-recovery high-voltage diode can be avoided (it usually has great leakage current). This structure works if V$_{OUT}$ is close to GND (or lower) while LVG is on. The charging time (T$_{charge}$) of C$_{BOOT}$ is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R$_{DS(on)}$. At a low frequency operation this drop can be neglected, but if the frequency is increased the drop must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS.

Equation 3

$$V_{DROP} = I_{CHARGE} \cdot R_{DSON} \rightarrow V_{DROP} = \frac{Q_{GATE}}{T_{CHARGE}} \cdot R_{DSON}$$

where Q$_{gate}$ is the gate charge of the external power MOS, R$_{DS(on)}$ is the ON resistance of the bootstrap DMOS and T$_{CHARGE}$ is the charging time of the bootstrap capacitor.

For example: given the typical value of 120 Ω for $R_{DS(on)}$ and using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V if the T_{CHARGE} is 6 ms. In fact:

Equation 4

$$V_{DROP} = \frac{30nc}{5\mu s} \cdot 120\Omega \approx 0.7$$

V_{DROP} has to be considered when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology does not allow a sufficient charging time, an external diode can be used.

When operating at very low frequencies, the high side driver ON time of the high-side driver can be very long. Therefore the C_{BOOT} voltage can drop because of HVG steady-state consumption. To avoid extremely large capacitors (> 1-2 µF), an external charge pump can be added (see *Figure 7* as example). It is mandatory for the diodes to have a low parasitic capacitance since C1 and C2 should be greater than the capacitance of the diodes. The oscillator has to work in order to balance the high-voltage side consumption, and the minimum frequency is fixed by the values of C1 and C2 (with C1 = C2 = 33 pF then f > 250 – 300 kHz).

Figure 6.   Bootstrap driver
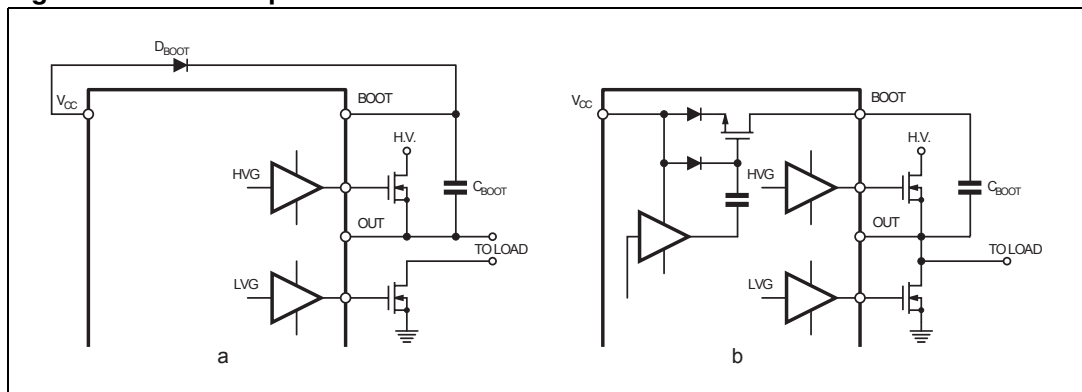
Figure 7. External charge pump
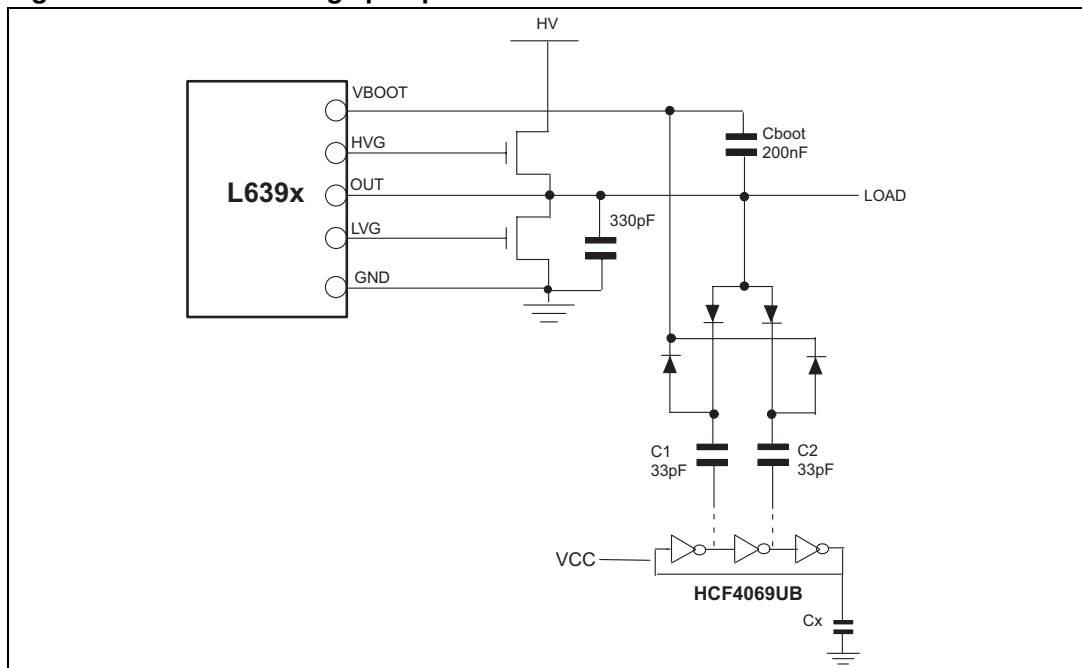
6 Application examples

6.1 Basic topology: single half-bridge

A typical schematic for one half-bridge is shown in *Figure 8*.

Figure 8.   Typical schematic of power half-bridge
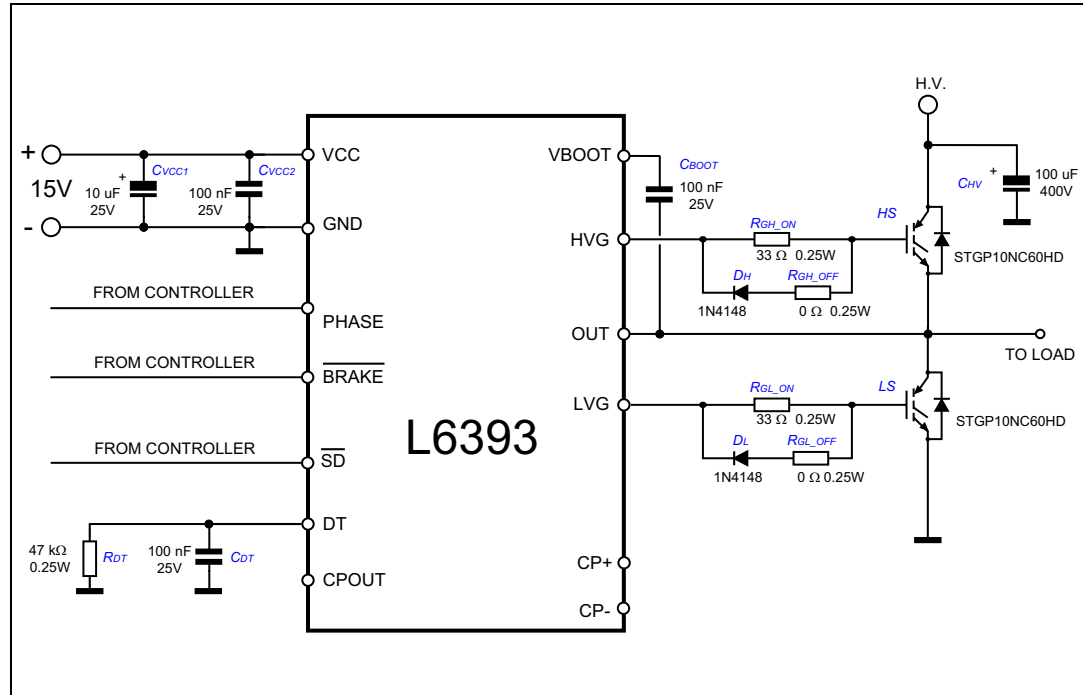
The half-bridge comprises two power switches such as IGBTs (or MOSFETs), one high-side and one low-side. When the high-side switch is ON, it brings the output voltage of the half-bridge to the HV bus voltage, which can be a high DC voltage power supply with large power availability, while the low-side switch shorts the output to the power ground voltage when it is ON. Thanks to the internal floating structure for the high-side switch driving, n-type IGBTs (or n-channel MOSFETs) can be used. The gate driver works exactly like a digital/analog-power interface between the controller and the power stage. Note that it is usually recommended (not mandatory) to have some gate resistances between each power switch gate and the corresponding gate driver output, in order to limit current during the gate charge.

6.1.1 VCC supply pin

Regarding the V_{CC} pin, a local filtering of the supply voltage very close to the L6393 IC is recommended. Generally, the suggestion is to use two capacitors, one electrolytic with a greater value (C_{VCC1} = 10 μF, for example), which has a great energy capability but also a non-negligible ESR (so is quite slow in providing the current) and a second smaller ceramic capacitor (C_{VCC2} = 100 nF) which has a lower ESR value but a lower energy capability. The first capacitor works mainly as the bulk energy storage while the second is able to supply the dynamic current spikes required by the commutations of the device, so is better for high-frequency decoupling of the IC supply voltage.

6.1.2 BOOT (floating) supply pin

To supply the high-side floating section of the gate driver, the bootstrap capacitor must be placed between the BOOT pin 14 and the OUT pin 12. For a detailed description of the proper dimensioning of the bootstrap capacitor, refer to *Chapter 5*. The capacitor must be placed as close as possible to the related IC pins. The bootstrap diode required for the charge of the bootstrap capacitor is integrated inside the L6393 device.

6.1.3 Logic input pins

The logic input pins must be connected to the controller with the guidelines provided in *Chapter 2*. If the application environment is very noisy and the logic input voltage is low (for example, 3.3 V), it can be useful to place some small RC network (not showed in *Figure 8*) in series with the logic input lines, in order to avoid false input triggering due to external noise.

6.1.4 Dead time pin

The resistance value on the DT pin must be selected as per the indications in *Chapter 4* and in *Figure 5*. It is recommended to connect a capacitor with a value of at least 100 nF between the DT and GND pins, as close as possible to the IC and with short PCB tracks.

6.1.5 Comparator

The comparator is completely uncommitted and both the two input pins are externally available. Attention must be paid to the output pin CPOUT, which is inverted with respect to the comparator inputs due to the open-drain transistor connected to the output.

6.1.6 Gate driver outputs: gate lines

The gates of the power switches and the gate driver outputs can be connected directly, but usually some gate resistors are placed in series on the gate lines in order to limit the gate current during commutations. The final target is to control the dV_{OUT}/dt of each half-bridge output and then reduce the EMI. A more detailed explanation of the mechanisms behind the dV_{OUT}/dt control through the gate resistors is provided in *Section 6.4*. The following calculations should be considered as approximated analyses of the gate charge phenomenon, and therefore, in order to obtain the proper sizing of the gate resistor, it is always strongly recommended to evaluate the resulting power bridge transitions through bench analyses.

As shown in *Figure 8*, the gate line is split into two paths, one for the turn ON (with, in the example, a gate resistor of 33 Ω) and the other one for the turn OFF, using a small signal diode as path selector. Using this specific topology, the equivalent turn OFF resistance is in a first approximation the parallel of the turn OFF and the turn ON resistances (neglecting the diode drop). In the example, the turn OFF resistance is set to 0 Ω to provide the lowest resistance path for the turn OFF of the IGBT. In fact, as explained in the two following paragraphs, low impedance on the gate driver turn OFF helps to reduce the induced turn ON phenomenon.

Regarding the layout of such gate lines, it is always strongly recommended to place the power IGBT (or MOSFETs) very close to the gate driver. It is important to reduce as much as possible the lengths of such line paths as well as the areas included in the gate circuits, because these can act as weak antennas and could catch noise from the surrounding environment. The larger these areas, the higher the gain of such undesired antenna circuits.

Figure 9.   Layout suggestions for the gate driving circuits
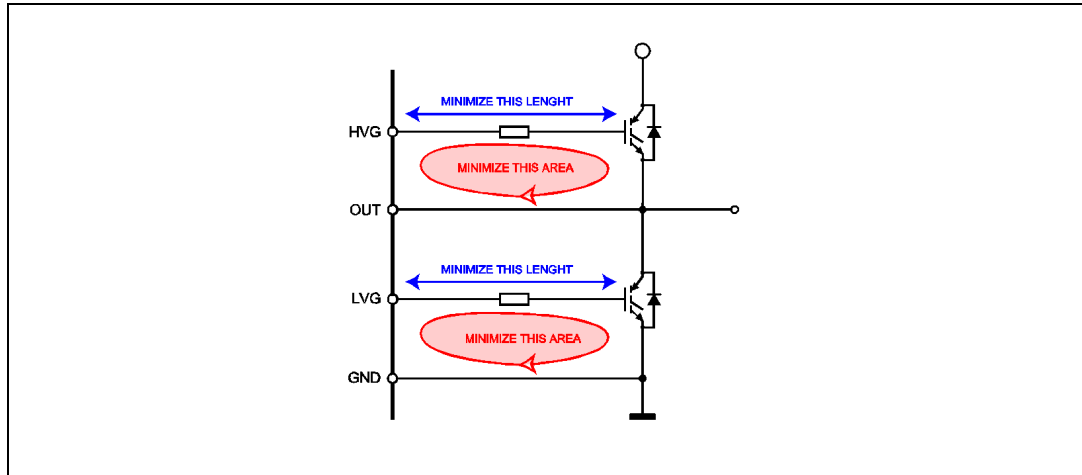
6.2   Full-bridge topology: single-phase fan motor driver

This paragraph provides a set of different example circuits using L6393 ICs for driving typical brushless single-phase permanent-magnet fan motors. The power stage topology used is full-bridge. Refer to paragraph 6.1 and 6.4 for the proper sizing of the L6393 external component.

The main purpose of the following examples is to show how such kinds of systems can be controlled without any additional microcontrollers – and make the application a complete stand-alone solution – by using the proper combination of L6393 IC gate drivers and a very limited set of external components.

6.2.1   Current mode

An application circuit with full-bridge topology controlled in current mode through two L6393 devices is shown in *Figure 10*.

Figure 10.   Application circuit for current mode FAN controller using two L6393 drivers
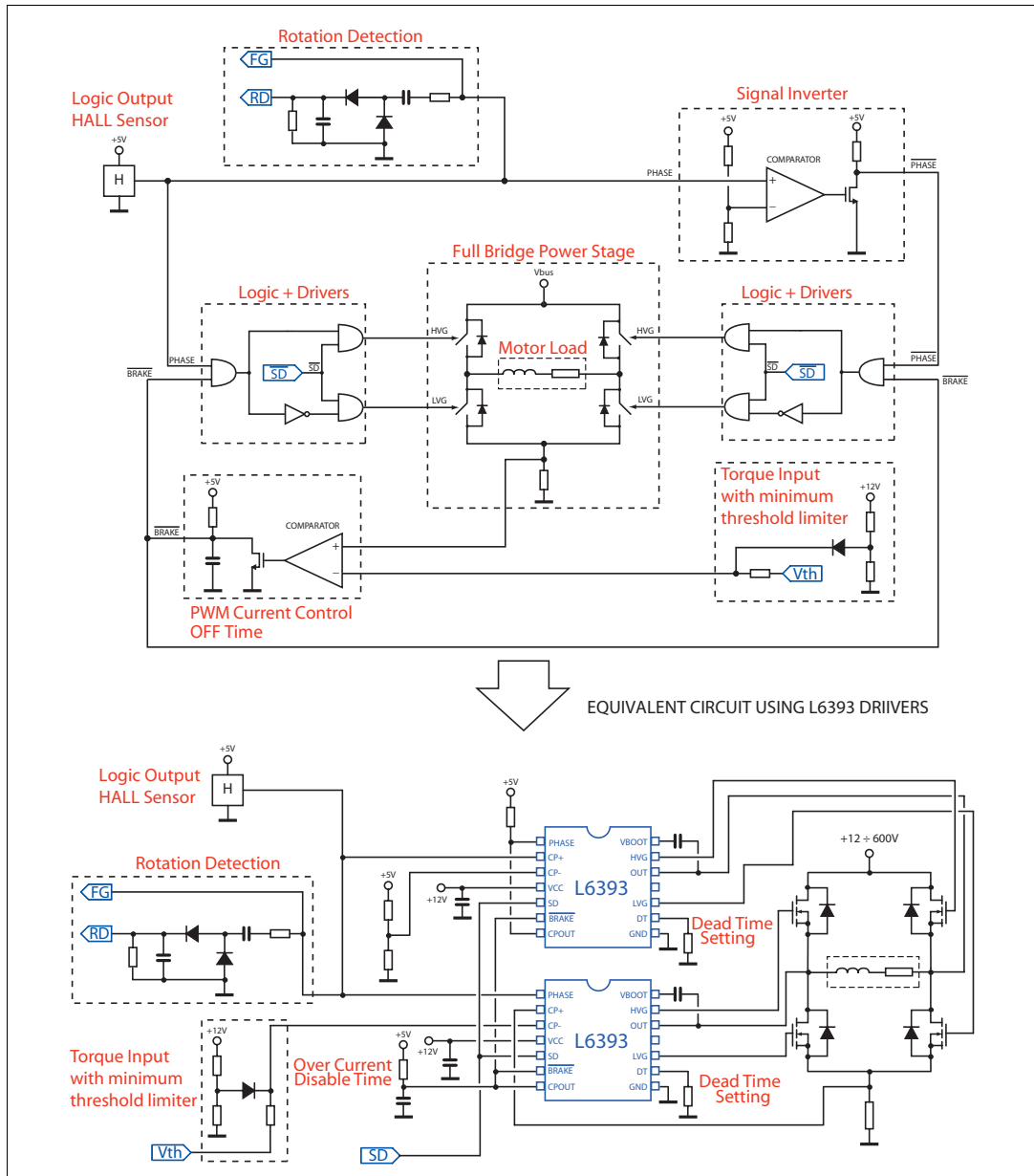
In the application circuit shown in *Figure 10*, the fan rotor position information is provided by the Hall sensor (with logic output) through a logic signal having the same frequency and the same phase of the rotor. This signal can be used to select which diagonal of the full-bridge must be turned ON starting from a certain rotor position. In fact, the targeted fan motor is a typical single-phase BLDC motor that requires synchronous driving with the rotor position. This operation is very simply implemented with the L6393 IC gate driver thanks to its logic signal management: the PHASE signal is in phase with the high-side output and in opposition of phase with the low-side output. This means that in order to turn ON a certain full-bridge diagonal the hall sensor signal can be directly fed to the PHASE input of one L6393 and the inverted signal to the PHASE input of the other L6393.

In the example of *Figure 10* the logic inversion of the hall signal is provided by a comparator which acts as a logic inverter. The comparator is directly available in one of the two L6393 drivers. The remaining comparator, belonging to the other L6393 IC, can be used as in the example to provide a PWM current control by comparing the sense voltage coming from the shunt resistor to a certain threshold voltage Vth, and by connecting the open-drain output of the comparator with both the two $\overline{\text{BRAKE}}$ inputs of the two L6393s. The analog input signal Vth is limited by the resistive divider and the small signal diode to a fixed minimum level. With this kind of current mode control, the reference signal Vth regulates directly the torque applied to the fan motor and then indirectly the speed. The type of current control obtained with this architecture is a peak current control with constant OFF time, dimensioned by the RC network on the open-drain output of the sense comparator. Note that the active pull-down of the $\overline{\text{BRAKE}}$ signal operated by the PWM comparator decreases the load current during the OFF time in "slow decay" mode, because the load is shorted by the bridge. If "fast decay" is desired, the PWM signal can be applied to the $\overline{\text{SD}}$ pins of the two drivers. *Figure 11* shows the waveform of the load current (flowing in the shunt resistor) and the Vth torque reference signal.

Figure 11. Current modulation (flowing in the shunt resistor) changing the Vth signal
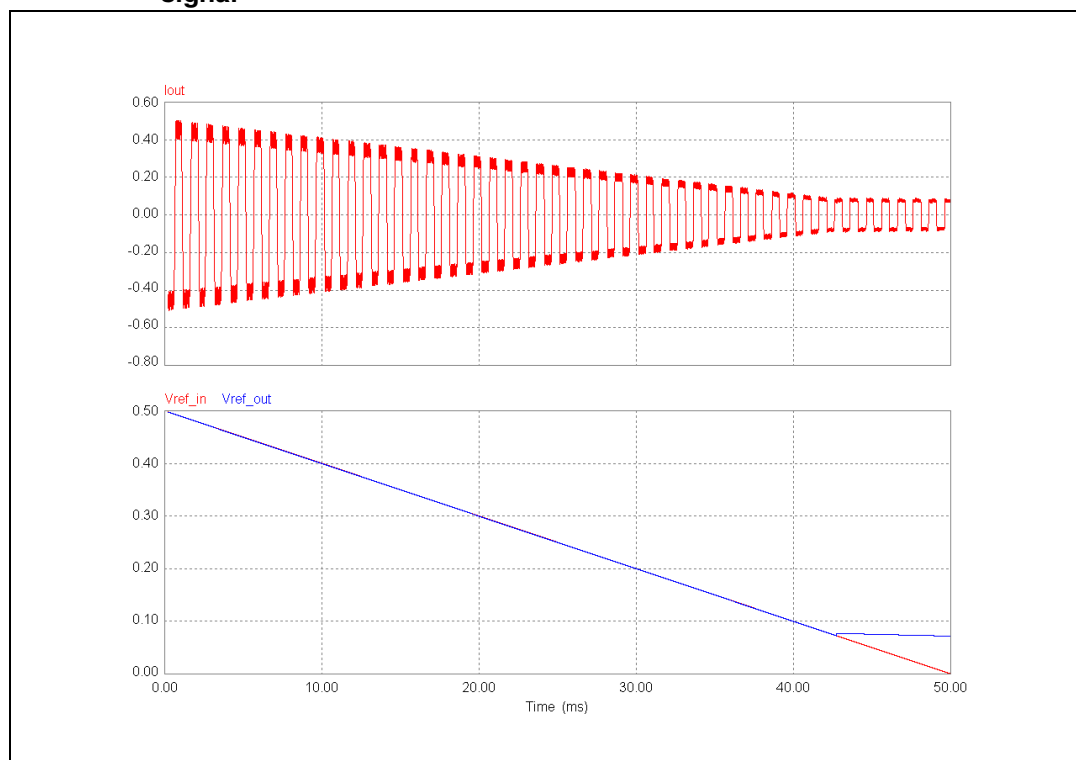
The rotation detection circuit works as a high-pass filter and can detect if the fan rotor is moving or not. In the event of a stall, the RD output goes to ground and provides information on the fan's stall condition.

Note that several different combinations of the circuitry available in the L6393 can be used. For example, if the inverted hall signal is already available (or is implemented using a small BJT or any other circuitry), the first comparator belonging to one of the two L6393s can be used for any other purpose.

6.2.2 Voltage mode - example 1

A different approach could be used to drive a single-phase BLDC fan: the voltage mode control. In the following example, an application circuit using the voltage mode approach is provided. This solution does not control the load current as in the previous circuit, but directly controls the duty cycle of the voltage applied to the load connected to the full-bridge. Additionally, the motor current is limited for protection purposes. As in the previous example, the diagonal of the full-bridge is selected by feeding the single-phase Hall Effect sensor signal directly to the PHASE input of one L6393 and the inverted signal to the PHASE input of the other L6393. Unlike the circuit shown in *Figure 10*, in this particular example the PHASE inversion is provided by a simple bipolar transistor since the two L6393 available comparators are already used for other purposes. Note that the PHASE inversion, as other analog/digital functions, can be obtained using various combinations of the features of the L6393 drivers or, where needed, some external components. The PWM voltage control is implemented using one L6393 comparator which compares the voltage coming from a triangle generator with an external voltage reference. As in the previous circuit, the external reference threshold is also limited to a minimum value by the network composed by a resistive divider plus a small signal diode (see *Figure 12*). The result of the PWM comparator is fed into the $\overline{\text{BRAKE}}$ inputs of the two L6393s. As mentioned previously, the pull-down of the two $\overline{\text{BRAKE}}$ inputs provides a "slow decay" mode for the current control, shorting the motor load through the two low sides. If "fast decay" is required, the PWM signal can be applied to the $\overline{\text{SD}}$ pins of the two drivers. The remaining comparator can be used to implement a simple over-current protection obtained by reading the shunt resistor voltage between the low sides and ground. The open-drain output of the comparator can be connected directly to the two $\overline{\text{SD}}$ pins of the L6393s so as to set to high impedance the full-bridge stage after over-current detection. The RC network on this open drain output sets a disable time after the fault detection. If over-current protection is not needed, one of the integrated comparators can be used for other purposes (such as triangle waveform generation, for example).

Figure 12.   L6393 application circuit for voltage mode FAN controller (logic output hall sensor)
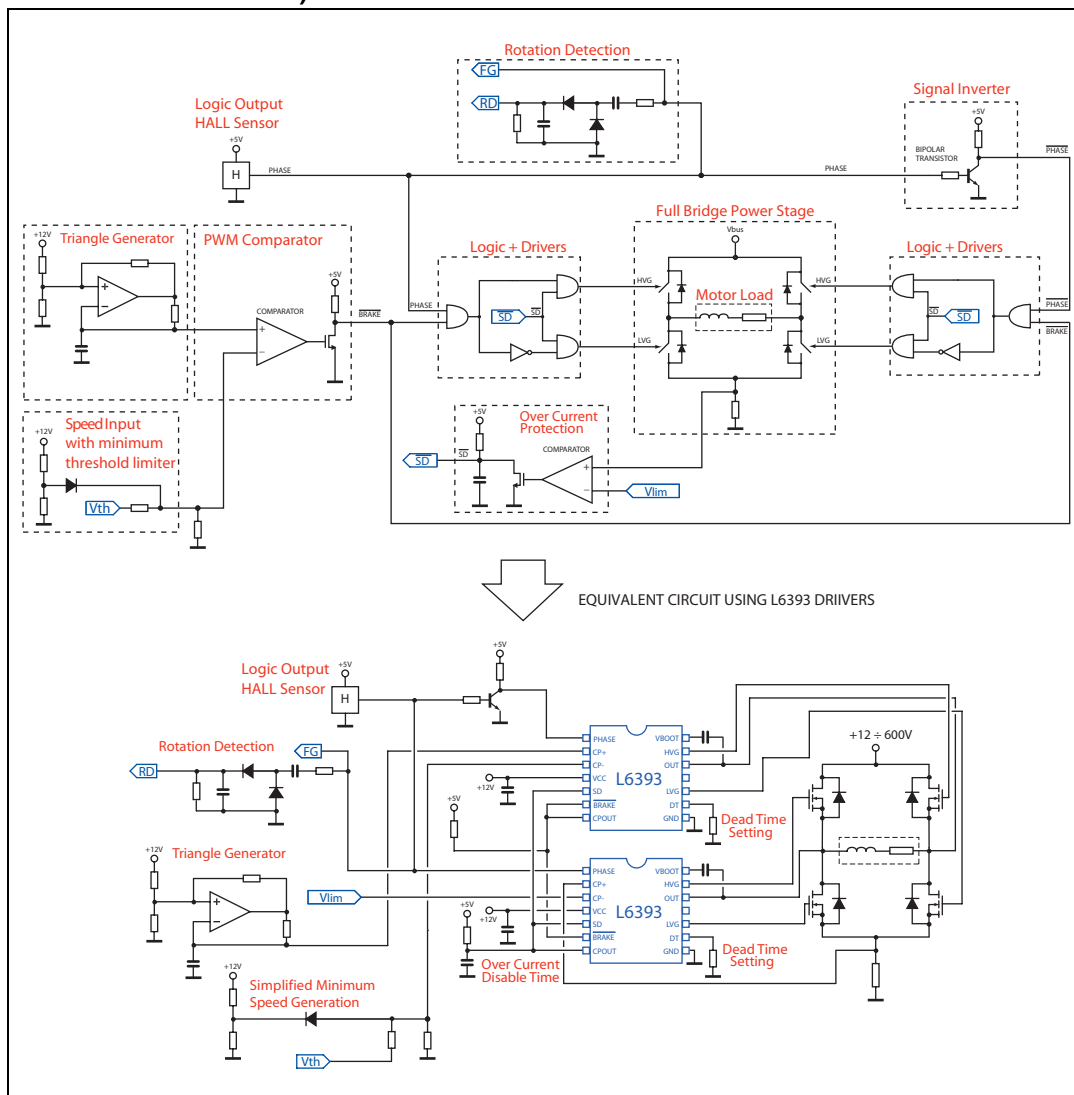
The same circuit for rotation detection as the one shown in *Figure 11* can be used in this case.

6.2.3   Voltage mode - example 2

Figure 13 provides another application of the L6393. As in the previous example, the control type is voltage mode, but the main difference is that the Hall Sensor has an analog differential linear output and it must be converted into a digital signal to be fed into the gate drivers' input logic. The conversion is provided by one comparator belonging to one of the two L6393s in the application. The other L6393 comparator is used to implement an over-current protection, similarly to the circuit shown in *Figure 12*. The remaining circuitry is similar to the previous example. In this particular case, for higher accuracy, the circuitry providing the minimum speed value is implemented using an op-amp in an ideal rectifier configuration.

Figure 13. **L6393 application circuit for voltage mode FAN controller (linear hall sensor)**
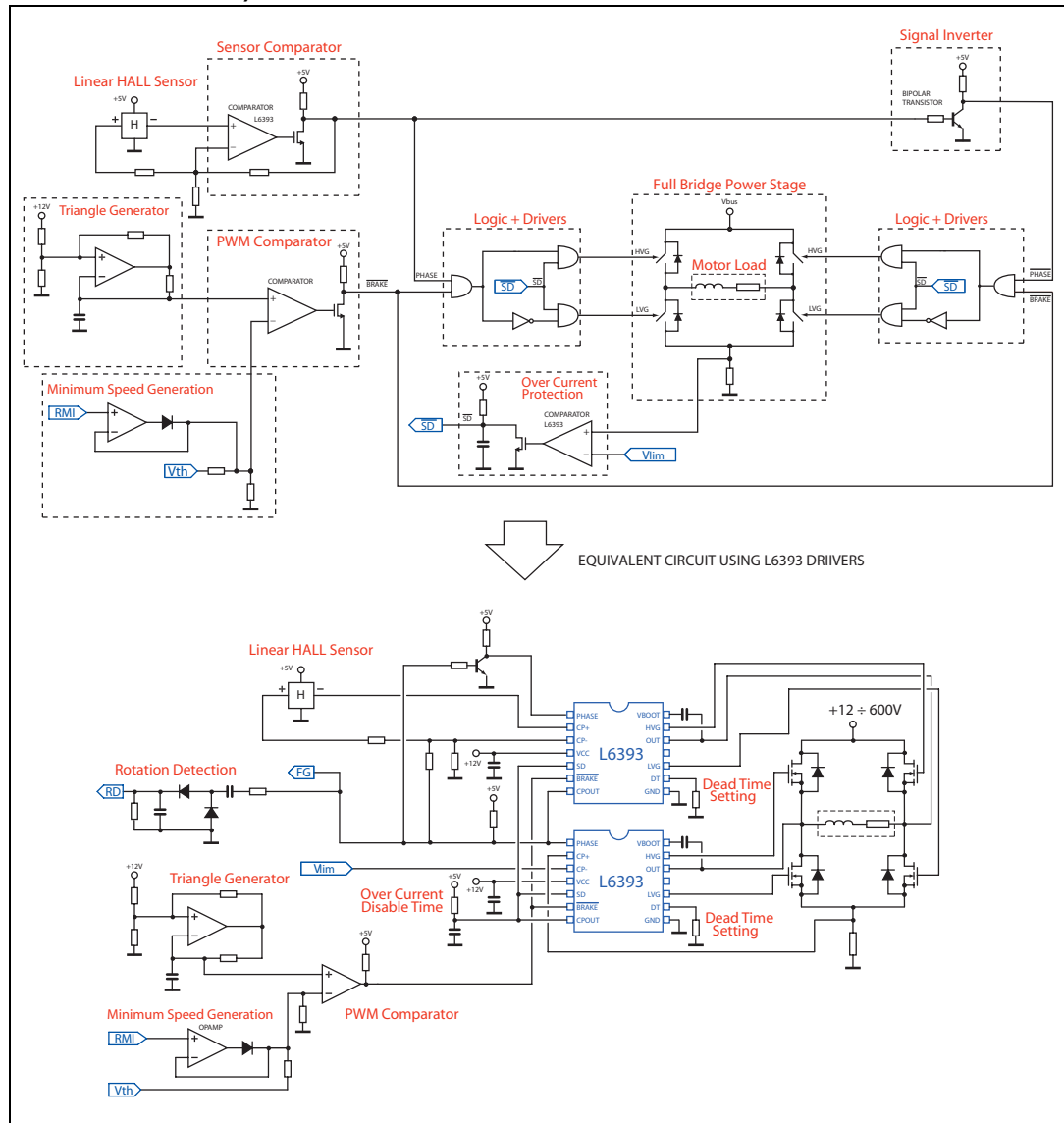
Figure 14 shows some waveforms related to the presented circuit.

Figure 14. Waveform related to the VM application circuit with linear hall sensor
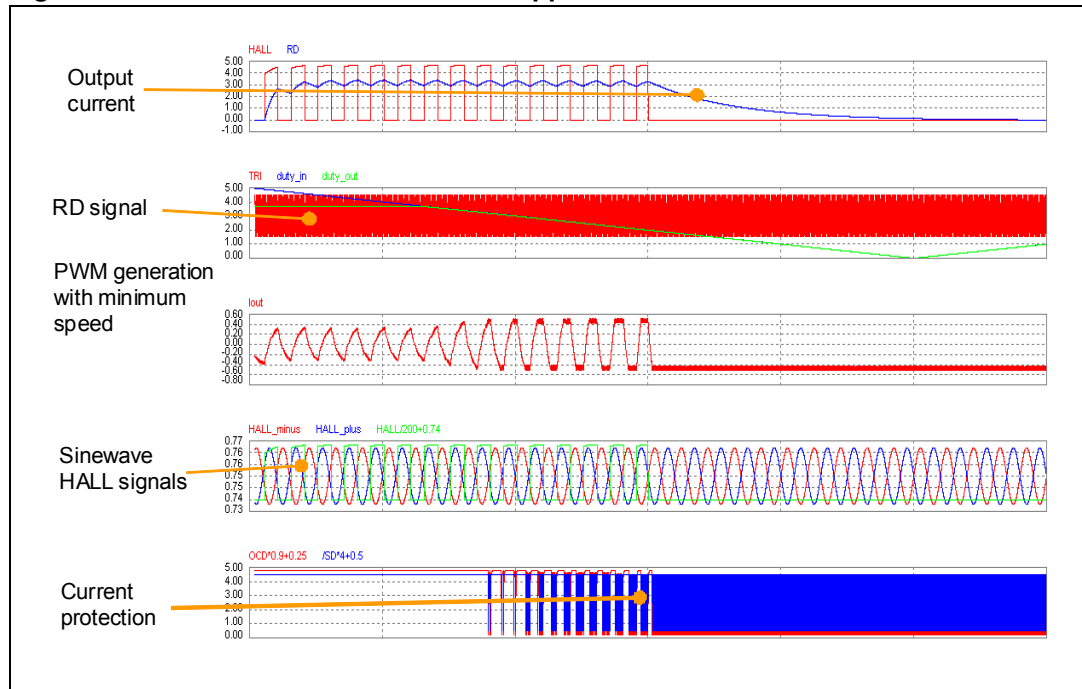
6.3 Full-bridge topology: brush DC motor driver

This section provides a further sample circuit using L6393 ICs to drive a typical brush DC motor. Again, the power stage topology used is full-bridge. Considering that the voltage mode control circuit is a simplification of the one implementing current mode control, only this last example is shown in the application circuit depicted in *Figure 15*.

The direction of the brush DC motor is selected by the DIRECTION signal, which is directly connected to the PHASE input of one driver and, once inverted, to the PHASE input of the other L6393 driver. The inversion of the PHASE signal is implemented using one L6393 comparator. The torque applied to the DC motor is controlled by the Vth signal which works as reference signal for a peak current control implemented using the other available L6393 comparator. The type of control is a peak current control with constant OFF time. It is possible to control the torque and thus indirectly also the speed of the motor, assuming that the load torque and the bus voltage remain constant.

The suggested circuit makes it possible to implement a simple brush DC motor driver using just two L6393s, a few simple passive components and a power full-bridge.

Figure 15. L6393 application circuit for brush DC motor controller (current mode)
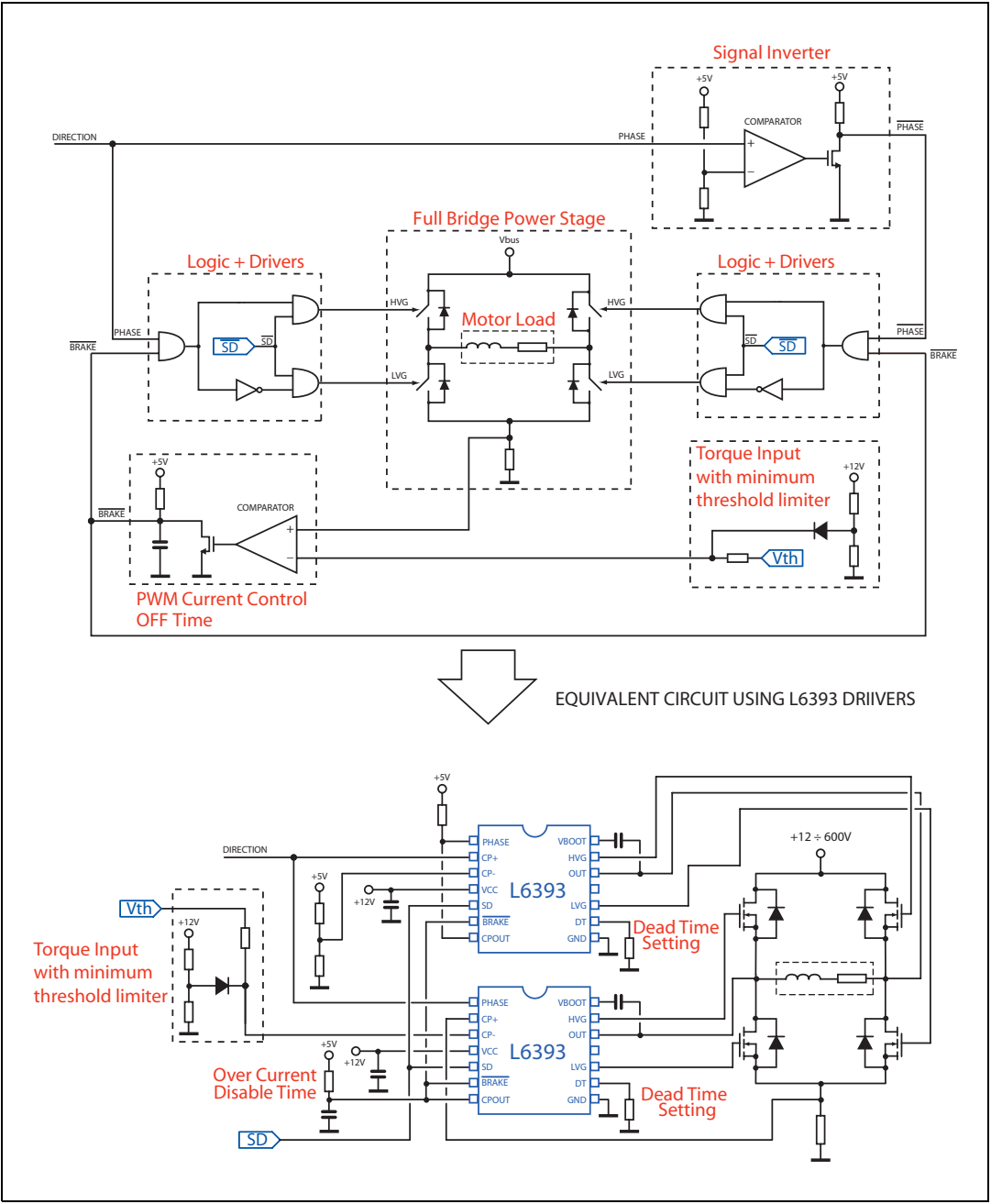
6.4 Gate driving: principle of working with inductive loads

This section provides a more detailed description of the power IGBT (or MOSFET) gate driving with inductive loads. The following explanations and calculations are only intended to provide a general understanding of the physical principles behind the phenomenon of the dV_{OUT}/dt control through the gate current limitation performed by the gate resistors. The purpose is to help the application designer using L6393 ICs to understand the various ways in which different parameters of the gate driver system act on the power transitions, and thus identify the main effects on which to focus.

Calculations and formulae should be considered as qualitative indications and not for an accurate quantitative use since, as explained in the above paragraph, they are the result of a first approximation study. The experimental verification of the design choices is always recommended.

The description distinguishes and explores the two main actors of the gate driver system: on the one hand the inner structure of the gate driver output buffers is described, and on the other hand the switching mechanism of a generic IGBT (or MOSFET) is detailed.

Figure 16 provides a simplified view of the L6393 gate driver output buffers. Each one can be considered as a CMOS push-pull stage where a p-channel MOSFET works as source driver while an N-channel MOSFET works as sink driver. The structure is similar for both the low side and the high side, and the behavior can be considered the same. In fact, the high-side driver can be thought of as a floating buffer having as supply the V_{BOOT} voltage and as reference the OUT pin. The C_{BOOT} capacitor represents the floating supply voltage source of the high-side driver. During the charge of the power switch gate, each source/sink MOSFET can be considered (in first approximation, for simplicity) as if it would be in the ohmic region, so it can be represented as an equivalent resistor with a value equal to its R_{DSon}. Thanks to this approximation, one can use a simplified equivalent circuit for the turn ON and the turn OFF commutation (see *Figure 16*). Regarding the turn ON, this gate charge circuit has two resistors in series (R_{GATE_ON} and R_{DSon_SOURCE}) and a supply voltage which is V_{CC} for the low side and Vboot-Vout for the high side. Regarding the turn OFF, the equivalent circuit is composed of just two resistors (R_{GATE_OFF} and R_{DSon_SINK}) connected to the source of the power switch.

Figure 16. Gate driver output buffers: equivalent circuit
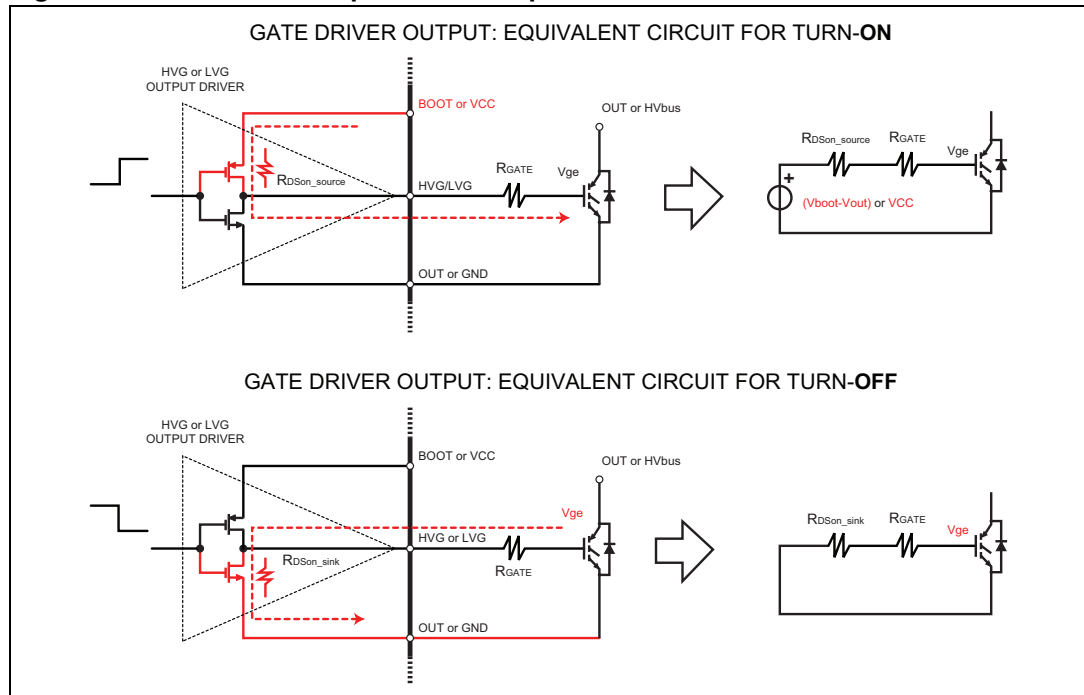
This first simplification is related to the inner structure of the gate driver circuitry. The following section focuses on the side of the power bridge and its commutations.

In a common half-bridge composed of a high-side and low-side switch, the transitions of the power IGBTs (or MOSFETs) are not all similar, but they can be distinguished into two main types: soft switching and hard switching (*Figure 17*). The key element in the dynamics of the transitions is the direction of the current flowing in the power IGBT (or MOSFET) under evaluation, which depends on the direction of the load current with respect to the half bridge. Essentially, if the current goes in the same direction as the power switch, the commutation is hard. If the current goes in the opposite direction, the commutation is soft.

Figure 17. Hard and soft switching
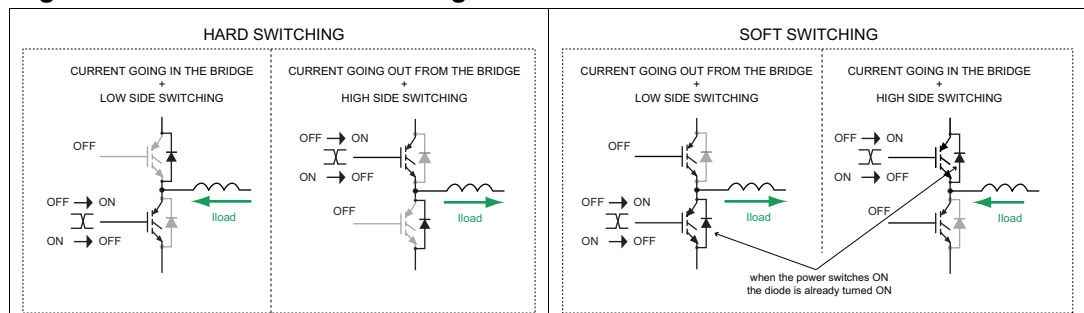
As shown in *Figure 17*, hard switching occurs when the high side is commutating and the load current is outgoing from the bridge or when the low side is commutating and the load current is ingoing to the bridge. This type of transition is called hard because the power switch turns ON when the related Vce (Vds) is at the maximum; Vce (Vds) goes back to the maximum during turn OFF (Vce is close to zero while the switch is steadily ON): the transition is completely managed by the switch that, during the commutation, dissipates energy.

On the other hand, if the switch turns ON when its Vce is already close to zero or Vce keeps staying close to zero after turn OFF, the transition is soft and, during the commutation, the switch dissipates almost no energy. This last condition occurs when the free-wheeling diode of the switch is bringing the current because the diode is in the same direction as the load current.

As a general rule, one should consider that the dynamics of the transition (dV_{OUT}/dt, Vce rise/fall time etc.) is always managed and controlled by the power switch in hard switching, while its companion switch is necessarily in soft switching (because it is in the opposite direction with respect to the load current). Considering this and in order to understand the mechanism of the power IGBT (MOSFET) transition, the hard switching transition is further described below. Note that all of the following descriptions always consider an inductive load connected to the half-bridge stage output.

Figure 18 depicts the dynamics of the hard switching for the turn ON transition.

The first graph is related to the gate charge curves of the power IGBT (or MOSFET). This is a typical graph available in the datasheet of every IGBT or MOSFET, and describes the dependence of the amount of charge required by the IGBT gate on the voltage drop between the gate and the emitter (or source). The second graph shows the collector current (Ic) and Vce voltage versus time. The third graph shows the working point of the IGBT traced on the various Ic vs. Vce characteristic curves for different Vge voltages. For a single turn ON transition, four main phases related to the power IGBT (MOSFET) commutation can be distinguished. On the left side of *Figure 18*, the IGBT conditions for each phase are described. During phase T1, the gate begins to be charged, but the power IGBT is still not conducting because Vge is below the IGBT threshold. In this state the IGBT current is zero and its Vce is at the maximum, while Vge is gradually increasing. In phase T2, the Vge voltage goes above the IGBT threshold and the IGBT starts to bring part of the load current, while Vce remains fixed at the maximum level because the free-wheeling diode of the companion IGBT is still bringing the rest of the load current, and therefore is still in conduction, clamping in this way the Vce voltage. Both in T1 and T2 phases, the gate current contributes to charge the equivalent Cge parasitic capacitance of the IGBT. In the Ic vs. Vce characteristic plot, the T2 phase is the vertical section of the working curve trace, because the IGBT is moving on its own characteristic with a constant Vce and an increasing current, while its Vge is increasing too. When the amount of current flowing in the IGBT is equal to the load current, the diode turns OFF and the Vce voltage starts to decrease because it is no longer clamped by the free-wheeling diode of the other IGBT. The working point on the Ic vs Vce curve reaches the Iload value and starts to move horizontally on the Ic constant curve in the direction of the decreasing Vce voltages. This is the T3 phase, usually called *plateau* phase. This name comes from the fact that the gate charge curve is horizontal for the whole T3 phase, until Vce reaches the Vce_sat value corresponding to the Iload current. Note that the Vge voltage is constant although the gate current flowing in the IGBT gate is not zero: the reason is that the whole gate current is used to charge the Cgc (Miller) parasitic capacitance which then experiences a dV/dt on its terminals because the Vce voltage is decreasing after the diode turn OFF. In a first approximation, if the Cgc was constant (it is actually not), the dV_{OUT}/dt could be calculated as follows:

$$\left(\frac{dV_{OUT}}{dt}\right)_{FALL} = \frac{I_{SOURCE}}{C_{GC}}$$

The above formula shows that the source current coming from the gate driver can directly control the dV_{OUT}/dt of the power half-bridge. This calculation is just a first approximation since, typically, the Cgc miller capacitance value is not constant but depends on the Vce voltage: Cgc is not linear. The main effect of the Cgc's abrupt variation is that the actual slope of the out transition is composed of two different dV_{OUT}/dt slopes, one faster and the other slower (with respect to the value obtained by the above formula). See *Figure 18*. In this document, only the first approximation approach will be used.

Figure 18. Turn-ON hard switching details with induction load: gate charge and plateau phase
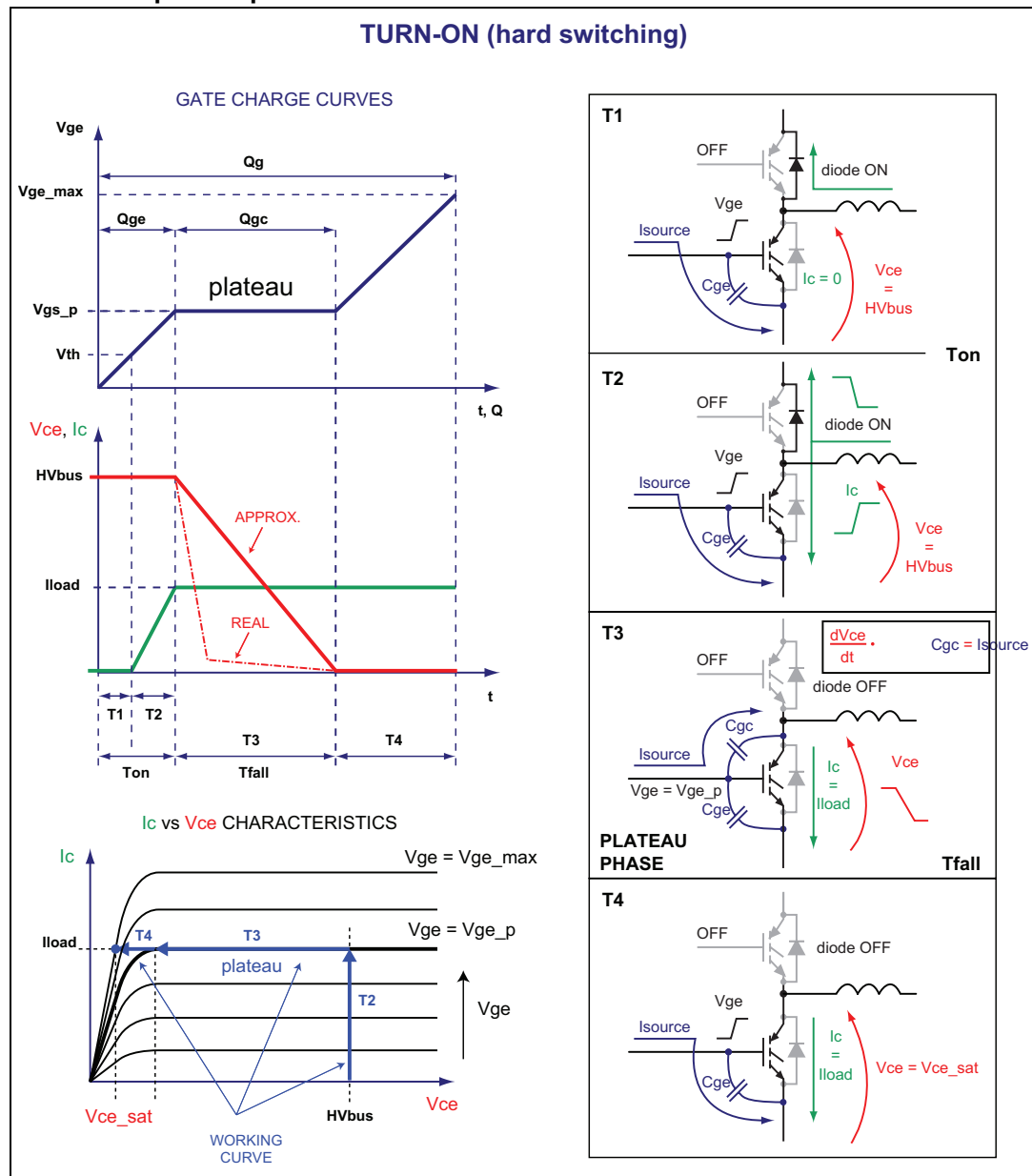
Due to the Cgc's non-linearity the IGBT (or MOSFET) datasheet also reports the equivalent total amount of charge required during the different gate charge phases: the total gate charge Qg required for turning ON the IGBT (or MOSFET) completely, the Qge required for increasing the Vge up to the plateau voltage and the Qgc required during the whole plateau phase. This last amount of charge is also called plateau charge. The time required to provide the complete plateau charge is the Tfall time and this is the same time necessary for completing the Vce transition. For Ton time is intended the time delay between the beginning of the gate charge and the full conduction of the IGBT (or MOSFET), when the power switch current equals the full load current. So:

$$T_{FALL} = \frac{Q_{GC}}{I_{SOURCE}}$$

It is now possible to merge the equivalent gate driver output circuit reported in *Figure 16* and the considerations about the different gate charge phases in the total equivalent circuit reported in *Figure 19*.

Figure 19.   Total equivalent circuit for turn-ON
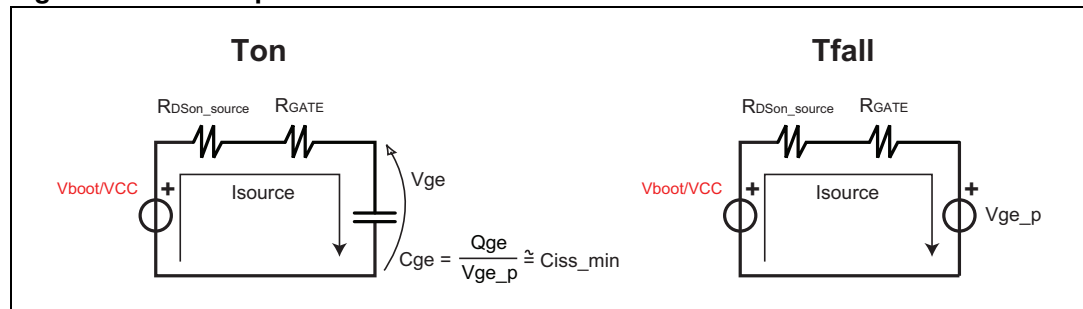
From the above circuit the value of the transition times could be calculated (the following formulae are related to the low-side transition, but the same are also suitable for the high-side by changing "VCC" with "V_{BOOT}-V_{OUT}").

$$T_{ON} = \left(R_{DSon\_source} + R_{GATE}\right) \cdot C_{ISS\_min} \cdot \ln\left(\frac{VCC}{VCC - Vge\_p}\right)$$

$$T_{FALL} = \frac{Q_{GC}}{I_{SOURCE}} = Q_{GC} \cdot \frac{\left(R_{DSon\_source} + R_{GATE}\right)}{VCC - Vge\_p}$$

CISS_min is used because when the Vce (or Vds) of the power IGBT (or MOSFET) is maximum (equal to HVbus), the CISS (which depends on the Vce) shows its minimum value.

During the turn-OFF of the power IGBT (or MOSFET), the behavior is the same as for the turn-ON but in reverse time order. *Figure 20* provides the gate charge characteristics and Vce vs. Ic curves.

Figure 20.   Turn-OFF hard switching details with induction load: gate charge and plateau phase
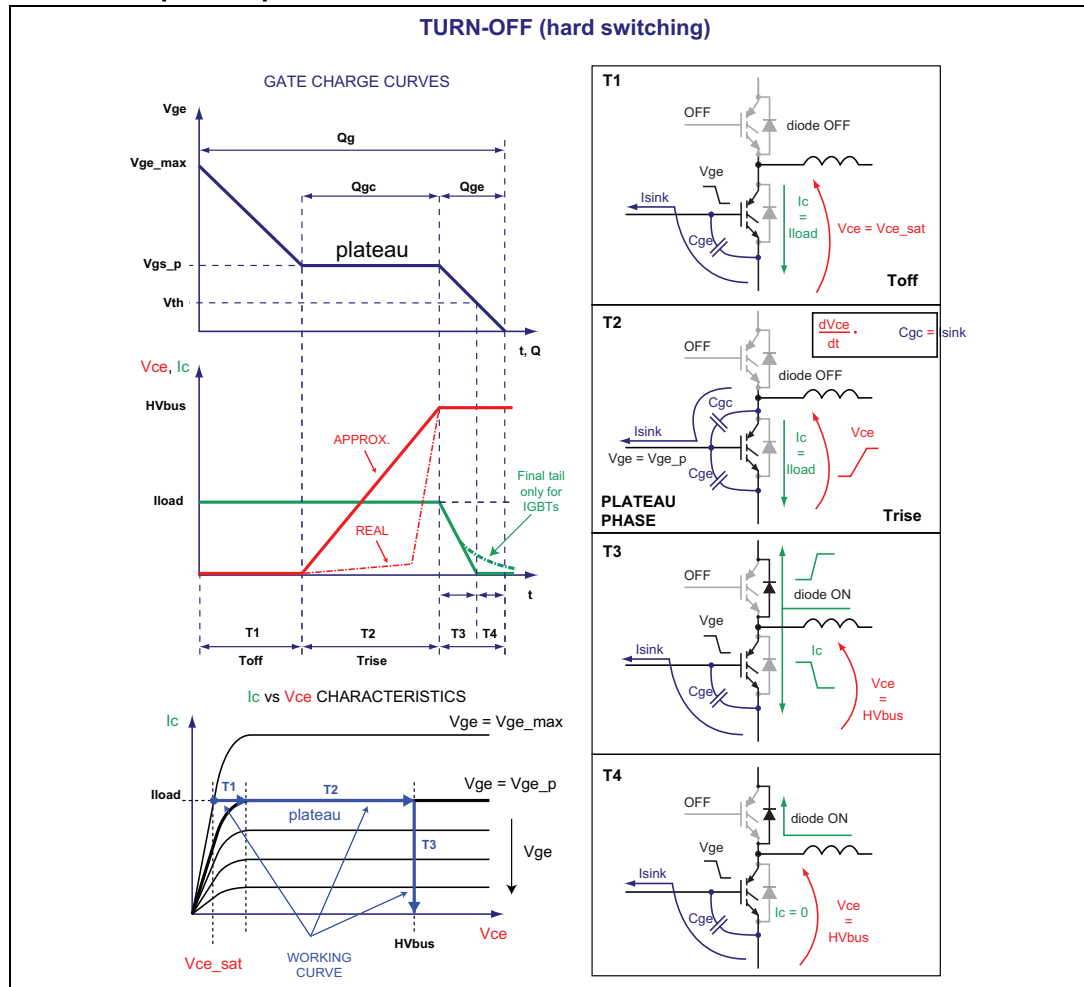
The rising dV_{OUT}/dt and Trise can be calculated as follows.

$$\left(\frac{dV_{OUT}}{dt}\right)_{RISE} = \frac{I_{SINK}}{C_{GC}}$$

$$T_{RISE} = \frac{Q_{GC}}{I_{SINK}}$$

As discussed above the equivalent gate driver output circuit can be represented as in *Figure 21*.

Figure 21. Total equivalent circuit for turn-OFF
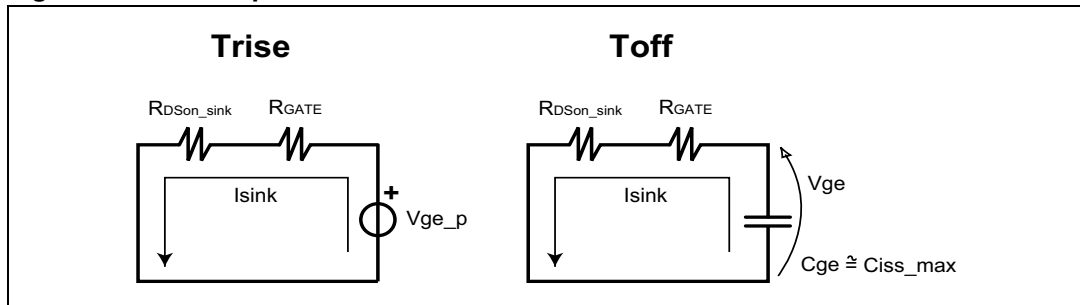
Given the equivalent circuits in *Figure 21* and the approximations on the power IGBT's (MOSFET) switching behavior, the timings are the following.

$$T_{OFF} = \left(R_{DSon\_sink} + R_{GATE}\right) \cdot C_{ISS\_max} \cdot \ln\left(\frac{VCC}{Vge\_p}\right)$$

$$T_{RISE} = \frac{Q_{GC}}{I_{SINK}} = Q_{GC} \cdot \frac{\left(R_{DSon\_sink} + R_{GATE}\right)}{Vge\_p}$$

As above, CISS_max is used because when the Vce (or Vds) of the power IGBT (or MOSFET) is minimum (equal to Vce_sat), the CISS (which depends on the Vce) shows its maximum value.

Even if they are just approximations, Tfall and Trise are very important values to be estimated because they provide an indication about the power dissipation during the switching of the power IGBT (or MOSFET), which can be approximated as indicated in *Figure 22*.

Figure 22.   Power dissipation during switching (approximation)
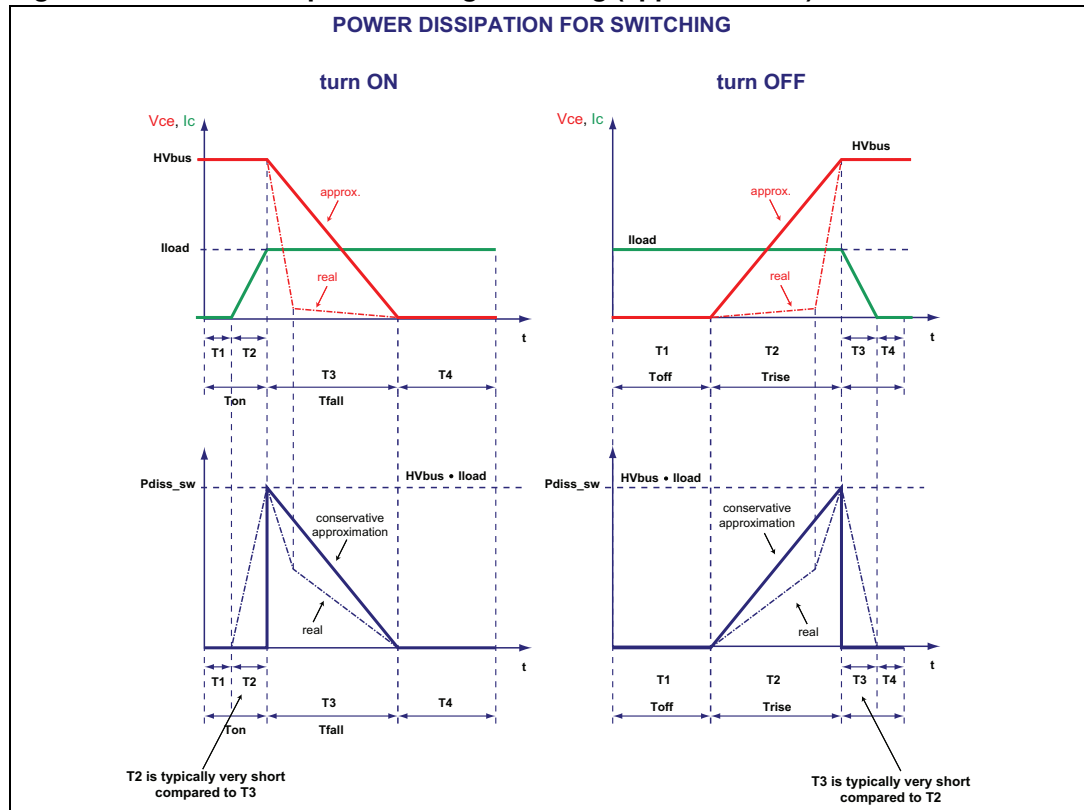
Since the T2 time for the turn ON and T3 time for the turn OFF are much shorter compared to respectively Tfall and Trise, the approximated instantaneous amount of energy dissipated during the commutation can be calculated as the triangular area having as base the Tfall or Trise time, and as height the product between the maximum Vce voltage (equal to HVbus) and the Iload current value, as follows:

$$E_{DISS\_SW} \cong \frac{(HV_{BUS} \cdot I_{LOAD}) \cdot (T_{FALL} + T_{RISE})}{2}$$

$$P_{DISS\_SW} \cong \frac{(HV_{BUS} \cdot I_{LOAD}) \cdot (T_{FALL} + T_{RISE}) \cdot f_{SW}}{2}$$

The term f_{SW} represents the switching frequency of the power IGBT (or MOSFET).

In summary, using the results obtained by these approximated calculations, it is clear that the main consideration when dimensioning the gate resistor values is the trade-off between the electromagnetic emissions and the power dissipated during power IGBT (or MOSFET) switching, as shown in *Figure 23*.

Figure 23.   Rgate dimensioning criteria
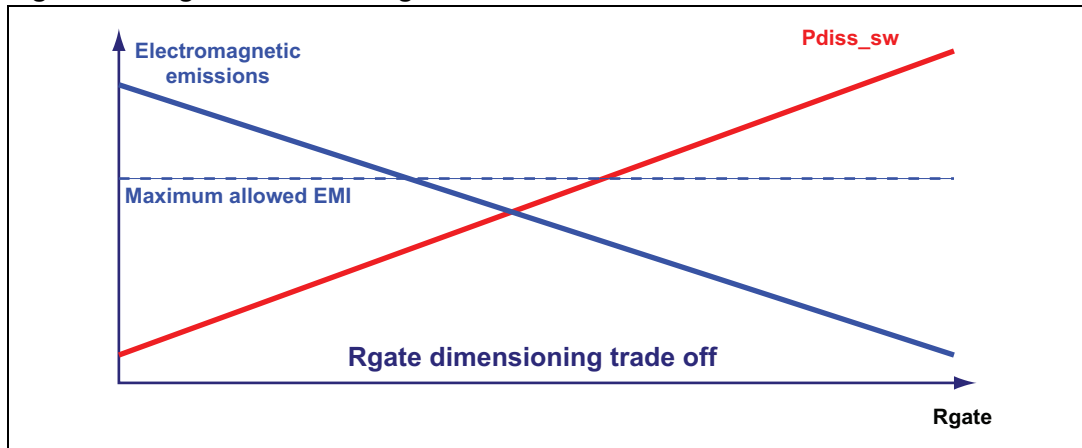
Rgate has an influence on the power dissipation on the one side and on the EMI effects on the other side, therefore the best trade-off must be chosen during the application's design-in phase.

7 Induced turn-on phenomenon

One possible phenomenon to be analyzed is the induced turn ON that could happen on a turned OFF power IGBT (or MOSFET) when its companion on the same half-bridge is switching on. This phenomenon is due to the current injected on the gate by the Miller parasitic capacitance (Cgc), which causes an undesired voltage increase on the gate of the power IGBT (or MOSFET) which should be kept well turned OFF. Induced gate voltage depends on the absolute value of the parasitic capacitance Cgc, its relative ratio with Cge, the value of the dV_{OUT}/dt of the half-bridge and the valu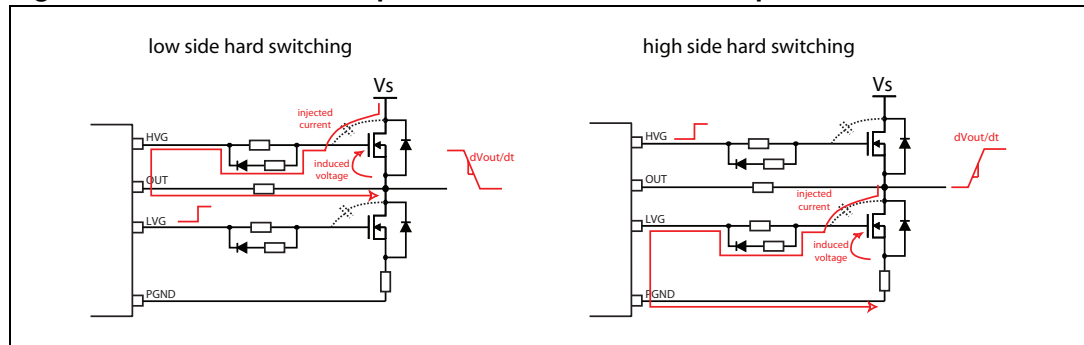e of the equivalent (turn OFF) resistance between the emitter (or the source) and the gate. *Figure 24* shows this phenomenon.

Figure 24. Induced turn ON phenomenon - circuital description

Note that typically the induced turn ON phenomenon does not cause a complete turn ON of the power MOSFET, so it is hard to have a destructive cross-conduction on the half bridge during commutations. Nevertheless, a weak conduction of the opened power switch might increase the power dissipation of the power stage, increasing then the overall temperature of the power MOSFETs and reducing the efficiency. This is the reason why this phenomenon deserves particular attention also in terms of thermal performances of the power application.

This phenomenon could be reduced in the following ways.

a) By reducing the resistance path between the gate and emitter (source). Reducing as much as possible the gate resistance in which the injected current flows results in a lower voltage drop on the gate. The drawback could be an increase of the dV_{OUT}/dt during the turn OFF of the power IGBT (or MOSFET) which commutates in hard-switching and then an increase of the electrical noise and EMI issues (as explained in the previous paragraph the power IGBT or MOSFET in hard-switching is always the one which has the channel in the same direction as the current). On the other hand, the dVout/dt during turn OFF is usually lower than the one during turn ON because the plateau voltage is closer to the source voltage than the supply voltage of the driver, resulting in a lower gate current for the discharge of the gate charge.

b) By reducing the maximum dV_{OUT}/dt. This reduction can be achieved by increasing the gate resistor value that limits the gate current for the turn ON of the power MOSFET. The drawback is a consequent increase of the switching time, which means dissipating more power during commutations.

c) By using a MOSFET/IGBT with a lower Cgd/Cgs (or Cgc/Cge for IGBTs) ratio. This solution is not always the easiest, but it could be the best strategy when the induced turn ON phenomenon is dominant.

8 How to increase the gate driver output current capability

In some cases, certain applications may require more gate driver output current capability. This requirement can be found in systems where the power rating is higher than approximately 1 kW. In such applications in fact, typically the power MOSFET/IGBTs have a big gate charge which contributes to slow down the power switch transition (the dV_{OUT}/dt), increasing the power dissipation during each commutation. Note that also in applications with power ratings higher than 1 kW, the output current capability of the L6393 may be enough if the power dissipation for commutation is acceptable (the power dissipation due to RDSON or VCESAT is not dependent on the gate current). However, if the limitation of such power contribution is a constraint, the dV_{OUT}/dt of each transition must be increased by enhancing the current capability of the gate driver.

A simple way to increase the current capability of the gate driver outputs is to insert, in series with the two gate lines of one half-bridge gate driver IC, two external current buffers (*Figure 25*).

Figure 25. Block diagram of output current capability enhancement using external current buffers
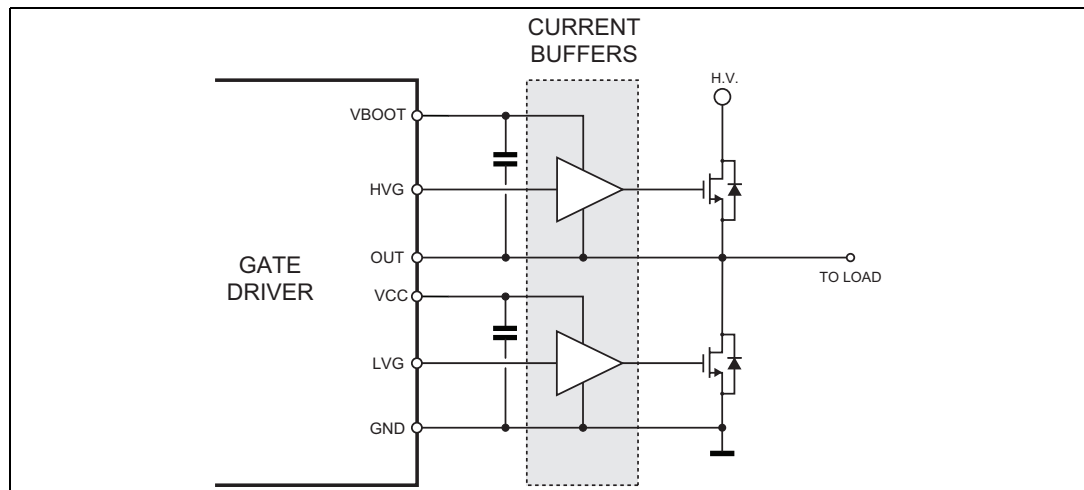
Typically, the current buffers are implemented using bipolar NPN-PNP push-pull non-inverting (emitter follower configuration) structures. *Figure 26* shows a typical circuit using a gate driver with bipolar push-pull current buffers.

Figure 26. Example of a gate driving circuit with current buffers to increase current capability
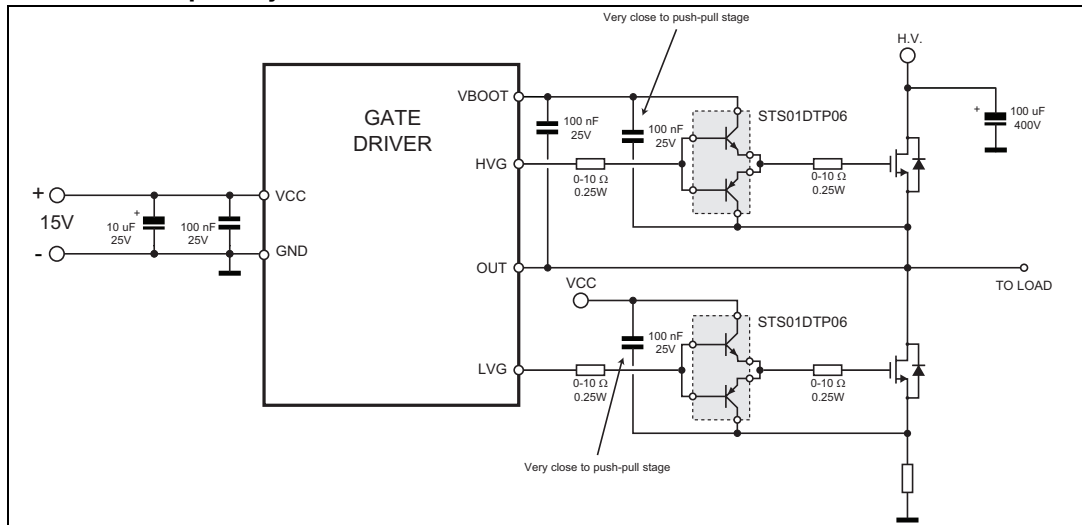
In the example above, the ST devices STS01DTP06 are dual NPN-PNP complementary bipolar transistors rated for 1 A current and available in the small SO-8 package. The two push-pull structures are placed on each gate driving path and must be provided with a decoupling capacitor very close to the device pins (as shown in *Figure 26*).

9 Below-ground voltage on the OUT pin

A typical phenomenon found in a great number of power applications is the below ground voltage experienced by the OUT pin that can sometimes be very high. Contrary to popular belief, the real problem in the below-ground voltage is not in the maximum absolute value of the OUT pin, rather the voltage on BOOT pin and the over-charging of the bootstrap capacitance. This paragraph explains in detail the root causes of the below-ground voltages and describes actual issues that could result from the phenomenon.

9.1 Below-ground voltage phenomenon

In power applications that use half-bridge topologies and typically driving loads with a significant inductive component, the output of the power half-bridge systematically experiences a below-ground voltage transition, which can be seen in a dynamic contribution as a greater undershoot spike and in a static contribution as a below-ground static voltage with lower absolute value (*Figure 27* b). This phenomenon happens when the bridge carries out a so-called hard-switching transition towards the low voltage level and the load current is outgoing (from the bridge to the load): when the high-side switch turns off, the output current tends to remain quite constant due to the inductive component of the load, and then has to flow through the low-side freewheeling diode, which turns on going from a high-voltage reverse condition to a forward condition. It is evident that until the output bridge voltage has not reached the "zero" value, the diode is turned off, so the output transition is dominated by the high-side turn-off commutation. After the output voltage reaches a zero voltage level, the diode can turn on and it begins to bring the whole load current in a very brief time, so the high dI_F/dt causes the well-known forward peak voltage, which is the main contribution to the undershoot spikes. Other contributions to dynamic below-ground voltage are the spikes due to the high dI/dt experienced by the parasitic inductances in series with the free-wheeling diode located along the turn-off current path of the half bridge (*Figure 27*).

Figure 27. Below-ground voltages in L6393
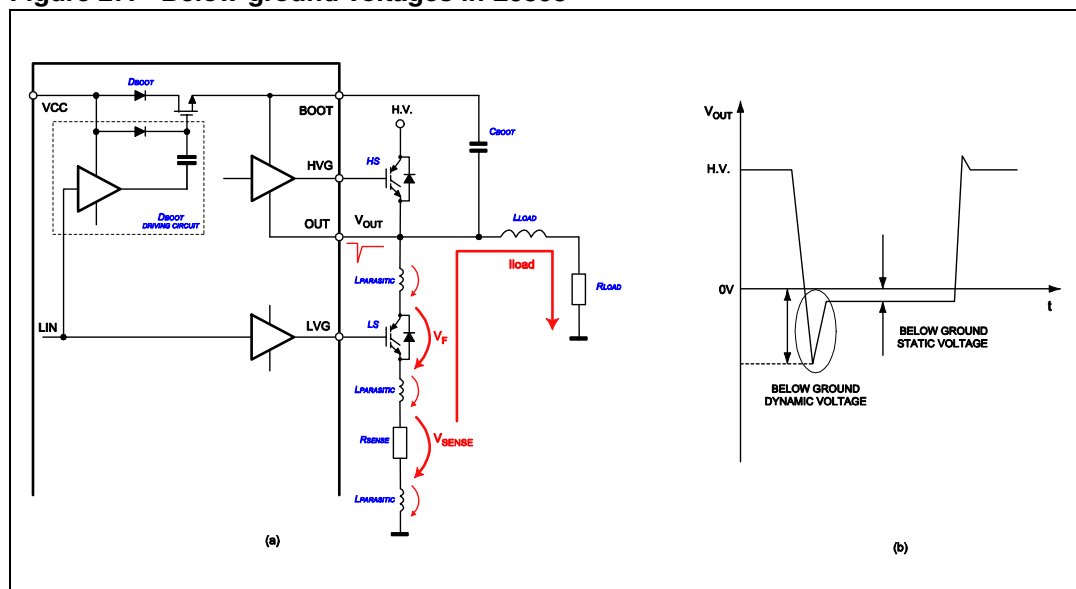
The overall below-ground voltage on the OUT pin can be calculated as follows.

**Equation 5**

$$V_{OUTmin\_static} = -(R_{SENSE} \cdot I_{LOAD} + V_F)$$

Equation 6

$$V_{BGV\_spike} = \underbrace{V_{FPK} + L_{PARASITIC} \cdot \frac{dI_F}{dt}}_{\text{dynamic contribution}} + \underbrace{V_{OUTmin\_static}}_{\text{static contribution}}$$

Where:

- V_{FPK} is the free-wheeling diode transient peak forward voltage; it depends mainly on the device technology and on the dI_F / dt of the current in the diode. Typical values may range from some volts to more than 10 V. *Figure 28* shows the VFP vs. dIF/dt of the STTH1L06 diode.

- dI_F / dt is the current slope in the low side IGBT/MOSFET and may have a value from some tens to some hundreds of A/µs. Its value depends mainly on the power switch characteristics and in part on the driving current.

- $L_{PARASITIC}$ represents the sum of all parasitic inductances on the current path and mainly depends on the PCB layout. In general, during the design of the power application it is important to pay attention to the layout of the power bridges in order to limit this parameter. Typical values of a good layout are in the order of some tens of nH. Note that it is also useful to use R_{SENSE} resistors with low parasitic inductance for the same reason.

- $R_{SENSE} * I_{LOAD}$ product is the value of the V_{SENSE} voltage and is typically less than 1 V, also for thermal dissipation issues on the same resistor.

- V_F is the forward voltage of the free-wheeling diode and is usually less than 2 V.

Figure 28.   Transient peak forward voltage vs. dI$_F$/dt of STTH1L06 diode
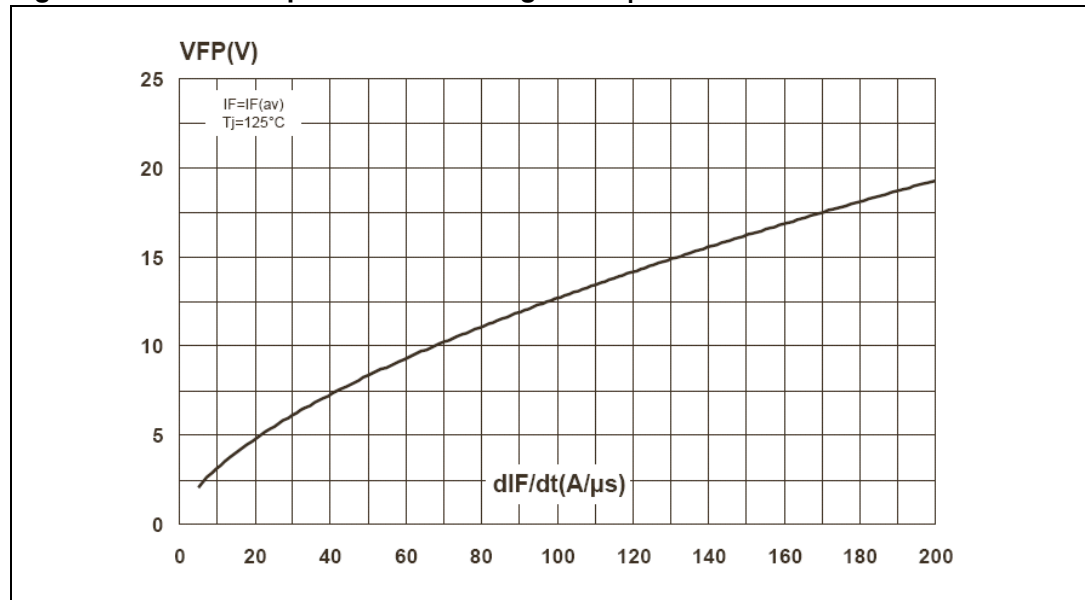
9.2 How to reduce the below ground spike voltage

In order to reduce the below ground spike, the following action should be taken:

● Reduce the parasitic inductances (see *Figure 27*).

● Reduce the dI_F/dt by slowing down the turn-off of the high side IGBT/MOSFET.

In most of application the two previous strategies result to be enough to reduce properly the below ground spike voltage, increasing the robustness of power system and then the margin for safe operation of the application. On the other hand in some cases, where the below ground spike voltage is significantly higher, the above suggestions may be not sufficient to limit that value and then it could be useful to add some external components to improve further the noise robustness of the power stage section:

● Add a small resistor (2÷10 Ω typically) in series to the OUT line (see *Figure 29*). The series resistor has the positive effect of limiting the spike voltage on the BOOT pin, thanks to the filtering effect of such resistor coupled with the bootstrap capacitor. Note that, in order to obtain an effective filtering effect, the OUT resistor must be placed between the minus terminal of bootstrap capacitor and the output of the power stage, as indicated in *Figure 29*.

Figure 29.   Use of OUT resistor to limit the below ground voltage spike on OUT pin
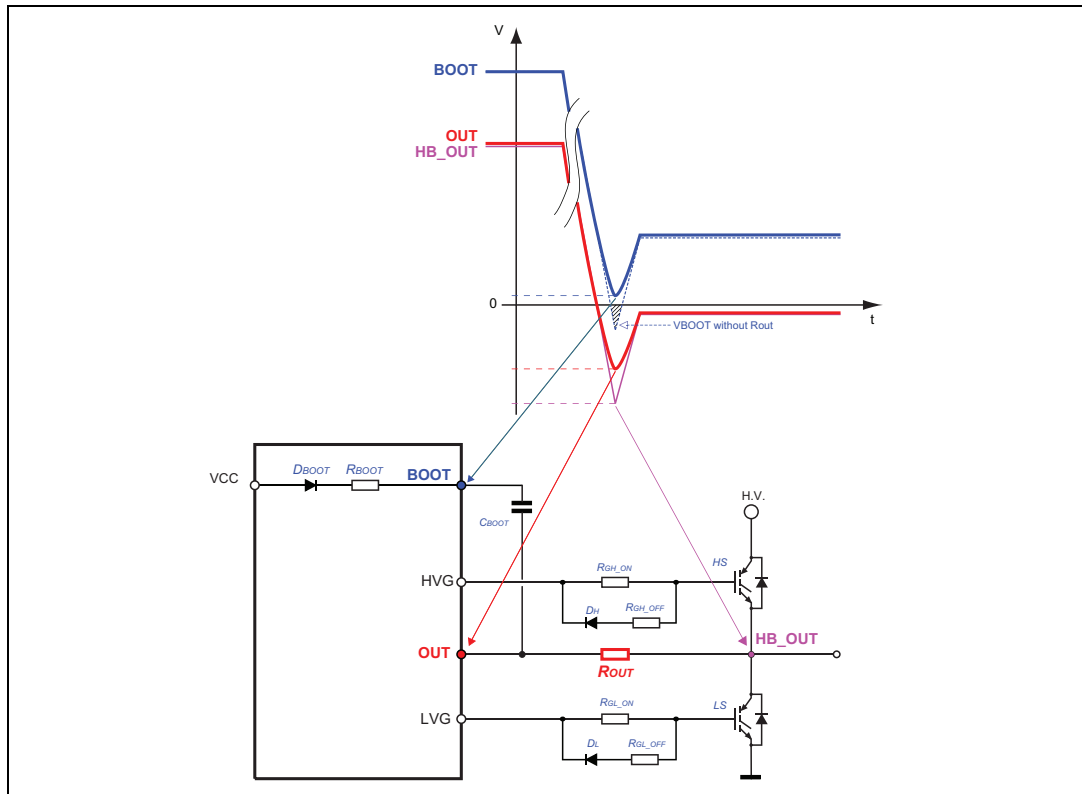
Note that this resistor is in series with both the turn ON and the turn OFF path, so it must be considered in the sizing of overall turn-ON and turn-OFF resistance.

In case neither the OUT resistor would not be enough to limit the below ground voltage, the following final resolving action could be taken:

● Add a high voltage fast diode (e.g. STTH1L06) between the GND pin and the OUT pin (very close to the device pins) in order to clamp directly on the gate driver OUT pin the below ground voltage spike. Note that, in any case, this diode must be used together with the OUT resistance suggested in the previous tip, because it must be avoided that the diode brings the very large load current during low side recirculation, in order to increase the clamping action of the diode itself (see following *Figure 30*).

Figure 30. Use of combination of OUT resistor and OUT diode to limit the below ground voltage spike on OUT pin
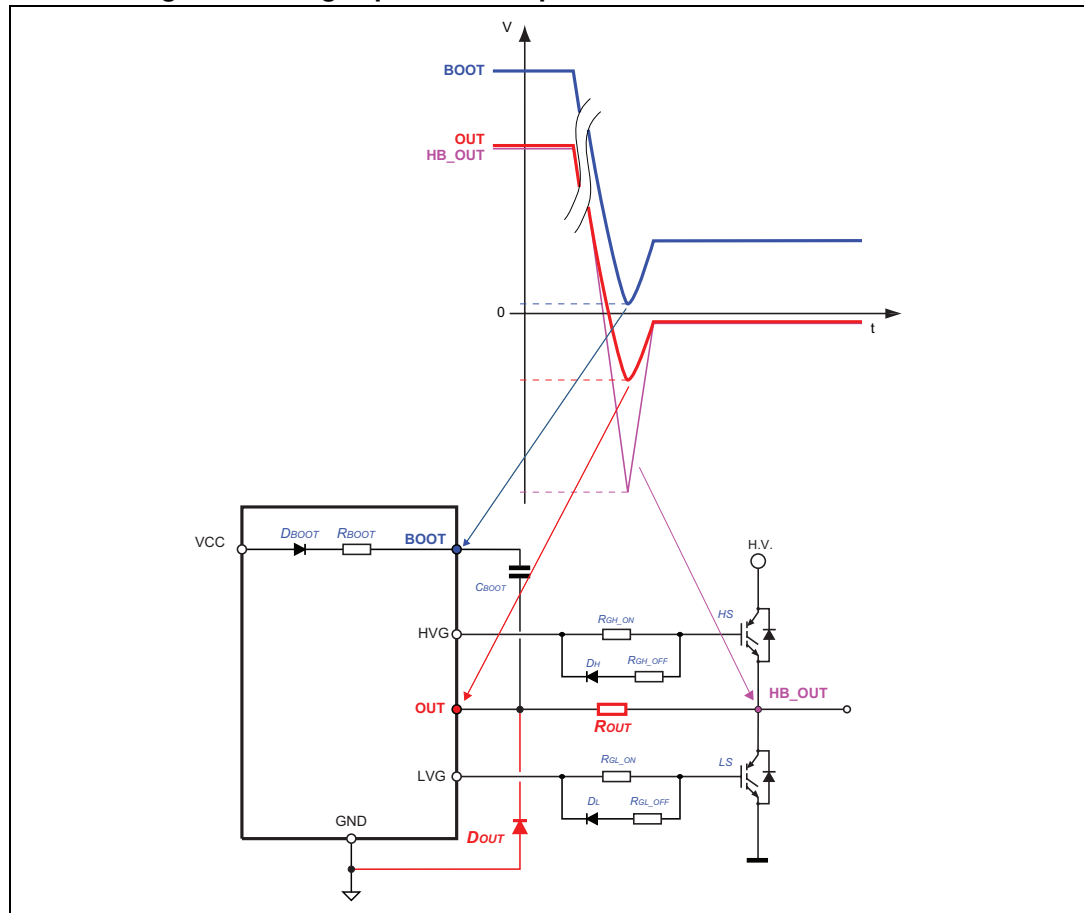
Note that R_{OUT} resistor is also in series with the charging path of the bootstrap capacitor. Its effects may be more evident during the first charge of the bootstrap capacitor, when it is completely discharged and a significant charging current may flow into the R_{OUT} resistor, producing an additional voltage drop between ground and OUT pin. Because during the bootstrap charging the HVG pin is set to low level, the OUT pin and the HVG pin are shorted together and have the same voltage, so the voltage drop due to ROUT results directly transferred to the V_{GE} (or V_{GS}) of the high side IGBT (or MOSFET). Then the risk is that a weak turn ON of the high side power switch, when the low side power switch is already ON, could cause a cross-conduction in the power half bridge. Actually in most of cases this doesn't represent an issue for the proper working of the application, because the typical intrinsic resistance R_{BOOT} (~120 Ω) in series to the internal bootstrap diode is much higher than the R_{OUT} commonly used and the voltage drop on R_{OUT} is negligible.

9.3 Issues related to the below-ground voltage phenomenon

The issues resulting from significant below-ground voltages on the OUT pin are not related to the maximum absolute voltage values that the OUT pin is able to withstand, but related mainly to the voltage value of the BOOT pin, which is indirectly bound with the OUT pin voltage. There are two main issues to be carefully taken in consideration, both related to the absolute maximum ratings of the IC.

- VBOOT absolute minimum voltage.
- VBOOT-VOUT absolute maximum voltage.

9.3.1 V_{BOOT} voltage safe operating condition

Electrically, the OUT pin could stand safely below ground of many volts without problems, but the BOOT pin cannot. The absolute value of the VBOOT voltage must not go steadily below -0.3 V in order to avoid the turn-on of the built-in junction between the BOOT pin and the IC gate driver substrate (connected to GND), normally in reverse condition. The turn-on of this junction could in fact cause a very high current that could in turn cause damage to the device.

9.3.2 Bootstrap capacitor overcharging

Another important point to consider is the overcharging of the bootstrap capacitor. Even before the OUT pin approaches the zero voltage value, the bootstrap diode (internal or external) tends to tie V_{BOOT} close to the VCC supply voltage; since the OUT pin is below ground, the bootstrap capacitor is overcharged through the current coming from the bootstrap diode and then the V_{BOOT} - V_{OUT} voltage increases. It is very important that the bootstrap overcharging does not overcome the recommended maximum value for the V_{BOOT} - V_{OUT} voltage (see the relevant datasheet), because the high-side floating section of the gate driver could be damaged.

Note that a significant overcharging of the bootstrap capacitor is really only possible through the static contribution of the below-ground voltage, because the dynamic below-ground voltage is very brief and the overcharging transition is limited by the time constant RC of the bootstrap capacitor and by the overall resistance in series with the bootstrap diode.

Figure 31 shows the overcharging phenomenon in detail.

Figure 31. Bootstrap overcharging due to below-ground voltage on OUT pin
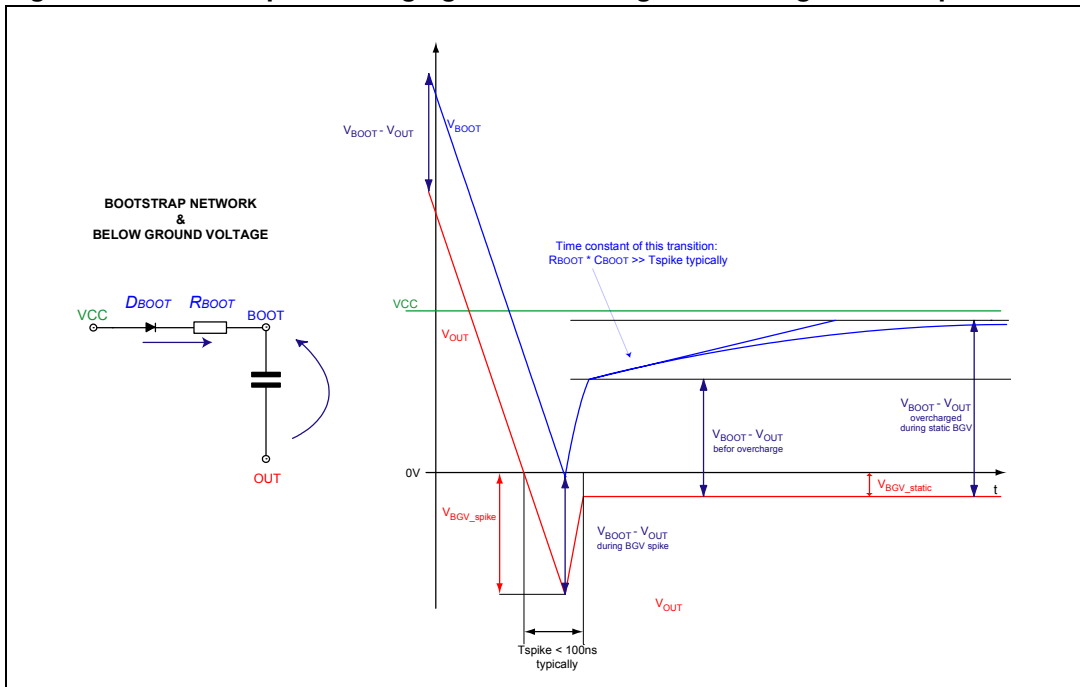
Note that in the L6393 IC gate driver the internal DMOS in series with the integrated bootstrap diode is only fully turned on when the LVG is ON. In fact, when the LVG is OFF, the gate of the bootstrap DMOS is biased at VCC voltage. This means that if the V_{BOOT} is pulled down by the bootstrap capacitor (due to a below-ground voltage on the OUT pin) at about 3 V (typical value) below the VCC voltage, the DMOS turns on again. *Figure 32* shows some different (internal and external) bootstrap network characteristics.

Figure 32. Different bootstrap network characteristics
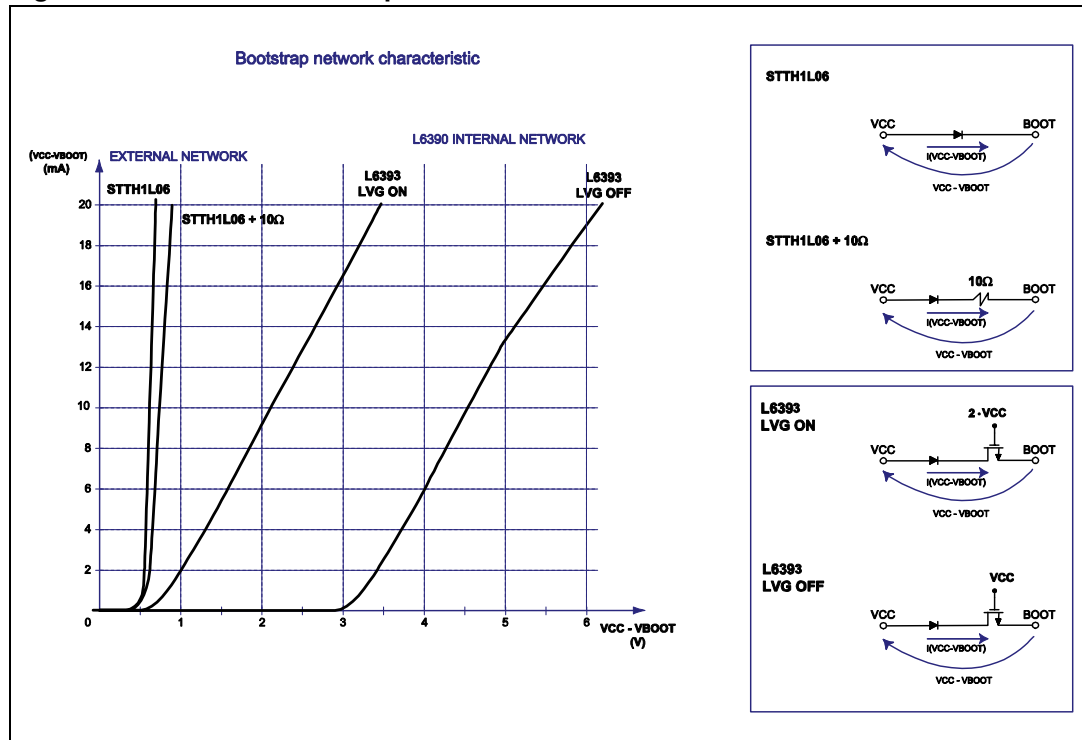
Regarding the below-ground voltage spike, typically this undershoot voltage has a very brief duration (less than 100 ns), therefore it is not enough to further overcharge the bootstrap capacitor since the time constant of the bootstrap charging is equal to the product of the C_{BOOT} and the R_{BOOT} resistance in series with the diode. Moreover, the higher this resistance, the lower the risk of bootstrap overcharging during BVG spikes.

For example, with an R_{BOOT} of 120 Ω and a C_{BOOT} equal to 100 nF, the associated time constant would be about 12 µs, much higher than the typical below-ground voltage spike duration: with the internal bootstrap diode it is very difficult to overcharge the floating section up to dangerous voltages in the very short duration of the undershoot spike. More attention must be paid to the below-ground voltage of the V_{BOOT} during this spike, because, as already explained above, the internal junction V_{BOOT} to substrate could turn on; for very short periods (some tens of nanoseconds) this is typically not a problem.

Figure 33 summarizes the main conditions to avoid any issues related to the below-ground voltage phenomenon in steady-state. As explained in *Section 9.1*, typically the static below-ground voltage is hardly higher than 2 V, so for most applications these constraints are not usually necessary.

Figure 33. L6393 safe operating range when OUT pin is below ground voltage (in steady state)
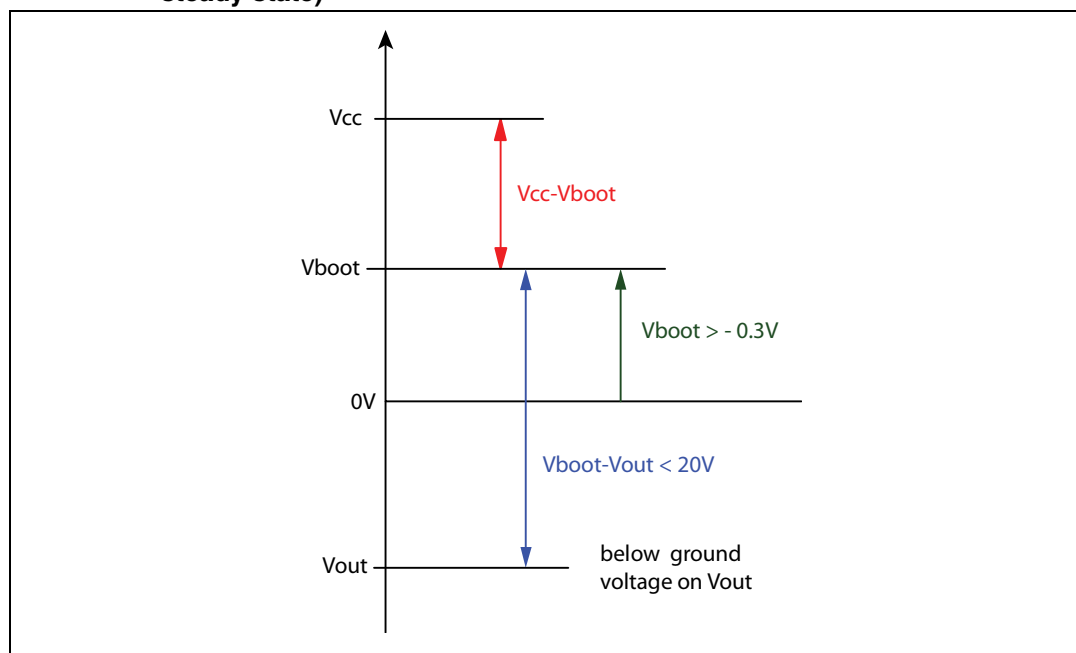
9.4 Functionality of L6393 outputs in below-ground condition

The L6393 IC gate driver makes use of a level shifter in order to send the set-reset information to the high-side floating section. The level shifter, shown in *Figure 34*, is mainly composed of two high-voltage switches, for set/reset signals, driven by the low-voltage section and linked to two pull-up resistors connected to the BOOT pin.

Figure 34. Driver functionality in below-ground voltage condition on OUT pin
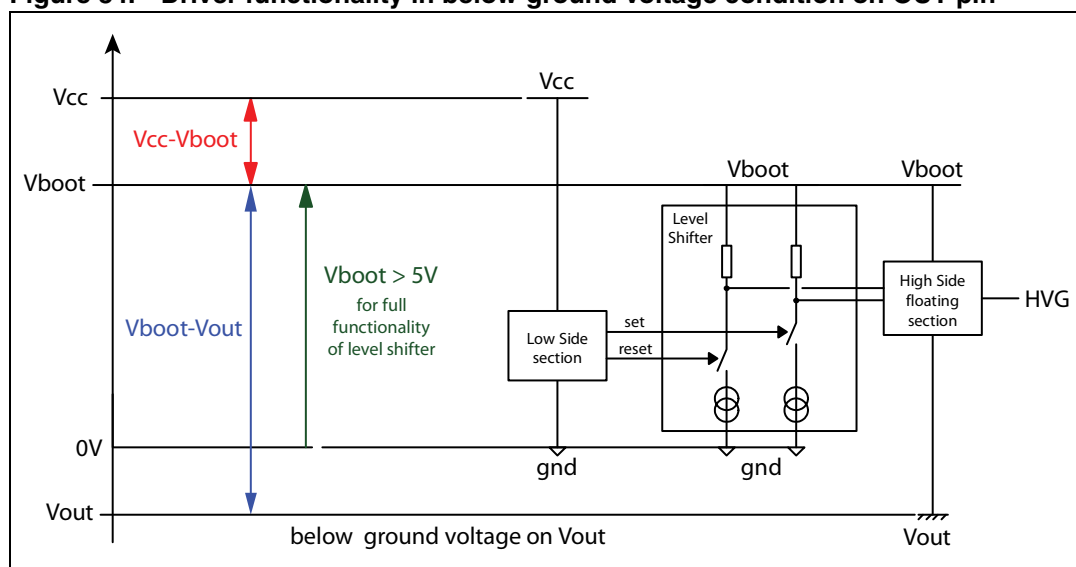
The two level-shifted signals are then fed into a logic latch in the high-side floating section, providing the logic state for the high-side gate driver (HVG output).

The L6393 IC provides the full switching functionality of the high-side section until the level shifter is operating. Because the two pull-up resistors are connected to the floating supply V_{BOOT} of the high-side floating section, the driver still works properly if the OUT voltage begins to go below ground. This means that the operating limit for the level-shifter structure has to be referred to the absolute value of the BOOT voltage with respect to ground. In fact, the BOOT voltage can be considered as the supply of the level-shifter block. The minimum operating value of the level-shifter supply is 5 V, so the V_{BOOT} value must be at least 5 V. The V_{BOOT} - V_{OUT} voltage can have any value in the range of 12.4 V ÷ 20 V. If the BOOT voltage is between 0 and 5 V, the functionality of the level shifter is not certain, but internal structures should not be damaged.

The following section provides some examples.

9.4.1   Steady-state (DC) conditions

When the LVG is OFF, the bootstrap diode only turns on when the BOOT voltage is about 2 V below VCC (worst case: minimum voltage drop value), so it could overcharge the bootstrap capacitor up to a maximum voltage of about VCC - 2 V - V_{OUT}. In order to not overcome the value of 20V on the V_{BOOT} - V_{OUT} voltage, the OUT pin could be forced permanently to the value of VCC - 2 V - 20 V; the L6393 IC would still operate safely, making the HVG output switching as the HIN logic input.

Table 3.   Minimum V_{OUT} in DC condition providing safe and full operation of the high-side section

	Example 1	Example 2	Example 3
VCC	12.5	15	17
V_{BOOT}	10.5	13	15
V_{OUT} (min)	-9.5	-7	-5
V_{BOOT} - V_{OUT} (max)	20	20	20

In any case it must be emphasized, as already explained in the previous paragraph, that in most applications the static below-ground voltage of the OUT pin is very rarely lower than approximately - 2 V.

9.4.2   Transient conditions

If the time during which the OUT pin goes below ground is limited, the bootstrap overcharge will probably not overcome the safe operating range (20 V) of V_{BOOT} - V_{OUT}, even if the V_{OUT} voltage is lower than the limit of VCC - 2 V - 20 V mentioned in the previous paragraph. In such a case, the gate driver and the high-side section are fully operational if the V_{BOOT} voltage remains above 5 V, as explained previously for the proper functioning of the high-side level shifter. In any case, the logic state is maintained as long as the V_{BOOT} remains above ground.

Figure 35.   OUT below-ground voltage in transient conditions: limited boot overcharging
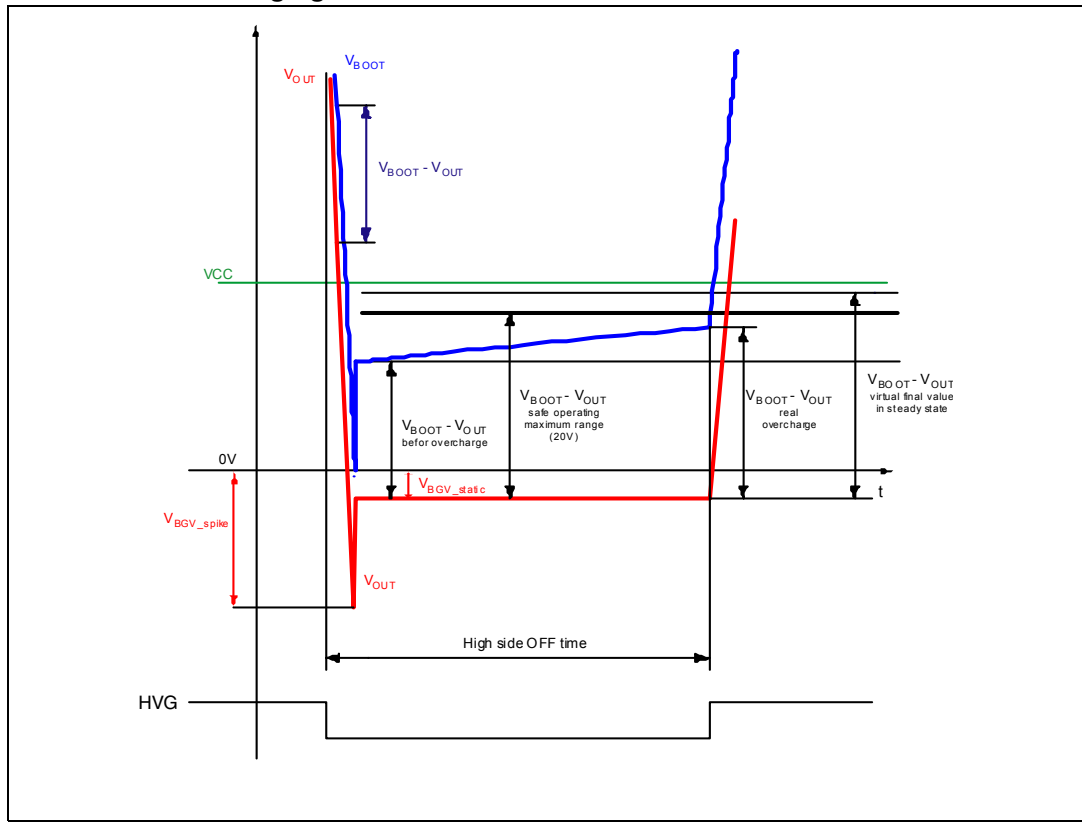
9.4.3   Below-ground voltage spikes

As explained in the previous section, the dynamic contribution of the below-ground voltage on the OUT pin does not have enough time to overcharge the bootstrap capacitor. This fact usually excludes the risk of exceeding the recommended maximum value of 20 V for the V_{BOOT} -V_{OUT} voltage, but on the other hand it increases the danger of pulling the BOOT pin down below ground, then violating its absolute minimum rating. As mentioned above, for safe operation of the IC gate driver, this phenomenon should be avoided. However, note that applicative bench tests have shown that the L6393 also works with below-ground spikes on the OUT pin that well exceed -50 V (see *Figure 36*).

**Figure 36. Example of below-ground voltage spike**
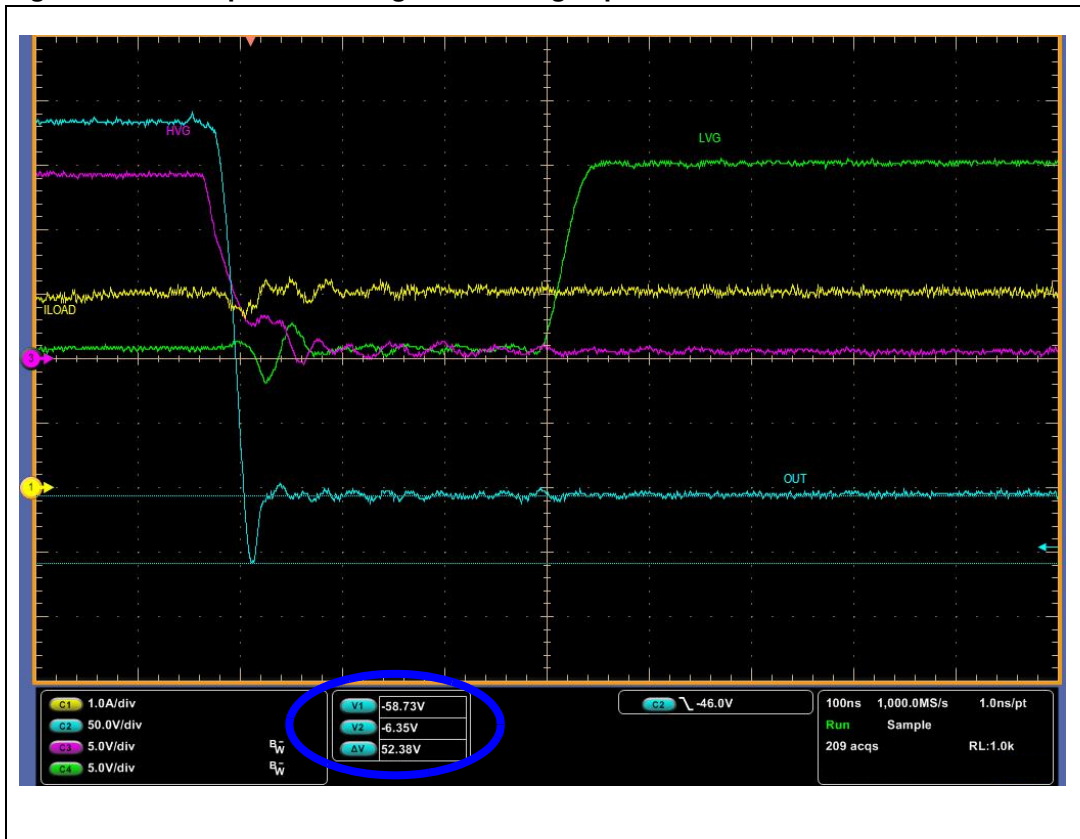
10 Layout suggestions

Typically, for power applications using high voltages and large load currents, the board layout of all circuits related to the power stage is important. Board layout includes different aspects, such as track dimensions (length and width), circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements and power sources in the PCB area.

There are several reasons for paying attention to the layout, which include all the EMI issues, both induced and perceived by the application, over-voltage spikes due to parasitic inductances along the PCB traces, proper connection of the sense blocks and the logic inputs of the L6393 device.

Figure 37 provides some layout guidelines and suggestions for a full-bridge application.

Figure 37.   Layout suggestion for a H-bridge power system
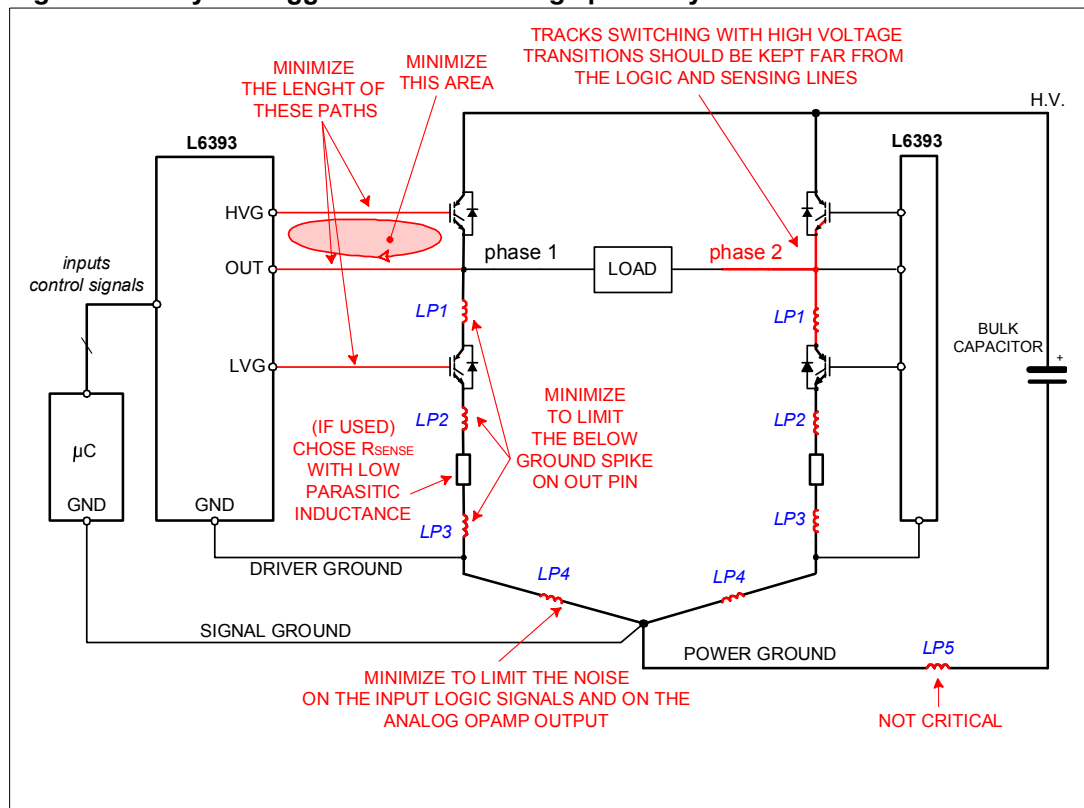
As explained in *Section 6.1.6*, the gate driving PCB traces should be designed as short as possible and the circuit area should be minimized to avoid sensitivity of such structures to surrounding noise. Typically, a good power system layout keeps the power IGBTs (or MOSFETs) of each half-bridge as close as possible to the related gate driver.

Figure 37 shows a set of parasitic inductances related to the different circuit tracks. The various inductance groups may have undesired effects which should be limited as much as possible. Moreover, note that *Figure 37* emphasizes parasitic inductances located on the lines usually managing high voltages and fast current transitions, which are very noisy.

The group of LP1, LP2 and LP3 parasitic inductances is located along the low-side path of each half-bridge, between the OUT pin and the GND of the related driver, and provides an undesired contribution to the issue of below-ground voltage spikes on each OUT pin of the L6393 (described in *Section 9.1*). In fact, at the beginning of the current recirculation on the low-side switches, the current may experience a high dI/dt which is able to produce, on those parasitic inductances, significant voltage spikes. Those spikes add up with the voltage drop of the low-side diode and of the R_{SENSE} (when present) and have a negative sign, so the overall voltage drop between OUT and GND may be significant. The suggestion is to limit as much as possible each contribution to this phenomenon by limiting the length of tracks LP1, LP2 and LP3 and by using an R_{SENSE} resistor with low intrinsic inductance. LP1 may be reduced by connecting the OUT line directly to the collector (or drain) of the low-side IGBT (or MOSFET), LP2 may be reduced by placing the R_{SENSE} resistor as close as possible to the emitter (or source) of the low-side IGBT (or MOSFET). The LP3 may be minimized by connecting the GND line (also called driver ground) of the related gate driver directly to the R_{SENSE} resistor.

LP4 represents the parasitic inductance located between the ground connections of each gate driver (driver ground) and the ground connection of the application controller (also called signal ground). Due to its location, this parasitic inductance introduces noise which is experienced by the input logic signals and by the L6393 comparator output signal. In fact, each phase of the bridge causes high currents (with high dI/dt) to flow on these paths, causing voltage noise which drops between the gate driver ground and the controller ground. This noise between the two grounds is directly added to all logic and analog voltage signals between the gate driver and the micro-controller, including the input logic signals and the analog output of the related comparator. It is recommended to minimize this noise by reducing as much as possible the distance between the signal ground and the driver ground (for each gate driver in the system). In general, it is recommended to connect the signal ground to the various driver grounds through a star connection, in order to improve the balancing and symmetry for any kind of driving topology.

Note: *Ground loops must be avoided; only a single path must connect two different ground nodes.*

The LP5 parasitic inductance is not usually critical because it stands between the minus terminal of the bulk capacitor and the signal/power ground: the spikes on this parasitic element have little influence on other system nodes.

Another useful suggestion is to respect some distance between the lines that switch with high-voltage transitions and the signal lines sensitive to electrical noise. The tracks of each OUT phase bringing significant currents and high voltages should be separated from the logic lines and analog sensing circuits of the comparators.

11 Revision history

Table 4. Document revision history

Date	Revision	Changes
01-Dec-2009	1	Initial release.

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