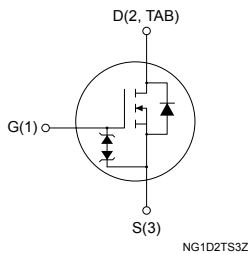
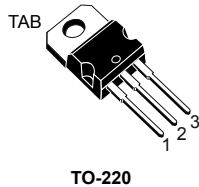


## N-channel 300 V, 360 mΩ typ., 9 A SuperMESH Power MOSFET in a TO-220 package



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$
STP12NK30Z	300 V	400 mΩ	9 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Zener-protected

### Applications

- Switching applications

### Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

#### Product status link

[STP12NK30Z](#)

#### Product summary

Order code	STP12NK30Z
Marking	P12NK30Z
Package	TO-220
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	300	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	9	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	36	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	90	W
ESD	Gate-source human body model ( $R = 1.5\text{ k}\Omega$ , $C = 100\text{ pF}$ )	3	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 9\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance, junction-to-case	1.38	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance, junction-to-ambient	62.5	$^\circ\text{C}/\text{W}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max.)	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	155	mJ

## 2 Electrical characteristics

$T_C = 25\text{ °C}$  unless otherwise specified.

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	300	-	-	V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 300\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 300\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$	-	-	50	
$I_{GSS}$	Gate-body leakage current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$	-	-	$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4.5\text{ A}$	-	360	400	m $\Omega$

1. Specified by design, not tested in production.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	670	-	pF
$C_{oss}$	Output capacitance		-	125	-	pF
$C_{rss}$	Reverse transfer capacitance		-	28	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }240\text{ V}$	-	70	-	pF
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	3.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 240\text{ V}$ , $I_D = 9\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 13. Test circuit for gate charge behavior)	-	25	35 <sup>(2)</sup>	nC
$Q_{gs}$	Gate-source charge		-	5.5	-	nC
$Q_{gd}$	Gate-drain charge		-	13.4	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

2. Specified by design, not tested in production.

**Table 6. Switching times**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 150\text{ V}$ , $I_D = 4.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$	-	16	-	ns
$t_r$	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	36	-	ns
$t_f$	Fall time		-	10	-	ns

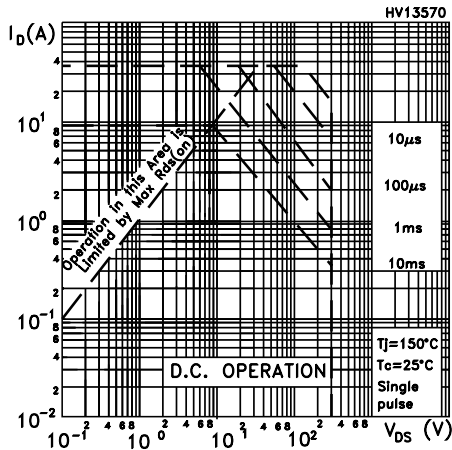
**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-	9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-	36	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 9\text{ A}$ , $V_{GS} = 0\text{ V}$	-	-	1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,	-	165	-	ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 40\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	0.9	-	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see the Figure 14. Test circuit for inductive load switching and diode recovery times)	-	11.2	-	A

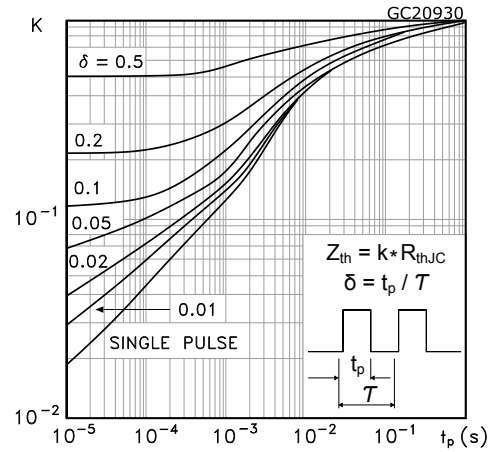
1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

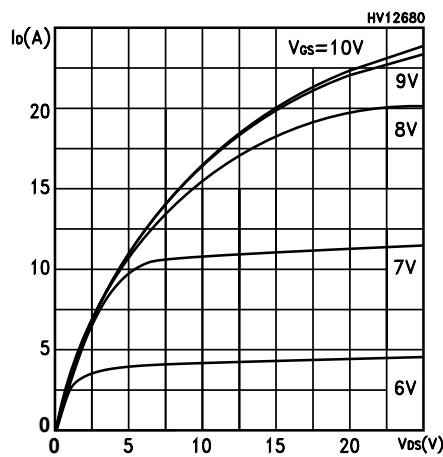
**Figure 1. Safe operating area**



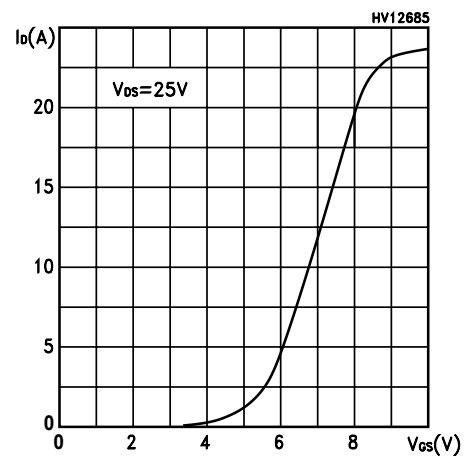
**Figure 2. Normalized transient thermal impedance**



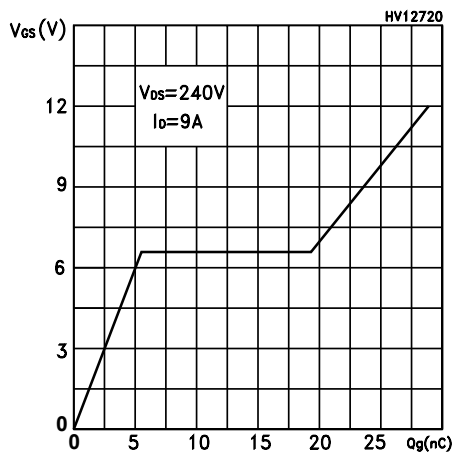
**Figure 3. Typical output characteristics**



**Figure 4. Typical transfer characteristics**



**Figure 5. Typical gate charge characteristics**



**Figure 6. Typical drain-source on-resistance**

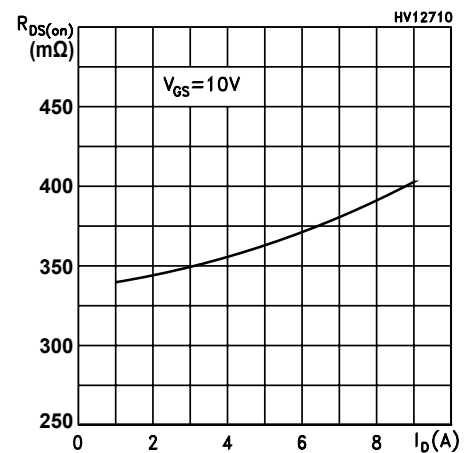


Figure 7. Typical capacitance characteristics

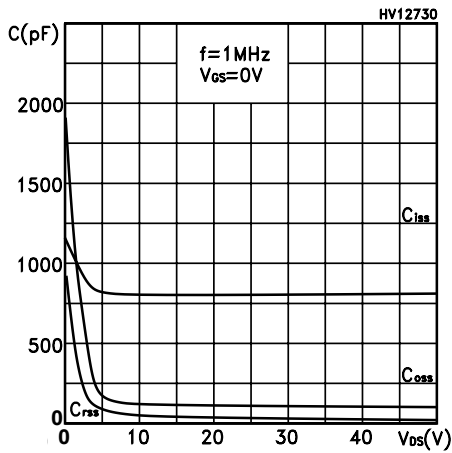


Figure 8. Normalized gate threshold vs temperature

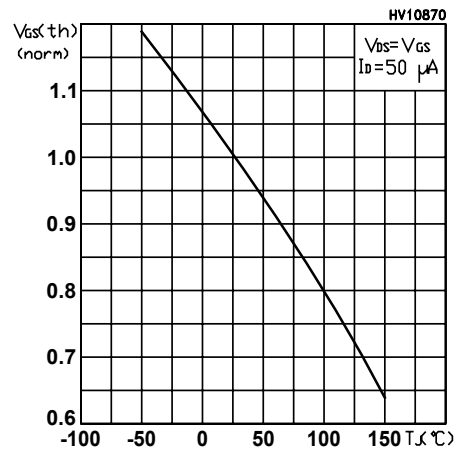


Figure 9. Normalized on-resistance vs temperature

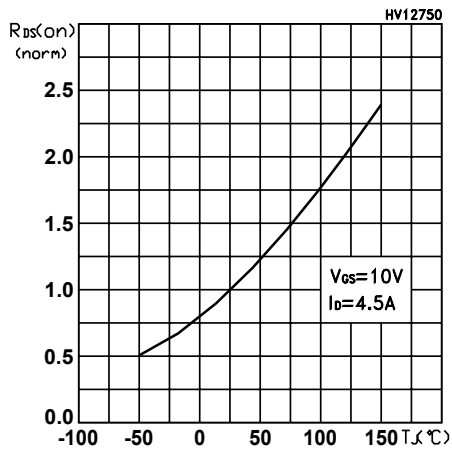


Figure 10. Normalized breakdown voltage vs temperature

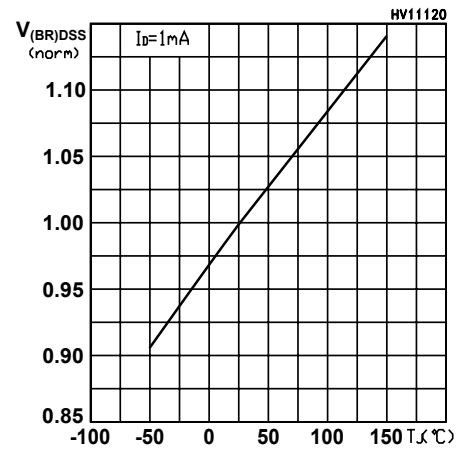
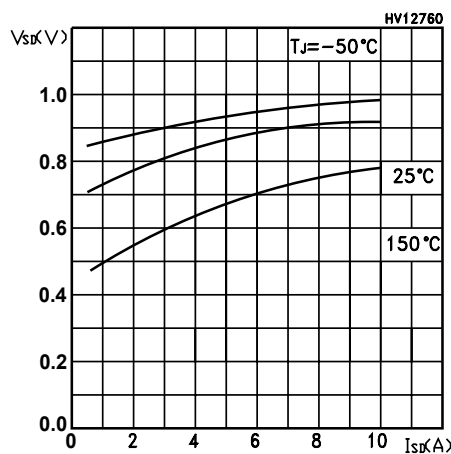


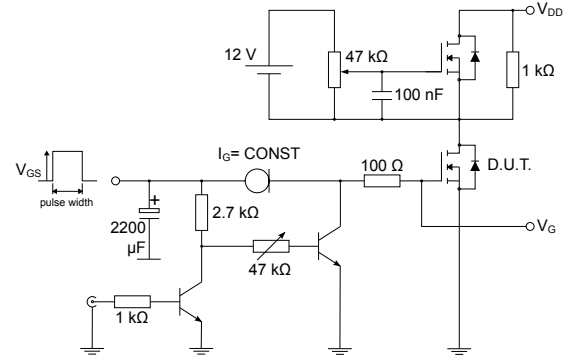
Figure 11. Typical reverse diode forward characteristics



### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**

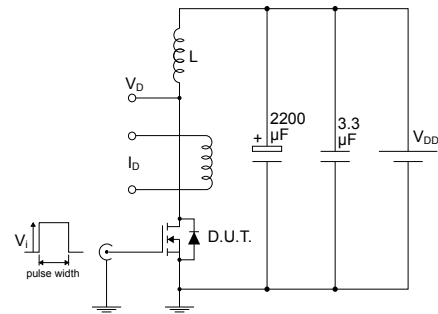

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**Figure 13. Test circuit for gate charge behavior**


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**Figure 14. Test circuit for inductive load switching and diode recovery times**


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**Figure 15. Unclamped inductive load test circuit**


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**Figure 16. Unclamped inductive waveform**


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**Figure 17. Switching time waveform**

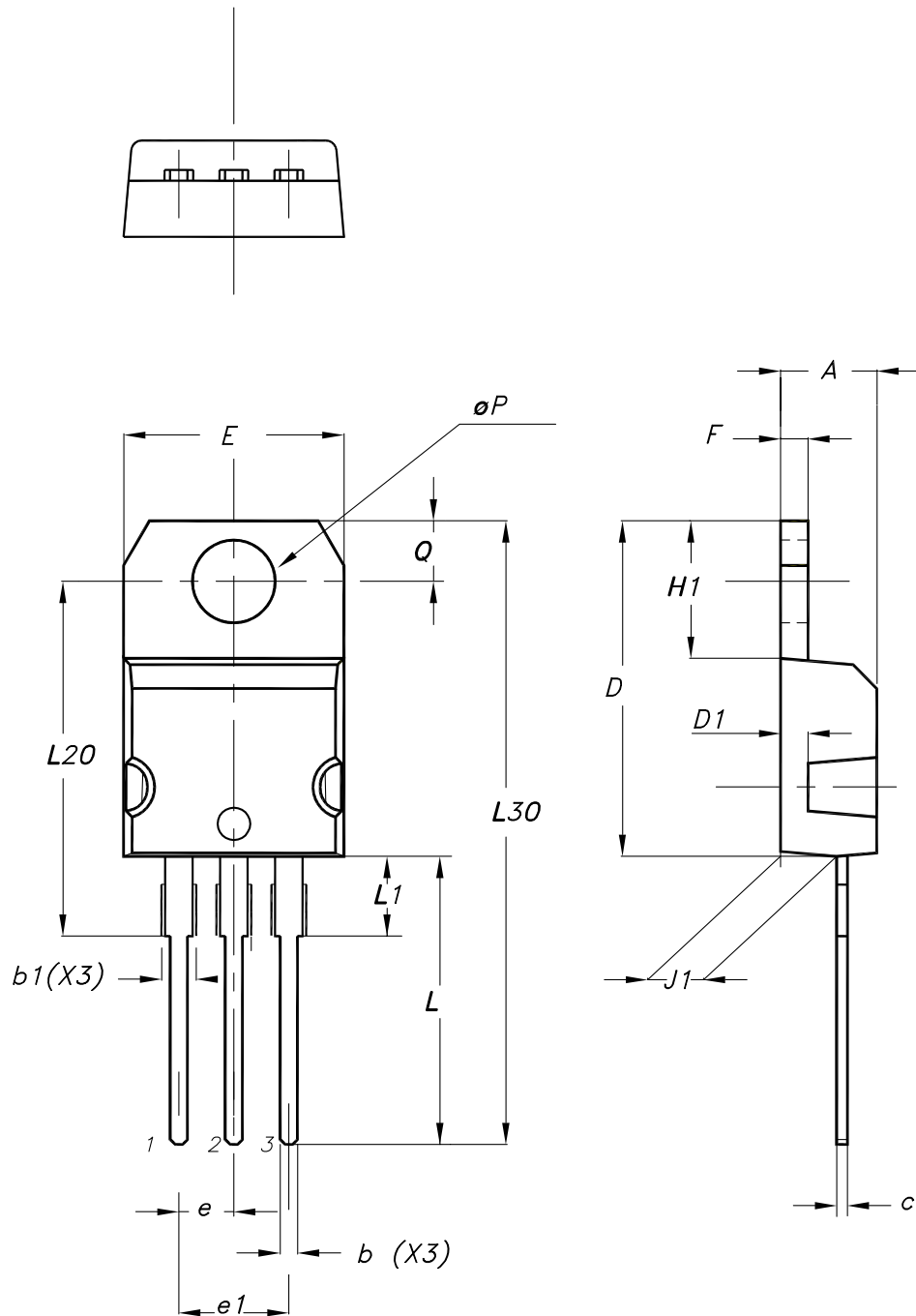

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## 4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 TO-220 type A package information

Figure 18. TO-220 type A package outline



0015988\_typeA\_Rev\_24

**Table 8. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

## Revision history

**Table 9. Document revision history**

Date	Revision	Changes
11-Dec-2002	1	First release.
23-Mar-2026	2	Updated Section 4: Package information. Minor text changes.

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