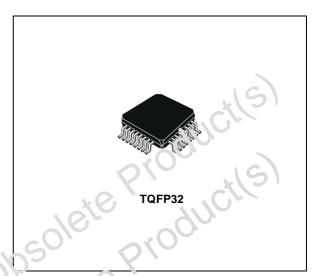




DIFFERENTIAL LVDS CLOCK DRIVER

- 100ps PART-TO-PART SKEW
- 50ps BANK SKEW
- DIFFERENTIAL DESIGN
- MEETS LVDS SPEC. FOR DRIVER OUTPUTS AND RECEIVER INPUTS
- REFERENCE VOLTAGE AVAILABLE OUTPUT V_{BB}
- LOW VOLTAGE V_{CC} RANGE OF 2.375V TO 2.625V
- HIGH SIGNALLING RATE CAPABILITY (EXCEEDS 700MHz)
- SUPPORT OPEN, SHORT, AND TERMINATED INPUT FAIL-SAFE (LOW OUTPUT STATE)
- PROGRAMMABLE DRIVERS POWER OFF CONTROL



DESCRIPTION

The STLVD210 is a low skew programmable 1-to-5 dual differential LVDS driver, designed with clock distribution in mind. The LVDS input signals can be either differential or single-ended if the VBB output is used.

The STLVD210 is provided with a 11 bit shift register with a serial in and a Control Register. The purpose is to enable or power of each output clock channel and to select the clock input. The

STLVD210 is specifically designed, modelled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within a device. The net result is a dependable guaranteed low skew device.

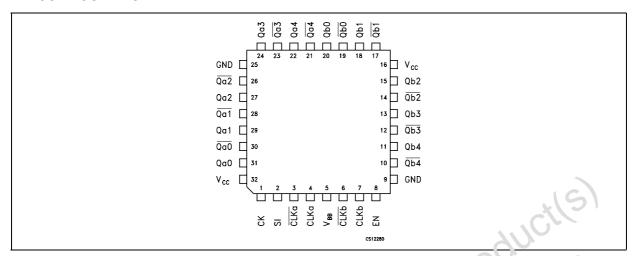
The STLVD210 can be used for high performance clock distribution in 2.5V systems with LVDS levels. Designers can be take advantage of the device's performance to distribute low skew clocks across the backplane or the board.

ORDEPING CODES

Туре	Range	Package	Comments
STLVD210Bt	-40 to 85 °C	TQFP32 (Tray)	250 parts per Tray
STLVD2.62! R	-40 to 85 °C	TQFP32 (Tape & Reel)	2400 parts per reel

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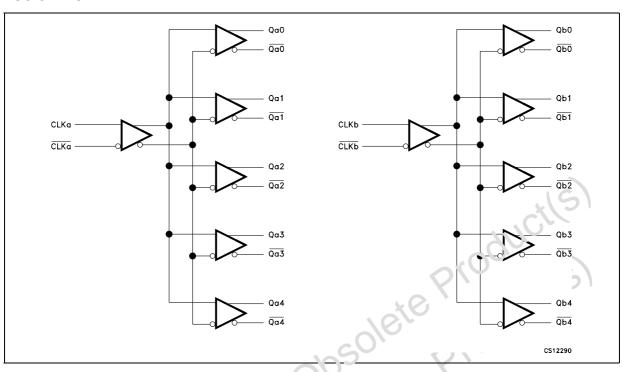
PIN CONFIGURATION



PIN DESCRIPTION

	SYMBOL	NAME AND FUNCTION
1	CK	Control Register Cluck
2	SI	Control Registe Serial IN/CLK_SEL
3, 4, 6, 7	CLKn/CLKn	LVDC CL K Inputs
5	V _{BB}	Reference Voltage Output
8	EN	Device Enable/Program
9, 25	GND	GROUND
0, 11, 12, 13, 14, 15, 17, 8, 19, 20, 21, 22, 23, 24, 26, 27, 28, 29, 30, 31		LVDS
16, 32	V _{CC}	Supply Voltage
solete P	Rodinio	

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Para:neter	Value	Unit
V _{CC}	Supply Voltage	-0.3 to 2.8	V
V _I	Input Voltage	-0.2 to (V _{CC} +0.2)	V
Vo	Output Voltage	-0.2 to (V _{CC} +0.2)	V
I _{OSD}	Driver Short Chront Current	Continuous	
ESD	Electros atic Discharge (HBM 1.5KΩ, 100pF)	>2	KV

Absolute Maxim 'n Ca ings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

THERMAL DATA

Symbol	Parameter	Value	Unit
R _{Tj-c}	Thermal Resistance Junction-Case	13	°C/W

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		TYP	Max	Unit
V _{CC}	Supply Voltage	2.375		2.625	V
V _{IC}	Receiver Common Mode Input Voltage	0.5(V _{ID})		2-0.5(V _{ID})	V
T _{OPR}	Operating Free-Air Temperature Range	-40		85	°C
T _J	Operating Junction Temperature	-40		105	°C

DRIVER ELECTRICAL CHARACTERISTICS ($T_A = -40$ to 85 °C, $V_{CC} = 2.5V \pm 5\%$, unless otherwise noted. Typical values are at $T_A = 25$ °C) (Note 1)

Symbol	Doromotor	Test Conditions		Unit		
Symbol	Parameter	rest Conditions	Min.	Тур.	Max.	Onit
V _{OD}	Output Differential Voltage	$R_L = 100 \Omega$	400	500	600	mV
ΔV_{OD}	V _{OD} Magnitude Change				30	mV
Vos	Offset Voltage		1.05	1.15	1.25	V
ΔV_{OS}	V _{OS} Magnitude Change				30	mV
Ios	Output Short Circuit Current	$V_O = 0V$		15	30	mA
		$V_{OD} = 0V$		7	15	

NOTE 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device pround unless otherwise specified.

RECEIVER ELECTRICAL CHARACTERISTICS ($T_A = -40$ to 85 °C, $V_{CC} = 2.5V \pm 5\%$, Tabless otherwise noted. Typical values are at $T_A = 25$ °C) (Note 1)

Symbol	Parameter	Test Conditions	270	√alue	10	Unit
Symbol	Falametei	lest Collultions	Min.	Тур.	Max.	Unit
V _{IDH}	Input Threshold High	1810		41)	100	mV
V _{IDL}	Input Threshold Low		-100	70,0		mV
I _{IN}	Input Current	V _I = 0V	0/1	42	100	μΑ
		V _I = V _C C		2	10	

NOTE 1: All currents into device pins are positive; all currents out c. device pins are negative. All voltages are referenced to device ground unless otherwise specified.

DRIVER ELECTRICAL CHARACTERISTICS ($T_A = -40$ to 85 °C, $V_{CC} = 2.5V \pm 5\%$, unless otherwise noted. Typical values are at $T_A = 25$ °C) (Note 1)

Sumbal	Params'er	Test Conditions		Value		l lmi4
Symbol	Params ev	rest Conditions	Min.	Тур.	Max.	Unit
V _{BB}	Output Returence Voltage	$V_{CC} = 2.5 \text{ V}$ $I_{BB} = 0.5 \text{ mA}$	1.15	1.25	1.35	V
I _{CCD}	Power Supply Current	All driver enabled and loaded		125	180	mA
	Sr. 40	All driver disabled		18	25	
C _{II}	Input Capacitance	$V_I = 0V$ to V_{CC}		5		pF
UOUT	Output Capacitance			5		pF
V _{IH}	Logic Input High Threshold	V _{CC} = 2.5 V	2			V
V _{IL}	Logic Input Low Threshold	V _{CC} = 2.5 V			0.8	V
l _l	Logic Input Current	$V_{CC} = 2.5 \text{ V}, V_{IN} = V_{CC} \text{ or GND}$			±10	μΑ

NOTE 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

LVDS TIMING CHARACTERISTICS ($T_A = -40$ to 85 °C, $V_{CC} = 2.5V \pm 5\%$, unless otherwise noted. Typical values are at $T_A = 25$ °C) (Note 1)

Cumbal	Dovemeter	Took Conditions		Unit			
Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Uill	
t _{TLH}	Transition Time Low to High	$R_L = 100 \ \Omega, C_L = 5 \ pF$		220	300	ps	
t _{THL}	Transition Time High to Low			220	300	ps	
t _{PHL} , t _{PLH}	Propagation Delay to Output			2	2.5	ns	
f _{MAX}	Maximum Input Frequency		700	900		MHz	
t _{SKEW}	Bank Skew			50		ps	
	Part-to-Part Skew			100			
	Pulse Skew			60			

NOTE 1: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

SPECIFICATION OF CONTROL REGISTER

The STLVD210 is provided with a 11 bit shift register with a Serial In and a Control Register. The purpose is to enable or power of each output clock channel. The STLVD210 provides two working modality: PROGRAMMED MODE (EN=1)

The shift register have a serial input to load the working configuration. Once the configuration is loaded with 11-clock pulse, another clock pulse loads the configuration into the control register. The first bit on the serial input line enables the outputs Qb4 and Qb4, the second bit enables the outputs Qb3 and Qb3 and so on. The last bit is the fewer significations. To restart the configuration of the shift register a reset of the state machine must be done with a clock pulse on CK and the EN set to Low. The control register can be configured on time after each reset.

STANDARD MODE (EN=0)

In Standard Mode the STLVD210 isn't programmable, all the clock outputs are enabled.

TRUTH TABLE OF STATE N'AC LINE INPUTS

EN	S!	СК	ОИТРИТ
L	X	X	All Outputs Enable
Н	S L	Ţ	First stage stores "L", other stages store the data of previous stage
H	Н),,\[\]	First stage stores "H", other stages store the data of previous stage
5	X	7	Reset of the state machine, Shift register and Control Register

SERIAL INPUT SEQUENCE

	BIT#10	BIT#9	BIT#8	BIT#7	BIT#6	BIT#5	BIT#4	BIT#3	BIT#2	BIT#1	BIT#0
V	N.A.	Qa0	Qa1	Qa2	Qa3	Qa4	Qb0	Qb1	Qb2	Qb3	Qb4

A7/

TRUTH TABLE OF SEQUENCE

BIT#10	BIT#(0-4)	Qb(0-4)
X	L	OFF
X	Н	ON
PIT#10	PIT#/5 0\	02(0.4)

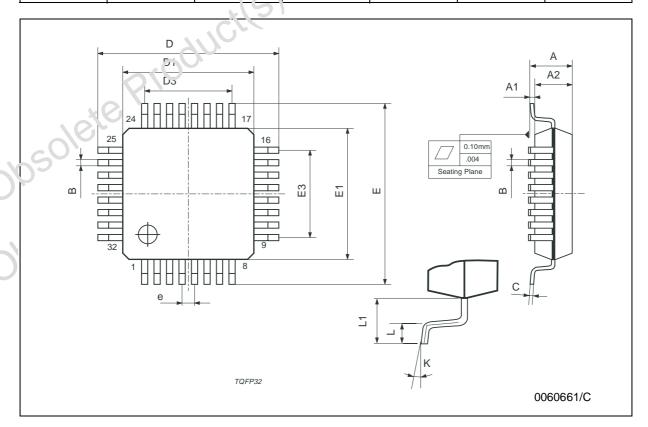
BIT#10	BIT#(5-9)	Qa(0-4)
X	L	OFF
X	Н	ON

TRUTH TABLE

Н	CLKa	Qa (0-4)	Qa (0-4)
	L	Н	
L	Н	L	N.
CLKb	CLKb	Qb (0-4)	Qb (0-4)
Н	L	Н	1/2/
L	Н	L	Ĥ
Obsolete Pro	.15)	Obsolete P	

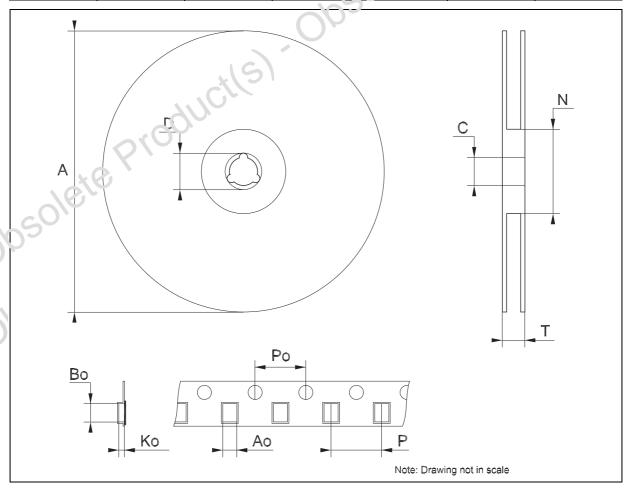
TQFP32 MECHANICAL DATA

DIM.	mm.		inch			
DINI.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
В	0.30	0.37	0.45	0.012	0.015	0.018
С	0.09		0.20	0.0035		0.0079
D		9.00			0.354	1/2
D1		7.00			0.276	5
D3		5.60			0.2.20	
Е		0.80			0.031	
Е		9.00		40.	0.354	
E1		7.00		10/2	0.276	
E3		5.60	C	0/2	0.220	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00	0		0.039	
K	0°	3.5°	7°	0°	3.5°	7°



Tape & Reel TQFP32 MECHANICAL DATA

DIM.	mm.		inch			
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
А			330			12.992
С	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		16)
Т			22.4			0.682
Ao	9.5		9.7	0.374	AU!	0.382
Во	9.5		9.7	0.374	1100	0.382
Ko	2.1		2.3	0.083		0.091
Po	3.9		4.1	0 173		0.161
Р	11.9		12.1	0.468		0.476



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