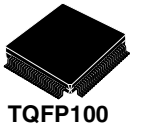
ST20184

ADSL2+ ANALOG FRONT END FOR CPE APPLICATIONS

1 Overview

The ST20184 is an ADSL2+ analog front end chip designed for CPE applications. It is first released as part of the ST-20190 Utopia chipset. The chipset allows equipment manufacturers to develop flexible platforms showing high performance, fully leveraging the ADSL2+ 24 Mbps wireline speed. These platforms can quickly adapt to the rapidly changing requirements of the emerging ADSL2+ Triple-play market covering data, voice and video applications.

Figure 1. Package



TQFP100

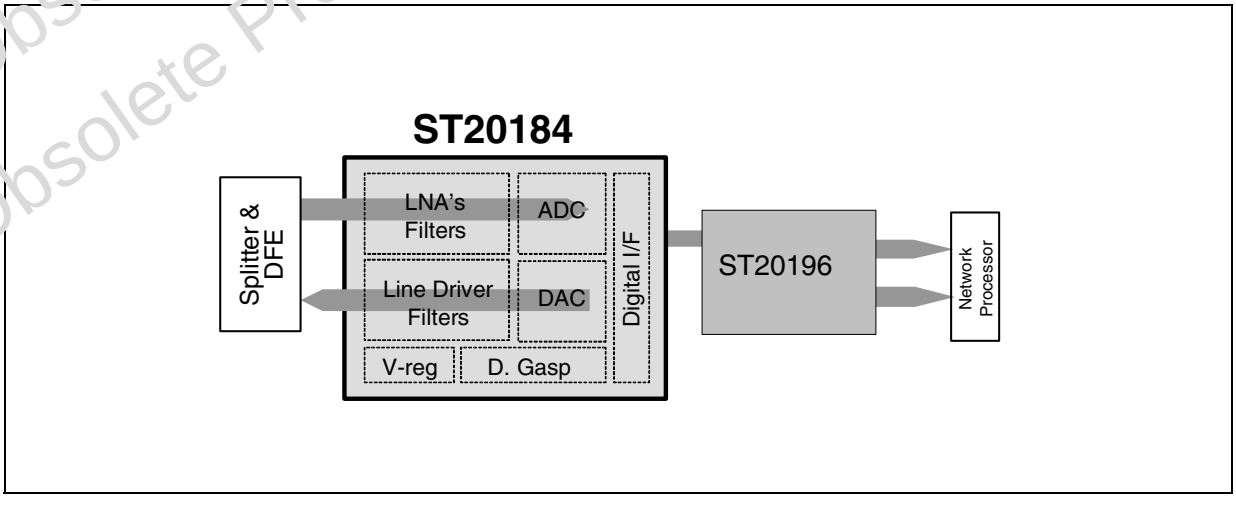
Table 1. Order Codes

Part Number	Package
ST20184	TQFP100

2 Features

- Multi-standard support
  - G.992.1 annexA,B,C (SBM/DBM) & I
  - G.992.2 - g.Lite
  - G.992.3 annexA,B,I,J,L (extended reach),M (double upstream)
  - G.992.4 - g.Lite.bis
  - G.992.5 annexA,B,C,I,J,M
  - ANSI T1.413 Issue2
  - ETSI TS 101 388 ADSL-over-ISDN
- Reduced Bill of Materials due to integration of :
  - Line driver
  - Tunable Rx and Tx-fitlers
  - Voltage regulator for 2.5V
  - Dying gasp comparator
- 13dBm online capable
- More than 14bit resolution DAC/ADC
- 70MS/s ADC interface and 8.8MS/s AC
- 4th order tunable continuous-time receive and transmit filters
- Low noise PGA's and 8dB Tx gain tuning
- Triple Rx input channel configuration
- Supply Voltage : 5V and 3.3V
- Typical power consumption : 750 mW
- Temperature range : I-range (-40°C to 85°C)
- Package : TQFP100

Figure 2. ST20184 Block Diagram



3 General Description

The new ADSL2+ standards will accelerate Broadband applications way beyond always-on data streaming, mainly used for web-browsing and e-mailing. Internet Service Providers are exploring several ways to increase their revenues by offering new services and applications and enlarging their customer base. This can be realized using the large number of new features and different annexes of ADSL2+.

Compared to its widely deployed predecessors, MTC20154 and MTC20174, the ST20184 has been designed in a shorter gate-length, state-of-the-art analogue CMOS technology. Due to the transition in semiconductor technology and the introduction of advanced design techniques, CAD tools and simulation software, the performances have been optimized to define the next generation requirements.

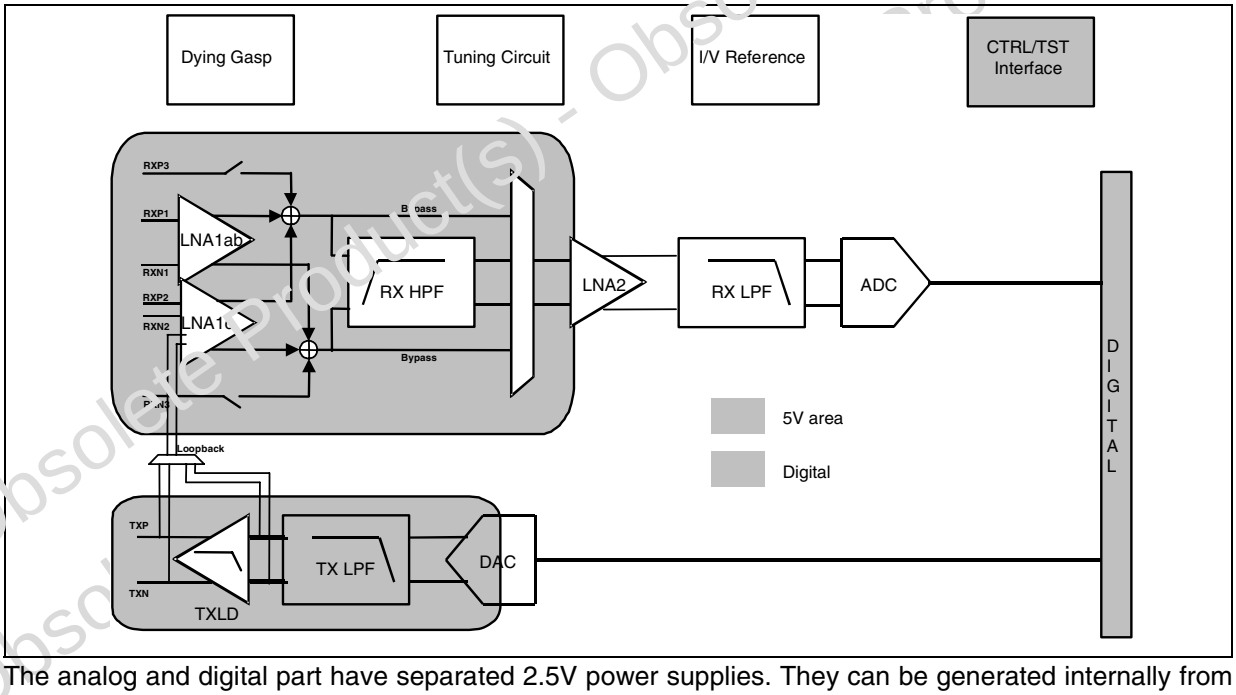
The ST20184 contains a integrated Line Driver supplied at 5V. In the receiving path great care has been taken to lower the noise floor, increase the dynamic range and linearity of the programmable gain amplifiers (LNA's). In both Rx and Tx path tunable, active filters have been integrated to deal with the different frequency allocations for upstream an downstream bands. The analogue/digital conversions are done by a more than 14bit resolution ADC and DAC.

For external BOM cost reduction a 2.5V Voltage regulator and dying gasp comparator is integrated and Digital clock recovery or Time domain interpolation has been implemented only requiring a X-tal to be hooked-up to the chip.

4 Functional Description

The ST20184 consists of the following functional blocks (see figure 3).

Figure 3. Functional block diagram of ST20184



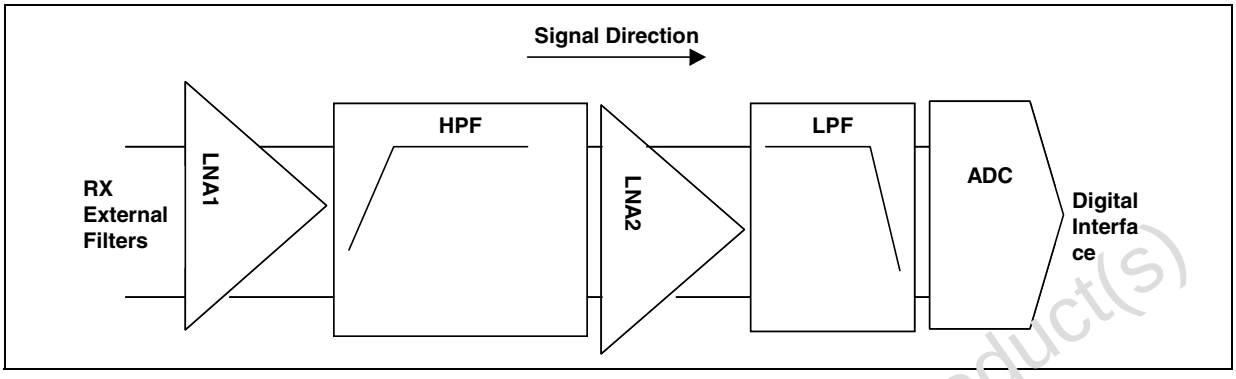
The analog and digital part have separated 2.5V power supplies. They can be generated internally from the 3.3V supply. In addition some part of the analog section of the ST20184 has a power supply of 5V. The digital I/Os work on an additional 3.3V supply.

4.1 THE RECEIVER (RX)

In the RX direction, a LNA (Low Noise Amplifier) provides a first amplification/attenuation stage. Its role is to make the signal fit in the RX input dynamic range while using the maximum amplification for noise reduction. The RX HPF is a 3rd order high pass filter with a switchable cut-off frequency of 140 kHz (Annex A,C,I,L) or 280 kHz (Annex B,J,M). It removes a part of the echo signal allowing the use of a low order, external, high pass filter. The second LNA provides a second amplification made possible by the prior fil-

ter. A low pass 2nd order filter is added before the ADC for anti-aliasing purposes. Analog-to-digital conversion at 70 MS/s and multiplexing to the 35 MHz RX bus take place before the signal is sent to the digital interface.

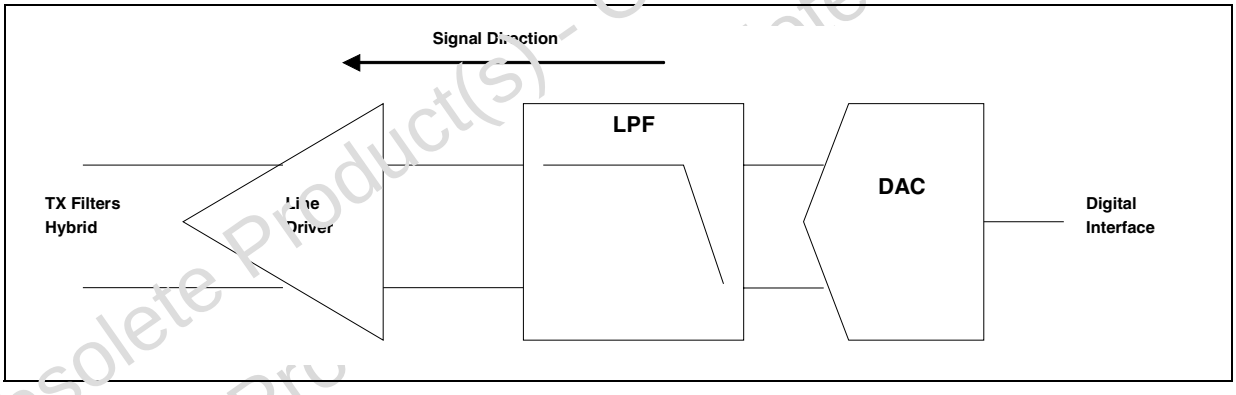
Figure 4. Receiver Block diagram



4.2 THE TRANSMITTER (TX)

In the TX direction, the data coming from the digital interface is de-multiplexed and converted to an analog signal. Next is a 2nd order low-pass filter with a switchable cut-off frequency of 160 kHz (Annex A,C,I,L) or 320 kHz (Annex B,J,M). Its output is amplified by the TX line driver that also provides a 2nd order Butterworth lowpass filtering.

Figure 5. Transmitter Block diagram



4.3 FILTER TUNING AND DYING GASP

A filter-tuning module is implemented in order to fine-tune each filter's cut-off frequency (fc) to compensate process variation.

A dying gasp controller is provided on the chip. It consists of a comparator that compares an external voltage coming from a power supply with an internal reference voltage.

4.4 THE DIGITAL INTERFACE

The digital interface block implements all the logic required to provide access in read and write mode to all the configuration and status registers. It can be divided into two parts:

– The data interface that converts the multiplexed data from/to the DMT signal processor into valid representation for the TX DAC and RX ADC.
– The control interface that allows the board processor to configure the ST20184 settings (RX/TX gains, filter band, etc.).

4.5 ATU-R BLOCK DIAGRAM

An ATU-R block diagram of the analog front end is presented in the following figure. In addition to the ST20184, the following blocks are a possible implementation to complete the line interface.

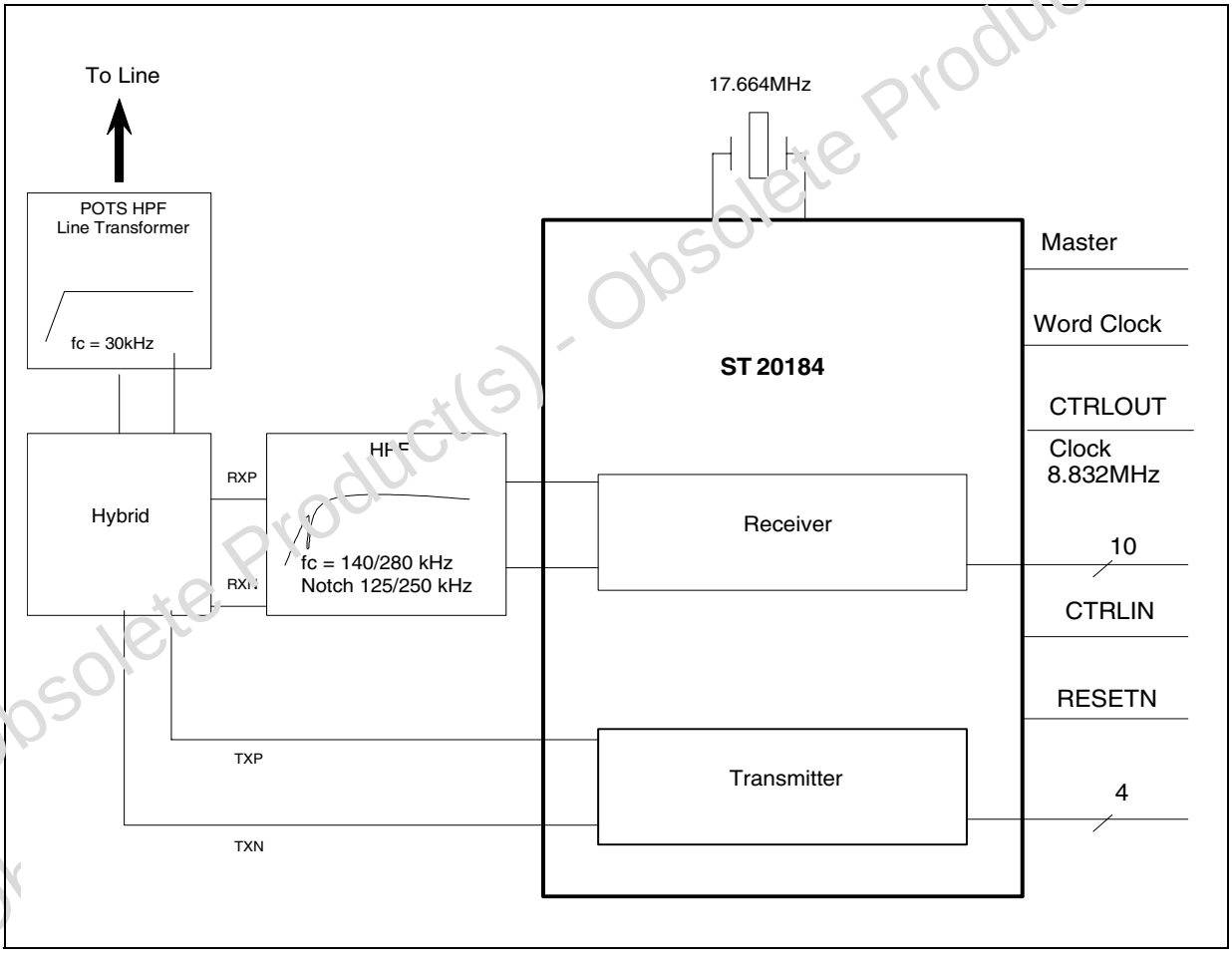
An external RX high pass filter is a third order filter that filters out the echo from the TX path. The ST-20184's internal high pass filter completes the echo cancelling in the RX path.

The hybrid is using a structure which is cost and space effective and it is characterized by minimum losses. The hybrid circuit provides also the necessary line impedance matching.

High pass filters at the end of the line interface filter out the POTS or ISDN band signals. DC blocking is an additional function of these filters.

The ADSL analog front end integrated circuit does not contain any circuitry for the POTS or ISDN service but guarantees that the POTS or ISDN bandwidth will not be disturbed by spurious signals from the ADSL spectrum.

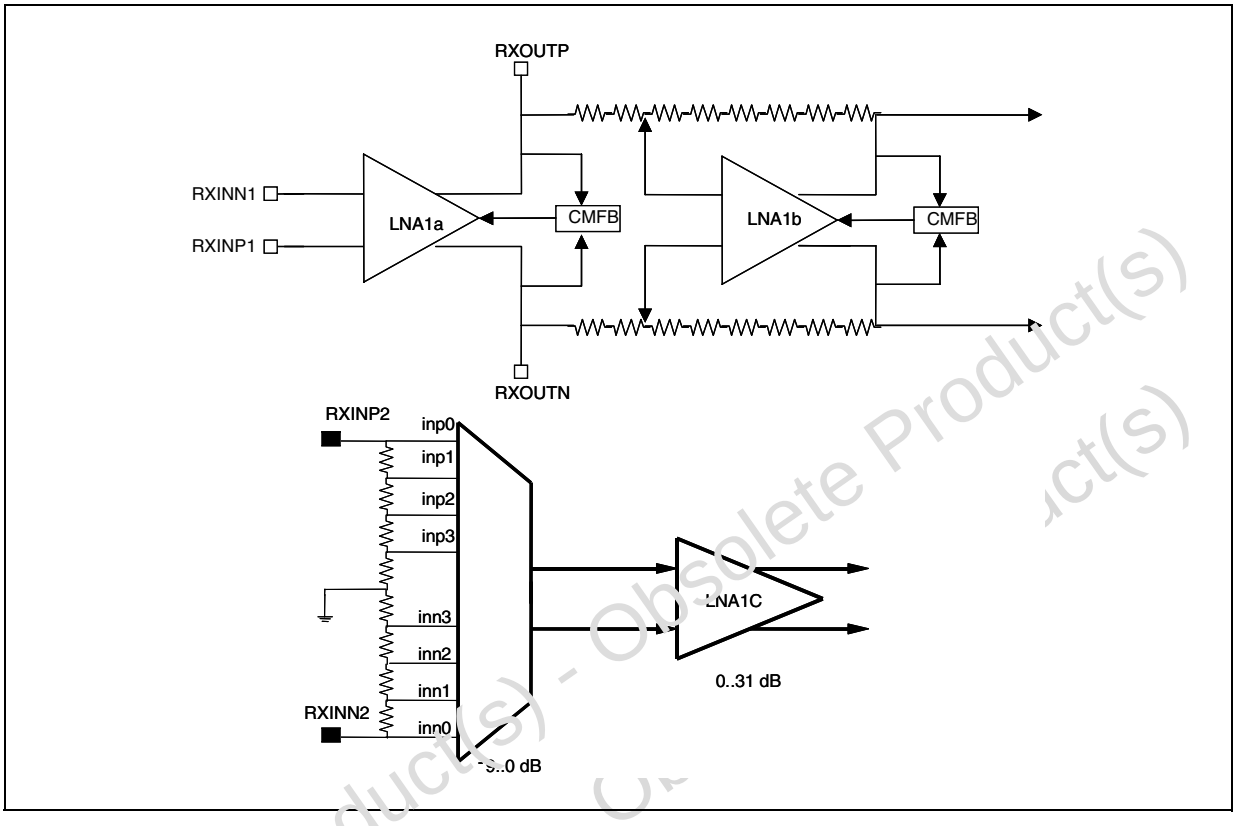
Figure 6. ATU-R AFE Block Diagram



4.6 ST20184 RX PATH

4.6.1 Low Noise Amplifier (LNA1)

Figure 7. Low Noise Amplifier 1 a/b or c



The Low Noise Amplifier (LNA1 a/b or c) is used in combination with the attenuator block to fit the input signal in the 3 volt peak differential output dynamic range.

The gain settings may vary from -9 to 30dB

Table 2. LNA1a/b Characteristics

Data	Min	Typ	Max	Unit
Input type		AC only, DC decoupled		-
Common mode input voltage (virtual ground)	-	AVDD5/2	-	V
Input impedance LNA1b – gain max	-	2*200	-	Ω
Input impedance LNA1b –gain min	-	2*4.2	-	kΩ
Common mode output voltage	-	AVDD5/2	-	V
Max peak output differential voltage (LNA1a&b)	-	3	-	Vpdiff
Amplification range	-10	-	32	dB
Maximum gain error at 1MHz	-0.5	-	0.5	dB
Digital interface	-	5	-	Bits

Table 2. LNA1a/b Characteristics (continued)

Data	Min	Typ	Max	Unit
Average noise for gain 32dB (over a 134kHz to 1.1Mhz band)		6.5	8	nV/√Hz
Gain settings for 1.69kOhm & 523Ohm external resistor Code 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	Low gain LNA1A:PD -9.3 -7.3 -6.3 -4.6 -2.9 -1.2 0.4 2.0 2.8 3.7 4.5 5.4 6.3 7.2 8.2 9.2		High gain LNA1A PU don't use don't use don't use 10.2 12.4 14.6 17.0 19.7 21.2 22.9 24.8 27.1 29.3 33.7 don't use don't use	
Power supply	4.75	5	5.25	V

Table 3. LNA1c Characteristics

Data	Min	Typ	Max	Unit
Input type		AC only, DC decoupled		-
Common mode input voltage	-	AVDD25LNA2	-	V
Max input differential voltage		AVDD5	AVDD5 + 1 Vd	Vpdiff
Differential Input impedance	20	-	38	kΩ
Common mode output voltage	-	AVDD25LNA2	-	V
Max peak output differential voltage	-	3	-	Vpdiff
Attenuation range	0	-	-9	dB
Attenuator step	-	3	-	dB
Amplification range	0	-	28	dB
Amplification step	-	3	-	dB
Maximum gain error in the 20kHz-200kHz band	-0.5		0.5	dB
Amplification code (Attenuation code is at 3) 0 1 2 3 4 5 6 7 8 9 10 11		0.0 2.8 5.7 7.5 9.3 12.4 14.9 17 19.9 21.9 24.4 27.9		dB
Equivalent integrated input noise at gain +20dB, min attenuation over a 20kHz–200kHz band.		12	13	nV/√Hz

Table 3. LNA1c Characteristics (continued)

Data	Min	Typ	Max	Unit
Attenuation digital interface	-	2	-	Bits
Attenuation digital code	'11' → 0 dB attenuation '00' → -9 dB attenuation			
Amplification digital interface	-	4	-	Bits
Amplification digital code	'0000' → 0 dB gain '1011' → 28 dB gain			
Power supply	4.75	5	5.25	V

4.6.2 RX Integrated High Pass Filter

The RX high pass filter attenuates the echo signal at low frequencies to allow a further amplification of the receive signal resulting in a better RX sensitivity.

The RX High Pass Filter has a switchable notch frequency at tone 14 for Annex A,C,I,L, or tone 27 for Annex B,J,M. In addition, it can be bypassed during handshake in Annex C.

The integrated high pass filter has characteristics shown in table 3.

Table 4. RX Band Pass Filter Characteristics

Data	Min	Typ	Max	Unit
Filter type	HP: 1st order Butterworth and 2nd order Chebychev			-
Annex A: Chebychev2 notch frequency Butterworth cut-off frequency		 14 134		 Tone kHz
Annex B: Chebychev2 notch frequency Butterworth cut-off frequency		 27 268		 Tone kHz

4.6.3 Low Noise Amplifier (LNA2)

This block optimizes the signal amplitude for best use of the ADC input dynamic range. It converts the 3 volts peak differential input dynamic into 1 volt peak differential output dynamic range.

Table 5. LNA2 Specification

Data	Min	Typ	Max	Unit
Input differential voltage	-	3	-	Vpdiff
Output voltage	-	1	-	Vpdiff
Amplification range	-11	-	20	dB
Amplification step	0.5	1	1.5	dB
Digital Interface	-	5	-	Bits
Digital code (x)	'00000' → -11 dB attenuation '11111' → 20 dB gain Gain formula: Av = 20*log10[(10+x)/(35-x)]			

4.6.4 RX Low Pass Filter

This block implements the RX anti-aliasing filtering, attenuates the DMT sidelobe and out of band signals. It also shifts the common mode voltage of the 5V powered LNA2 to the correct level for the 2.5V powered ADC. It is designed according to the following characteristics.

Table 6. RX Low Pass Filter Characteristics

Data	Min	Typ	Max	Unit
Filter type		2^{nd} order RC		-
Cut-off frequency (-3dB)	-	2.5	-	MHz

4.6.5 A/D Converter

A Sigma-Delta architecture is used for the A/D converter.

Table 7. A/D Converter Specifications

Data	Min	Typ	Max	Unit
Resolution		14		bits
Linearity		12.5		bits
Full scale input range	-	1.0	-	Vpdiff
Sampling rate	-	70.656	-	MHz

4.7 ST20184 TX PATH

4.7.1 TX Driver

The differential line driver buffers and amplifies the output of the TX filter in the TX signal path and reduces the out of band noise by means of a second order RC LPF. It is a class AB line driver with fixed gain settings (3 dB). Additionally, The line driver incorporates a digitally controlled bias setting. The distortion of the line driver is better than -65dB over the ADSL upstream band with a a differential load of 12.5Ω. The peak differential output swing is 4V.

The line driver characteristics are listed in the following table 8.

To ensure the stability of the line driver, the impedance it sees must be low enough up to high frequencies (100MHz). As in the application an external LC filter, the leakage inductance of the transformer or even the PCB tracks are an inductive load with increased impedance at high frequency, a stabilizer is added close to the TXP/TXN pins. It consists of an RC network as in following figure. At low frequencies (within US range) the capacitor must be sufficiently small to avoid loading the driver. At high frequencies the impedance of the capacitor becomes negligible so that the Line Driver sees the 6 ohm resistor (12 Ohm differential).

Figure 8. TX Driver stabilizer network

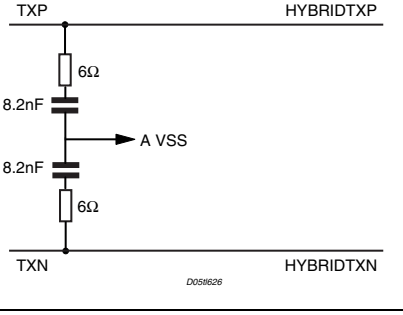


Table 8. TX Driver Characteristics

Data	Min	Typ	Max	Unit
Gain 28kHz	-	3	-	dB
Differential output load	-	12.5	-	Ω
Max. output differential voltage	-	4	-	Vpdiff
Common mode output voltage	-	AVDD5/2	-	V
MTPR	-	-65	-	dB
Power supply	4.75	5	5.25	V
Filter type	LP : 2^{nd} order RC			
Cut off frequency (-3dB) (Annex A/B)	-	148/300	-	kHz

4.7.2 TX Low Pass Filter

This filter performs the TX path out-of-band signal cancellation in order to in order to reduce Downstream signal degradation signal degradation due to NEXT (Near End Crosstalk). The TX low pass filter is also acting as a smoothing filter on the D/A converter output to suppress the image spectrum.

The TX Low Pass Filter has a switchable cut-off frequency of 160 kHz for Annex A,C,I,L, or 320kHz for Annex B,J,M.

It is designed according to the following characteristics.

Table 9. TX Low Pass Filter Specification

Data	Min	Typ	Max	Unit
Filter type	Second Order Butterworth			-
Cut-off frequency (-3dB)	-	160/320	-	kHz
Differential input voltage	-	2.8	-	Vpdiff
In band ripple gain error	-0.5	0	0.5	dB
In band gain	-	0	-	dB
Gain Step	-	0.5	-	dB
Power Supply	4.75	5	5.25	V

4.7.3 Digital To Analog Converter (DAC)

A current steering architecture is used. The characteristics are as following

Table 10. DAC Specifications

Data	Min	Typ	Max	Unit
Resolution		16		bits
Linearity		12		bits
Full scale output range at 0dB gain setting	-	2	-	Vpdiff
Sampling rate Fs	-	8.832	-	MHz
Latency	-	1	-	sampling clock period
DAC Gain settings	-6	-2.5	0	dB
Power Supply	4.75	5	5.25	V

4.7.4 PLL Based Frequency Multiplier

A simple 17.644 MHz crystal frequency can be used with the ST20184 on-board crystal driver.
A frequency multiplier, build up around an integrated Phase Locked Loop (PLL), is used to multiply the frequency to 35.328 Mhz (CLKM) and 70.656Mhz (ADC).

4.7.5 Dying Gasp

The dying gasp circuit monitors an external voltage derived from an external power supply voltage. A comparator compares this voltage with a reference voltage. A possible loss in power is detected and signaled to the digital integrated circuit ST20196 which in turn generates an interrupt. Two external resistors (R1, R2 in the figure below) are used in order to trim the external voltage extracted from the power supply voltage to the desired level. Depending on the supply voltage that is used, the time before the regulated supply drops below the requirements has to be sufficient for the power down to be implemented properly.

Figure 9. The Dying Gasp Circuit

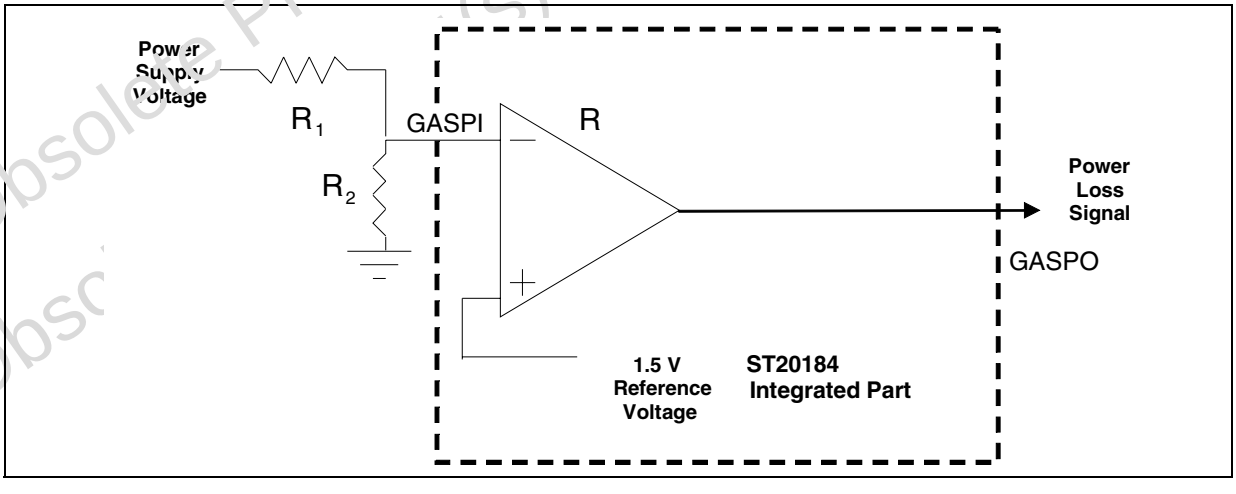


Table 11. Dying Gasp

Data	Min	Typ	Max	Unit
Comparison voltage	-	1.5	-	V
Latency between detection an alarm signal	-	0.5	-	µs

4.7.6 Voltage regulator

The voltage regulator has the function to provide the analog 2.5V power supply for the C184 chip.

The input power supply VRegIn is the 3.3V. Good HF quality and low ESR (lower than 1 ohm at 10kHz) capacitors are required for decoupling.

Two reference voltages are generated internally. The reference voltage coming from an internal resistive divider driven by 5V supply (VRefIn pin 7) is filtered out by an external cap on pin VRefCap (pin 8). The second reference voltage is based on theVRegIn voltage (pin34).

The reference voltage is defined by means of bit 11 in register &X1101.(Bit LDO_USB). When LDO_USB is at zero, which is the default condition, the reference voltage is based on VRefIn pin. When LDO_USB is forced to one, the reference voltage is based on VRegIn pin.

Table 12.

Data	Min	Typ	Max	Unit
Input power supply	3.0	3.3	3.6	V
Regulated output supply (VRegIn=3.3V, VRefIn = 5V)		2.5		V
Decoupling capacitance	10	-	-	µF

4.7.7 Power-On-Reset circuit

A double Power-On-Reset circuit (POR) is used in order to generate an internal reset in case of power supply lower than the PorL threshold and will be released when above PorH threshold. That internal reset signal complementary to the hard reset (applied on reset input pin) guarantees that the C184 chip is working under normal condition and places the driver in a self-protected mode.

A POR circuit is placed on each power supply (AVDD5 and AVSS25) and has the threshold levels depicted in following table. Both POR outputs are monitored separately by the modem chip via the ctrl interface. Their values can be read as POR25 and POR5 in register &X1011. These signals are set when a high level or rising edge is generated by the internal POR5 and POR25 circuit. The value of these bits are reset when they have been read through the control interface.

POR5 monitors the voltage of VREFIN pin (pin 7) and POR25 monitors the voltage of DVDD25PLL (pin82).

Table 13.

Data	Min	Typ	Max	Unit
VporL25	1.25	-	2.1	V
VporH25	1.3	-	2.2	V
Vhyst25	-	100	-	mV
VporL5	2.2	-	4.1	V
VporH5	2.4	-	4.3	V
Vhyst5	-	200	-	mV

4.7.8 HYBRID SWITCHES

C184 has two low impedant switches on board. They are used to stabilize the input impedance of LNA1. The switches can be controlled by means of HYBRID_CTRL<1:0> in register &X1111. The switch between terminal SW1P (pin 37) and SW1N (pin 38) is closed when HYBRID_CTRL<1> is forced to one, and opened when HYBRID_CTRL<1> is forced to zero. The switch between terminal SW2P (pin 39) and SW2N (pin 40) is closed when HYBRID_CTRL<0> is forced to one, and opened when HYBRID_CTRL<0> is forced to zero.

Table 14.

Data	Min	Typ	Max	Unit
Rsw1lo	4	9	18	Ohm
Rsw1hi	3	6	12	Ohm
Rsw2lo	4	9	18	Ohm
Rsw2hi	3	6	12	Ohm

4.8 Digital Interface

4.8.1 Digital Interface Blocks

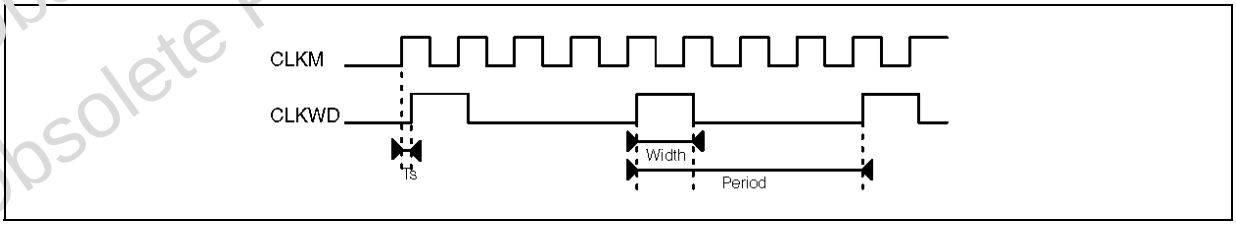
The ST20184's digital interface is composed of a bidirectional serial control interface (CTRLIN-CTRLOUT pins), one transmit data 4-bit wide parallel interface (TXn pins) and one receive data 10-bit wide parallel interface (RXn pins). The interfaces are used as follows:

- The control interface is dedicated to send and read commands towards the ST20184. The interface is synchronized over the word clock (CLKWD pin).
- The TXn interface is used to send digital words (16 bits) over the TX path DAC. The words are multiplexed over the 4 bit wide bus using the word clock as "start word" time reference. The bus is synchronized over the master clock @ 35.328MHz (CLKM pin).
- The RXn interface does not behave like the TX bus. It is dedicated to the PDM stream generated by the ADC. Two samples of each 5 bits will be multiplexed to a 10 bit bus running at 35.328MHz (CLKM).

4.8.2 Master and Word Clock

The system's master clock has a nominal frequency of 35.328 MHz. Based on this clock, a word clock is generated. It is used to synchronise the data multiplexed on the RX and TX buses of the ST20184. The CTRLIN/OUT serial interface will be also totally synchronised on this clock. The word clock is a square pulse having a high level duration (width) equal to one master clock period and a period equal to four master clock periods. The figure here below depicts the signal characteristics.

Figure 10. Word clock generation



4.8.3 Control interface (CTRLIN/OUT pins)

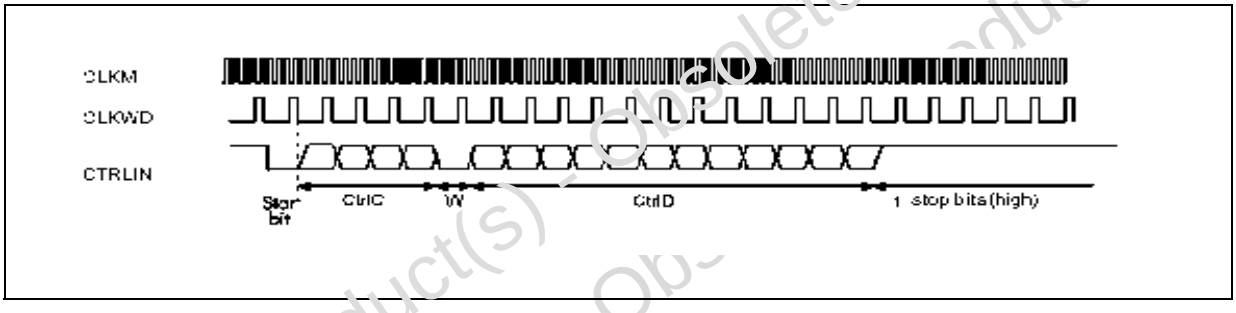
The control interface is bi-directional, allowing the modem chip to send commands towards the analog chip, and also to read the values of its internal registers. A 16-bit control message can be exchanged with the analog ASIC. It is composed of 12 control data bits (CtrlD), and 4 control command bits (CtrlC). The format is detailed in the table below. Note that it differs from the one introduced for the ST20174.

Bit Number	Semantic meaning
15	CtrlC MSB
14 to 13	CtrlC bits 2 to 1
12	CtrlC LSB
11	CtrlD MSB
10 to 1	CtrlD bits 10 to 1
0	CtrlD LSB

4.8.4 Write access to the ST20184

The bit sequence that is transferred is composed of 5 parts: a leading start bit, four bits representing an address (CtrlC), a logic zero to indicate it is a write access, 12 bits of data (CtrlD), and 1 stop bit. This bit sequence is transmitted on the serial interface at a rate defined by CLWD

Figure 11. Serial control interface for write accesses to 20184.

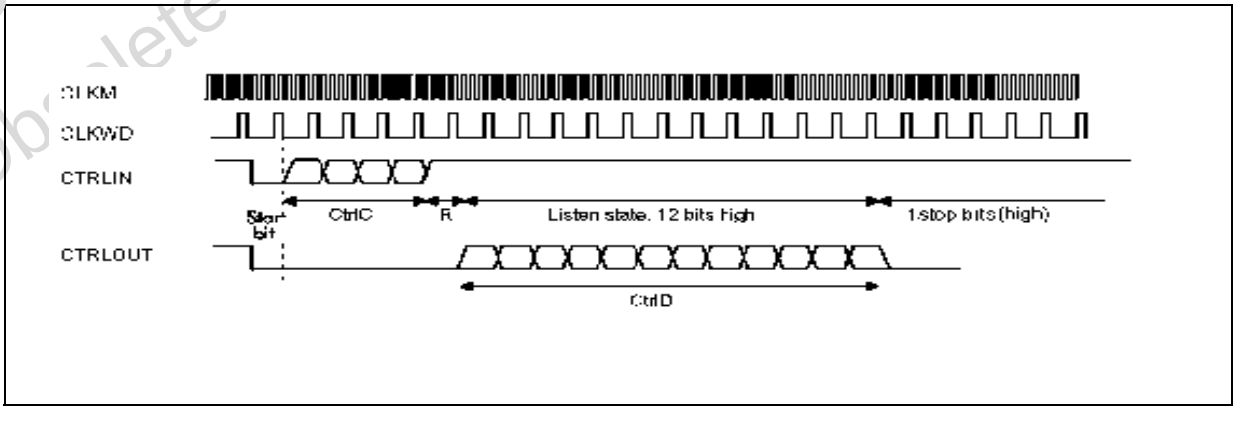


4.8.5 Read access to the ST20184

For this type of accesses, the CTRLIN pin is used, in addition to the already existing CTRLOUT.

The exchange of data takes place in the following order: The Modem chip transmits a leading start bit, four bits representing an address (CtrlC), and a logic one to indicate it is a read access. With the following CLWD pulse, the analog ASIC provides the 12 bits corresponding to the data addressed (CtrlD), and returns to logic zero.

Figure 12. Serial control interface for read accesses to 20184.



4.8.6 Control interface timing

The control interface bits are considered valid on each positive edge of the word clock. They will be sampled at this moment. The stop bit will trigger the internal data validation.

Figure 13. Control interface chronodiagram

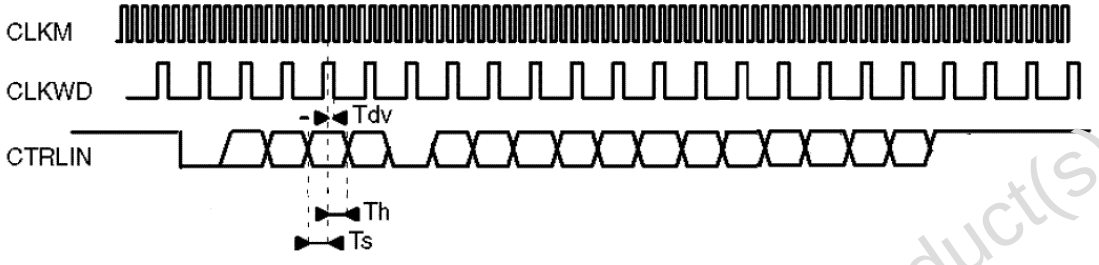


Table 15. Control interface timing requirements

Symbol	Parameter	min	Typ	max
Ts	Setup time	7 ns	-	-
Th	Hold time	0.2 ns	-	-
Tdv	Data valid	0.5 ns	-	3 ns

4.8.7 Control interface bit mapping

The following table depicts all the available control command op-codes and their corresponding data.

Table 16. CTRL interface op-codes and corresponding data

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
0000	**RX PATH CONFIGURATION: LNA1**		
	LNA1B_GAIN3-0 If LNA1A is on: "0000b"=-5.6dB "1100b"=+30dB (larger codes not used) If LNA1A is off: "0000b"=-9.3dB "1111b'=+9.3dB	0000b	CtrlD[3:0]
	LNA1C_ATT1-0 attenuator code for LNA1C	00b	CtrlD[5:4]
	Unused	00b	CtrlD[7:6]
	LNA1C_CM_SWITCH: Closes CM_SWITCH of LNA1C if PD_LNA1B=1 and LNA1C_CM_SWITCH=0. **This register should always be 0.**	0b	CtrlD[8]
	PD_LNA1A "1b"=power down	1b	CtrlD[9]
	PD_LNA1B "1b"=power down	0b	CtrlD[10]
	PD_LNA1C "1b"=power down	1b	CtrlD[11]

Table 16. CTRL interface op-codes and corresponding data (continued)

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
0001	**RX PATH CONFIGURATION: RX FILTER**		
	RX_PROG3_2-0 Analog equalizer settings	001b	CtrlD[2:0]
	RX_PROG2_3-0 Notch frequency	0111b	CtrlD[6:3]
	RX_ANNEXB_B1 select Annex B mode for stage 1 if "1b"	0b	CtrlD[7]
	RX_ANNEXB_2T2 select Annex B mode for stage 2 if "1b"	0b	CtrlD[8]
	RX_PROGF reduced cut-off freq. Of stage 1 if "1b"	0b	CtrlD[9]
	RX_BYPASS_2T2 bypass stage 2 if "1b"	0b	CtrlD[10]
	RX_BYPASS_B1 bypass stage 1 if "1b"	0b	CtrlD[11]
0010	**RX PATH CONFIGURATION: LNA2, ADC, RX_CTUNE**		
	LNA2_GAIN4-0 Gain LNA2 “11111b”=+20.2dB “00000b”=-10.9dB	00000b	CtrlD[4:0]
	LNA2_RXHP_BYPASS “1b”=bypass RX filter “0b”=normal mode	0b	CtrlD[5]
	ADC_2M_RXFILT Selects cut-off freq of Anti-Alias filter for ADSL+ mode “1b”=2.2M “0b”=1.1M	1b	CtrlD[6]
	RX_CTUNE4-0 Ctune code for RX filter	01100b	CtrlD[11:7]
0011	**TX PATH CONFIGURATION: DAC, TXLP, TX_CTUNE**		
	DAC_BIAS1-0 Select bias current of DAC ("11b" is maximum current)	11b	CtrlD[1:0]
	TXLP_ANNEXA select annex A mode if "1b"	1b	CtrlD[2]
	TXLP_ANNEXB select annex A or B mode if "b1" bypass if "0b"	1b	CtrlD[3]
	TXLP_GAINTUNE2-0 TX LPF gain “000b”=0dB” “001b”=1.5dB “010b”=1dB “011b”=0.5dB “100b”=-0.5dB “101b”=-1dB “110b”=-2dB “111b”=-3dB	000b	CtrlD[6:4]
	TX_CTUNE4-0 Ctune code for TX filter	01100b	CtrlD[11:7]

Table 16. CTRL interface op-codes and corresponding data (continued)

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
0100	**TX PATH CONFIGURATION: LD VARIOUS**		
	LD_BIAS3-0 select LD bias current "1111b"=maximum current	0111b	CtrlD[3:0]
	LD_RTUNE4-0 Rtune code for linedriver	01101b	CtrlD[8:4]
	MUTE_LD_AUTO mute-mode control bit for linedriver	0b	CtrlD[9]
	MUTE_LD_FORCE mute-mode control bit for linedriver	0b	CtrlD[10]
	DAC_TRIG_MUTE "1b"=mute mode	0b	CtrlD[11]
0101	**TX PATH CONFIGURATION: LD NMOS1** **Note:CtrlD[0] is not writable.** **Data-command should contain [0 CtrlD[11-1]].**		
	LD_COMP_NMOS1 Input from comparator NMOS1	READ ONLY	/
	LD_DAC_NMOS1_7-0 Absolute value of LD-DAC code for NMOS1	11111111b	CtrlD[8-1]
	LD_DAC_NMOS1_SIGN Sign of LD-DAC code for NMOS1	0b	CtrlD[9]
	LD_CALIB Calibration mode if "1b"	1b	CtrlD[10]
	LD_ANNEXB annex B filter mode if "1b"	0b	CtrlD[11]
0110	**TX PATH CONFIGURATION: LD NMOS2**		
	LD_COMP_NMOS2 input from comparator NMOS2	READ ONLY	/
	LD_DAC_NMOS2_7-0 absolute value of LD-DAC code for NMOS2	11111111b	CtrlD[8-1]
	LD_DAC_NMOS2_SIGN sign of LD-DAC code for NMOS2	0b	CtrlD[9]
	LD_SENSE_NMOS enable NMOS sensing if "1b"	1b	CtrlD[10]
	LD_SENSE_PMOS enable PMOS sensing if "1b"	1b	CtrlD[11]
0111	**TX PATH CONFIGURATION: LD PMOS1**		
	LD_COMP_PMOS1 input from comparator PMOS1	READ ONLY	/
	LD_DAC_PMOS1_7-0 absolute value of LD-DAC code for PMOS1	11111111b	CtrlD[8-1]
	LD_DAC_PMOS1_SIGN sign of LD-DAC code for PMOS1	1b	CtrlD[9]
	LD_NMOS enable NMOS if "1b"	0b	CtrlD[10]
	LD_PMOS enable PMOS if "1b"	0b	CtrlD[11]

Table 16. CTRL interface op-codes and corresponding data (continued)

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
1000	**TX PATH CONFIGURATION: LD PMOS2**		
	LD_COMP_PMOS2 input from comparator PMOS2	READ ONLY	/
	LD_DAC_PMOS2_7-0 absolute value of LD-DAC code for PMOS2	11111111b	CtrlD[8-1]
	LD_DAC_PMOS2_SIGN sign of LD-DAC code for PMOS2	1b	CtrlD[9]
1001	**TEST REGISTER**		
	TEST_XTAL “1b”= test mode for XTAL	0b	CtrlD[0]
	TEST_DRIVER “1b”= test mode for LineDriver	0b	CtrlD[1]
	TEST_ANALOG “1b”= test mode for Analog	0b	CtrlD[2]
	TEST_TST3 "1b"=bypass LNA1B and connected LNA1out to testbus 1	0b	CtrlD[3]
	TEST_NTREE “1b”= test mode for NandTree	0b	CtrlD[4]
	TEST_IIDQ “1b”= test mode for IDDQ digital	0b	CtrlD[5]
	DAC_SINE DAC generates a pre-programmed sine-wave	0b	CtrlD[6]
	LOOP_DAC “1b”=loop-back mode from output TX-LPF to input LNA1C	0b	CtrlD[7]
	TEST_TST1[1-0] TEST_TST1[1]= “1b” loop-back from LineDriverOut to input LNA1C	00b	CtrlD[8-9]
	TEST_TST2[1-0] TEST_TST2[0]= “1b”: DACout to testbus 3 and GP0/1 pins, TEST_TST2[1]= “1b”: Masterbias test	00b	CtrlD[10-11]
1010	**ID bits and Power Down signals: TX RX path**		
	ID2-0: ID bits to identify version of AFE chip	READ ONLY	CtrlD[2-0]
	PD_RXHP_BUTTER “1b”=power down	0b	CtrlD[3]
	PD_RXHP_CHEBY_OP1 “1b”=power down	0b	CtrlD[4]
	PD_RXHP_CHEBY_OP2 “1b”=power down	0b	CtrlD[5]
	PD_RXHP_CHEBY_OP3 “1b”=power down	0b	CtrlD[6]
	PD_LNA2 “1b”=power down	0b	CtrlD[7]
	PD_ADC “1b”=power down	0b	CtrlD[8]
	PD_DAC “1b”=power down	0b	CtrlD[9]
	PD_LD “1b”=power down	0b	CtrlD[10]
	PD_LD_COMP “1b”=power down	0b	CtrlD[11]

Table 16. CTRL interface op-codes and corresponding data (continued)

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
1011	**Various: Power Down signals, DGASP, POR, CTUNE_START**		
	PD_TXLP “1b”=power down	0b	CtrlD[0]
	PD_VCXO “1b”=power down	0b	CtrlD[1]
	unused	0b	CtrlD[2]
	PD_DGASP “1b”=power down	0b	CtrlD[3]
	PD_POR25 “1b”=power down	0b	CtrlD[4]
	PD_POR5 “1b”=power down	0b	CtrlD[5]
	PD_CTUNE “1b”=power down Note: this also resets internal registers of CTUNE block	0b	CtrlD[6]
	CTUNE_START start signal for CTUNE module	0b	CtrlD[7]
	DGASP	SR FlipFlop	CtrlD[8]
	POR25	SR FlipFlop	CtrlD[9]
	POR5	SR FlipFlop	CtrlD[10]
	CTUNE_OVER_UNDER_FLOW 1 if over or under flow to CTUNE circuit occurred	0b	CtrlD[11]
1100	**Clock register: VCXO (DAC), PLL, XTAL**		
	VCXO13-5 control code for VCXO_DAC	100000000b	CtrlD[8-0]
	VCXO_FAST_PLL	0b	CtrlD[9]
	Unused	1b	CtrlD[10]
	PLL_BYPASS bypass PLL if “1b”	0b	CtrlD[11]
1101	**Various: GP and RX Filter test bits**		
	GP3-0	BiDirectional	CtrlD[3:0]
	RX_TEST_ENABLE	0b	CtrlD[4]
	RX_TEST2-0 0=testbus 2 disable 1=LNA2out to testbus 2 2=LNA1Bout to testbus1 3=LNA1Bout to testbus2 4=RXHPF_B1out to testbus 2 5=RXHPF_2T2_OP1out to testbus 2 6=RXHPF_2T2_OP2out to testbus 2 7=RX_HPF_2T2_OP3out to testbus 2	000b	CtrlD[7:5]
	LNA1A_SAL_KEY “0b”=normal current “1b”=larger current in LNA1A	0b	CtrlD[8]
	LDSL “1b”=TX_LPF in LDSL-mode	0b	CtrlD[9]
	LDSL2 “1b”=TX_LPF in LDSL2-mode	0b	CtrlD[10]
	LDO_USB_MODE Selects 3.3V reference ladder for 2.5V LDO-generation. Used in USB-mode.	0b	CtrlD[11]

Table 16. CTRL interface op-codes and corresponding data (continued)

CtrlC[3:0]	Command and related data functional description	Initial Value after RESET(asynchr) POR25 (asynchr) POR5 (synchr)	CtrlD[11:0]
1110	**RX PATH CONFIGURATION: DAC 1**		
	DAC_CODE_ADD11-0	000000000000b	CtrlD[11:0]
1111	**RX PATH CONFIGURATION: DAC 2, HYBRID_CTRL and VCXO (PWM)**		
	DAC_CODE_ADD15-12	0000b	CtrlD[3:0]
	DAC_LIPARI “1b” lipari mode for DAC code	0b	CtrlD[4]
	HYBRID_CTRL1-0	00b	CtrlD[6:5]
	VCXO4-0 keep fixed at “00000b”	00000b	CtrlD[11:7]

N.B. All the unused data bits of a given control op-code are readable/writable.

4.9 RECEIVE/TRANSMIT INTERFACE

4.9.1 Transmit interface data representation

Data are fetched from the ADC using the RX interface, while the DAC receives its data from the TX interface. ADC and DAC converters are working at respectively 70.656 and 8.832MHz sampling frequency. 16 bit wide TX data transmission channel is implemented using two 4 bit wide buses. A multiplexing factor of 4 is used. The bus frequency is thus 35.328 MHz (master clock frequency). The 16 data bits are hereto nibbled into 4 packets of 4 bit wide each. Each of the two data words is multiplexed over the data bus according the little endian order, as depicted in the following table. The packets are numbered according their time occurance order in the multiplex.

Table 17. TX bus multiplexing description

Packet number	Bus line	Word bit
Packet 1	bit 0	bit 0
	bit 1	bit 1
	bit 2	bit 2
	bit 3	bit 3
Packet 2	bit 0	bit 4
	bit 1	bit 5
	bit 2	bit 6
	bit 3	bit 7
Packet number	**Bus line**	**Word bit**
Packet 3	bit 0	bit 8
	bit 1	bit 9
	bit 2	bit 10
	bit 3	bit 11
Packet 4	bit 0	bit 12
	bit 1	bit 13
	bit 2	bit 14
	bit 3	bit 15

4.9.2 Receive/Transmit Buses Interface Timing

CLKWD and signals of the data buses are clocked on the rising edge of the master clock (CLKM).

TX data are sampled on the rising edge of the master clock (CLKM) on the AFE chip.

CLKWD and RX data are sampled on the falling edge of the master clock in the modem chip.

The word clock pulse (CLKWD) is used as first (TX) packet reference. The packet sampled when CLKWD is high is considered to be the first. The binary information is then interpreted among four master clock periods. The following pseudo-code depicts how the data needs to be interpreted.

```
if (CLKM'event) and (CLKM = '1') then
        if (CLKWD = 1) then
                packet_counter <= 0
        else
                packet_counter <= packet_counter+1
        endif
        word_received(4*packet_counter,4*packet_counter+3) <= bit_packet
endif
```

Figure 14. TX-RX digital interface timing

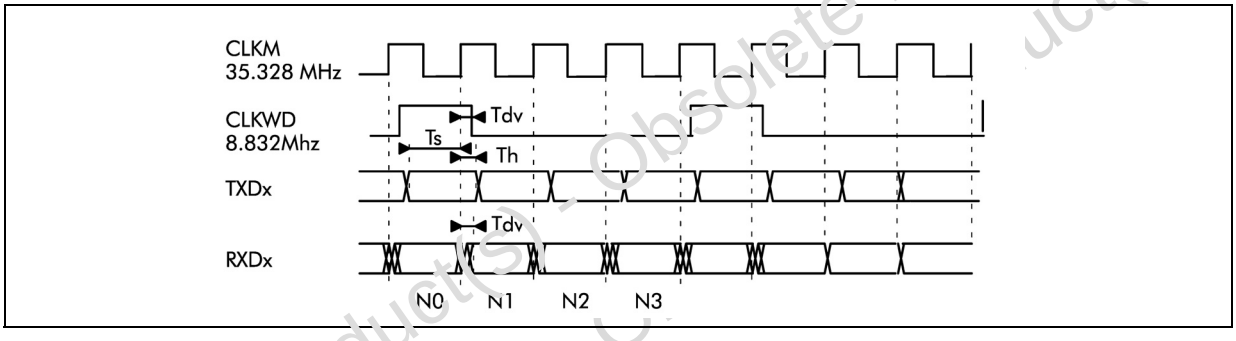


Table 18. Data interface timing requirements.

Symbol	Parameter	Min	Typ	Max	Remarks
Ts	Setup time	0.5ns	-	-	
Th	Hold time	0.2ns	-	-	
Tdv	Data valid	0.5ns	-	4ns	

4.9.3 TX data format

The digital dynamic of the DAC is 16 bits, signed representation. The following figure depicts the binary representation of TX interface.

Table 19. TX bit map

Sign	b14	B13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0

Two different DAC interfaces can be considered selected by the DAC_LIPARI bit as follows:

DAC_LIPARI = 0: All 16 bit TX interface sent to the DAC. Signed bit is inverted in order to be compatible with the unsigned representation of the DAC code. DAC_LIPARI = 1: Digital block provides a clamping of the TX received code such as maximal positive number is 2^14 -1, the most negative number is -2^14. In order to feed the full DAC dynamique, the code is then multiplied by 2 and sent to the DAC. LSB of the 16 bit DAC is consequently always 0. Signed bit is inverted in order to be compatible with the unsigned representation of the DAC code.

The TX interface can also be used to force the driver in mute mode synchronously by setting the DAC_TRIG_MUTE and MUTE_LD_AUTO registers. When DAC_TRIG_MODE is selected, the trigger condition is the LSB (b0) of the TX interface. The corresponding bit of the DAC code will be forced to zero. When DAC_TRIG_MODE = 0 and MUTE_LD_AUTO = 1, the trigger condition is the GP0 input pin. MUTE_LD_FORCE register continuously forces the driver in mute mode.
A summary of all 3 driver control modes is presented in the following table:

Table 20.

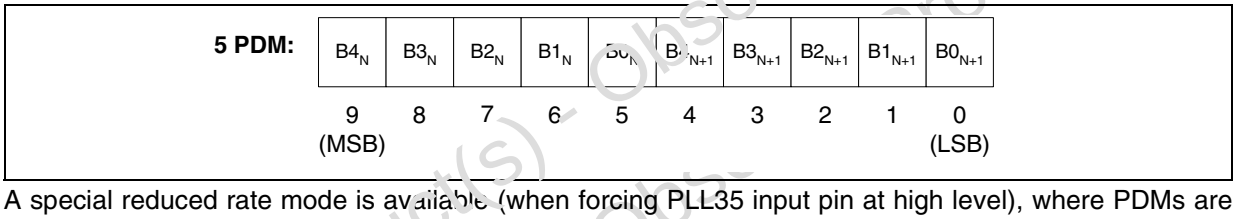
MUTE_LD_FORCE	MUTE_LD_AUTO	DAC_TRIG_MODE	DAC lsb	GP0 pin	Driver mode
0	0	x	x	x	Normal
1	x	x	x	x	Mute
0	1	1	0	x	Normal
0	1	1	1	x	Mute
0	1	0	x	0	Normal
0	1	0	x	1	Mute

Note: 1. "x" means "don't care"

4.9.4 RX data format

The dynamic of the signal from the ADC is limited to 5 bits(PDM4 to PDM0). This PDM stream runs at 70MHz (or at 35MHz in reduced rate mode) and will be multiplexed to limit the IO frequency to 35MHz.

Figure 15. RX bit map in normal mode



A special reduced rate mode is available (when forcing PLL35 input pin at high level), where PDMs are received at half the rate (35 MHz). So in this case, only the even (N) words are read from the AFRXD pins. Odd (N+1) words are "X" level.

4.9.5 Power Down Mode

The ST20184 is placed in power down mode when the pin PWD is high.

The chip status is as followed:

- Crystal driver and VCXODAC are active
- CLKM and CLKWD are generated.
- Digital blocks are active except for the RX IO's - they are at low level.
- Analog RX and TX are in power down.
- TX driver in power down (no signal transmitted) but output pins TXP and TXN in high impedance status.

4.9.6 Reset Mode

The ST20184 is placed in reset mode when the RESETN pin is pulled to ground (active low signal) (not active in test mode).

The chip status is as followed:

- Initial values for the registers are listed in the register table
- Crystal driver in power up: CLKM signal available after the lock time (see PLL block)
- CLKWD is not generated. The pin stays at high level.
- VCXODAC not active.
- Digital blocks are in reset: no activity.
- Analog blocks are in power down (All PD registers high except those requiring a test mode)
- TX driver in power down but output pins TXP and TXN in high impedance status.

5 Electrical Ratings and Characteristics

5.1 Absolute Maximum Ratings

Operation of the device beyond these limits may cause permanent damage. It is not implied that more than one of these conditions can be applied simultaneously.

Table 21. Power Supply Ratings

Parameter	Description	Condition	Min	Max	Unit
$AVDD5_{ABSM}$	Abs. max. analog 5V power supply		AVSS-0.3	5.5	V
$AVDD25_{ABSM}$	Abs. max. analog 2.5V power supply		AVSS-0.3	2.8	V
$DVDD_{ABSM}$	Abs. max. digital power supply		DVSS-0.3	2.8	V
DVDD-$AVDD25_{ABSM}$	Abs. max. difference between digital and analog power supply		-0.3	0.3	V
DVSS-$AVSS5_{ABSM}$	Abs. max. difference between digital and 5V analog ground		-0.3	0.3	V
DVSS-$AVSS25_{ABSM}$	Abs. max. difference between digital and 3V analog ground		-0.3	0.3	V

Table 22. Signal Pin Ratings

Parameter	Description	Condition	Min	Max	Unit
VIN_{ABSM}	Abs. max. input for normal digital and analog inputs		VSS-0.3	VDD+0.3	V
$VOUT_{ABSM}$	Abs. max. voltage at any output pin	-	VSS-0.3	VDD+0.3	V

5.2 Operating Conditions

Total cumulative dwell time outside the normal power supply voltage range or the ambient temperature under bias, must be less than 0.1% of the useful life.

The following operating ranges define the limits for functional operation and functionality outside these limits are not implied.

Table 23. Operating Conditions

Parameter	Description	Condition	Min	Typ	Max	Unit
AVDD5	5V analog power supply voltage range		4.75	5	5.25	V
AVDD25	2.5V analog power supply voltage range		2.375	2.5	2.625	V
DVDD25	2.5V digital power supply voltage range		2.375	2.5	2.625	V
DVDD33	Digital power supply voltage range		3.135	3.3	3.465	V
Tamb	Ambient temperature		-40		85	°C
Tj	Junction temperature		-40		125	°C
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction to Ambient			45.5		°C/W
Psij-c				0.6		°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction to Case			12.1		°C/W

5.3 Static Characteristics

5.3.1 Digital Inputs

Digital Schmitt-trigger inputs: Txi, CTRLIN, PDOWN, RESETN, TEST

Table 24. Schmitt trigger input characteristics

Parameter	Description	Condition	Min	Max	Unit
VIL	Low input voltage	-		.2*DVDD33	V
VIH	High input voltage	-	.8*DVDD33		V
VH	Hysteresis	-	1.0	1.3	V
Ileak	Input leakage current	-	-10	10	µA
Cinp	Input capacitance	-		3	pF

5.3.2 Digital Outputs

Digital Outputs: Rxi, CLKWD, Gpi, DRVi, DRVSD

Table 25. Digital output characteristics

Parameter	Description	Condition	Min	Max	Unit
VOL	Low output voltage	Iout=-4mA	-	.15*DVDD33	V
VOH	High output voltage	Iout=4mA	.85*DVDD33	-	V
Cload	Load capacitance	-		15	pF

5.3.3 Clock Output: CLKM

Table 26. CLKM output characteristics

Parameter	Description	Condition	Min	Max	Unit
VOL	Low output voltage	Iout=-4mA		.15*DVDD33	V
VOH	High output voltage	Iout=4mA	.85*DVDD33		V
Cload	Load capacitance			15	PF
Dcycle	Duty cycle		45	55	%

5.3.4 Power Budget

Table 27. Current Consumption

Parameter	Description	Condition	Typ	Max	Unit
Pd	Power dissipation in power up	12dBm on line	0.75	1.0	W
I_{AVDD5}	AVDD5 power up current consumption	12dBm on line	110		mA
I_{AVDD25} (Generated internally from 3.3V)	AVDD25 power up current consumption		44		mA
I_{DVDD}	DVDD power up current consumption		14		mA

5.4 PIN DESCRIPTION AND ASSIGNMENT

Table 28. Pinning Description ST-20184 AFE

Pin	Name	Description	Connection	Type	Dir.	Main Charac.
Digital interface						
85	DVSS25	Negative supply for digital core	Dig supply	Direct	Bi	Z≈0Ω
84	DVDD25	Positive supply for digital core	Dig supply	Direct	Bi	Z≈0Ω; 2.5V
4 87	DVDD33	Positive supply for digital IOs	Dig supply	Direct	Bi	Z≈0Ω; 3.3V
3 88	DVSS33	Negative supply for digital IOs	Dig supply	Direct	Bi	Z≈0Ω
73	TX3	Transmit data bus bit 3 (MSB)	Modem	Schmitt	In	High Z
74	TX2	Transmit data bus bit 2	Modem	Schmitt	In	High Z
75	TX1	Transmit data bus bit 1	Modem	Schmitt	In	High Z
76	TX0	Transmit data bus bit 0 (LSB)	Modem	Schmitt	In	High Z
77	CTRLIN	Serial control interface input	Modem	Schmitt	In	High Z
100	CTRLOUT	Serial control interface output	Modem	Tristate	Out	Imax=4mA Cmax=20pF
1	CLKM	Master clock output	Modem	Tristate	Out	Imax=4mA Cmax=20pF
2	CLKWD	Word clock output	Modem	Tristate	Out	Imax=4mA Cmax=20pF
89	RX9	Receive data bus bit 9 (MSB)	Modem	Tristate	Out	Imax=4mA Cmax=20pF
90	RX8	Receive data bus bit 8	Modem	Tristate	Out	Imax=4mA Cmax=20pF
91	RX7	Receive data bus bit 7	Modem	Tristate	Out	Imax=4mA Cmax=20pF
92	RX6	Receive data bus bit 6	Modem	Tristate	Out	Imax=4mA Cmax=20pF
93	RX5	Receive data bus bit 5	Modem	Tristate	Out	Imax=4mA Cmax=20pF
94	RX4	Receive data bus bit 4	Modem	Tristate	Out	Imax=4mA Cmax=20pF
95	RX3	Receive data bus bit 3	Modem	Tristate	Out	Imax=4mA Cmax=20pF
96	RX2	Receive data bus bit	Modem	Tristate	Out	Imax=4mA Cmax=20pF
97	RX1	Receive data bus bit 1	Modem	Tristate	Out	Imax=4mA Cmax=20pF

Table 28. Pinning Description ST-20184 AFE (continued)

Pin	Name	Description	Connection	Type	Dir.	Main Charac.
98	RX0	Receive data bus bit 0 (LSB)	Modem	Tristate	Out	Imax=4mA Cmax=20pF
70	PWD	General power down	Modem	Schmitt	In	'1': power down
99	GASPO	Dying Gasp output	Modem	Tristate	Out	Imax=4mA Cmax=20pF
86	PLL35	PLL 35/70MHz	Strap	Schmitt	In	High Z
71	RESETN	General reset (active low)	System	Schmitt	In	'0': reset
Analog interface						
66 64 63 62 56	AVSS25ADC	ADC analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
67 65 61 55	AVDD25ADC	ADC analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
69	DVDD25ADC	ADC digital positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
68	DVSS25ADC	ADC digital negative supply	Ana supply	Direct	Bi	Z≈0Ω
60	ExtRes	External resistance for bias (3k75-1%)	R network	Analog	Bi	DC current
59	Vcm	ADC virtual ground decoupling	C network	Analog	Bi	No DC current
57	Vrefn	ADC negative reference decoupling	C network	Analog	Bi	No DC current
58	Vrefp	ADC positive reference decoupling	C network	Analog	Bi	No DC current
25	AVDD5DRV	Internal TX driver positive supply	Ana supply	Direct	Bi	Z≈0Ω; 5V
24	AVSS5DRV	Internal TX driver negative supply	Ana supply	Direct	Bi	Z≈0Ω
31	TXNFB	TX driver negative feedback node	TX FBN	Analog	In	
26	TXPFB	TX driver positive feedback node	TX FBP	Analog	In	
23	PRTXN	Analog Predriver TX signal negative output	TX output	Ana 5V	Out	V_{CM} = AVDD5/2
22	PRTXP	Analog Predriver TX signal positive output	TX output	Ana 5V	Out	V_{CM} = AVDD5/2
30	OUTN	Analog TX signal negative output	TX output	Ana 5V	Out	V_{CM} = AVDD5/2
27	OUTP	Analog TX signal positive output	TX output	Ana 5V	Out	V_{CM} = AVDD5/2
29	AVDD5PWR	Internal TX driver positive supply for Line N	Ana supply	Direct	Bi	Z≈0Ω
28	AVSS5PWR	Internal TX driver negative supply for Line N	Ana supply	Direct	Bi	Z≈0Ω

Table 28. Pinning Description ST-20184 AFE (continued)

Pin	Name	Description	Connection	Type	Dir.	Main Charac.
5	GP3	Analog general purpose control pin	Board	Tristate	Out	Imax=4mA Cmax=20pF
6	GP2	Analog general purpose control pin	Board	Tristate	Out	Imax=4mA Cmax=20pF
10	GP1	Analog general purpose control pin	Board	Schmitt	In	High Z
11	GP0	Analog general purpose control pin	Board	Schmitt	In	High Z
32	AVDD25LNA2	LNA2 analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
33	AVSS25LNA2	LNA2 analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
45	AVDD5RXFLT	RX BPF analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 5V
48	AVSS5RXFLT	RX BPF analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
51	AVSS5LNA1	LNA1 analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
54	AVDD5LNA1	LNA1 analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 5V
20	GASPI	Dying gasp input reference voltage	Board	Analog	In	High Z
46	RX1N	Analog RX1 signal negative input (diff) – LNA1a	RX input	Analog	In	V_{CM} forced at AVDD5/2
47	RX1P	Analog RX1 signal positive input (diff) – LNA1a	RX input	Analog	In	V_{CM} forced at AVDD5/2
53	RX2N	Analog RX2 signal negative input (diff) – LNA1c	RX input	Analog	In	V_{CM} forced at AVDD5/2
52	RX2P	Analog RX2 signal positive input (diff) – LNA1c	RX input	Analog	In	V_{CM} forced at AVDD5/2
49	RXON	Analog RX signal negative output (diff) – LNA1a	RX output	Analog	Bi	V_{CM} forced at AVDD5/2
50	RXOP	Analog RX signal positive output (diff) – LNA1a	RX output	Analog	Bi	V_{CM} forced at AVDD5/2
41	RX3N/T2N	Neg. diff input/output access for test and annex C	RX input	Analog	Bi	V_{CM}=AVDD5/2
42	RX3P/T2P	Pos. diff. Input/output access for test and annex C	RX input	Analog	Bi	V_{CM}=AVDD5/2
82	AVDD25PLL	PLL analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
83	AVSS25PLL	PLL analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
81	AVDD25XTAL	Crystal driver analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
78	AVSS25XTAL	Crystal driver analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
79	XTALO	Crystal driver connection 1	Crystal	Analog	Bi	X_{cap} sensitive
80	XTALI	Crystal driver connection 2	Crystal	Analog	Bi	X_{cap} sensitive
18	IVCXO	VCXO output current	Board	Analog	Out	High Z

Table 28. Pinning Description ST-20184 AFE (continued)

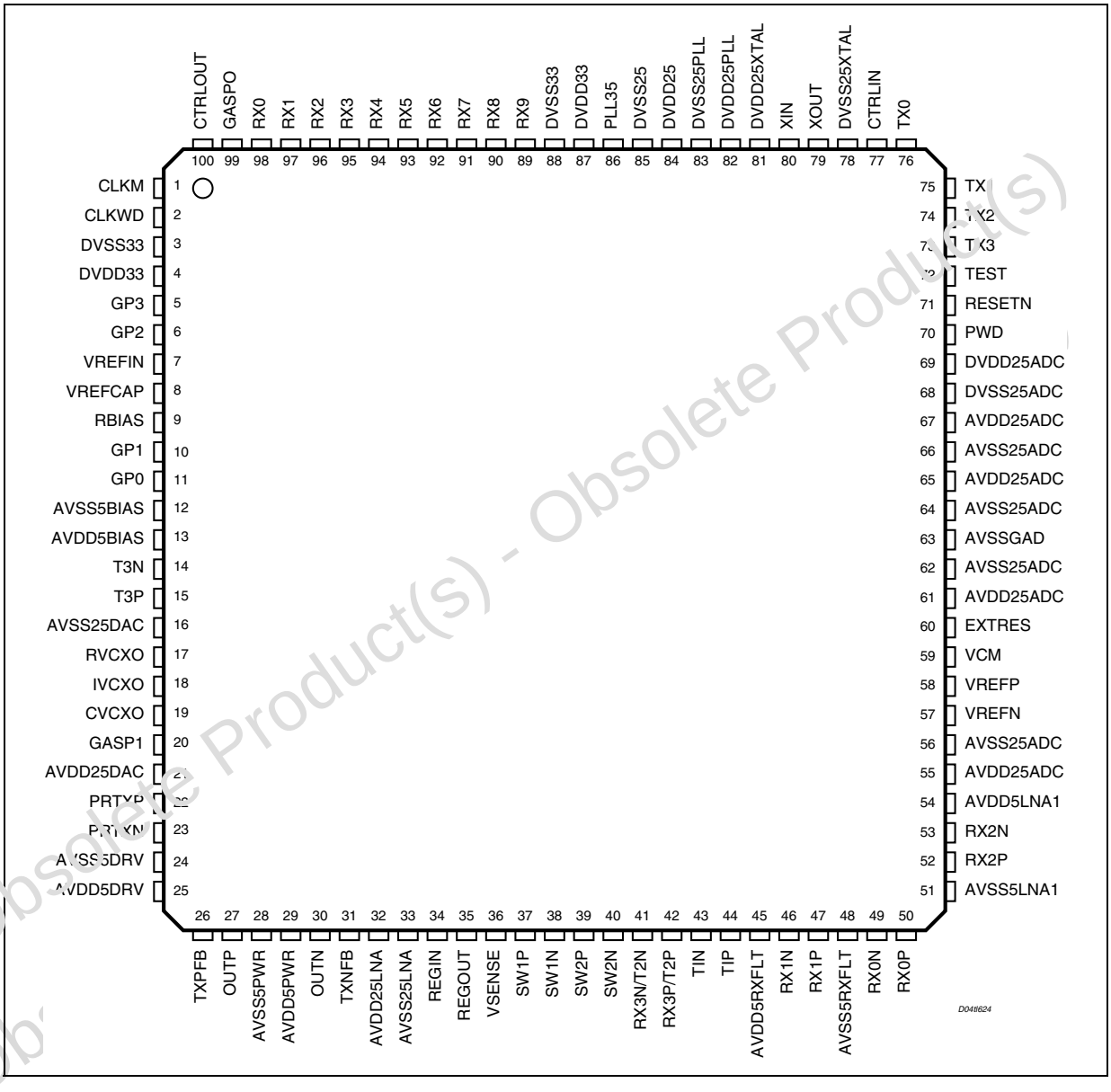
Pin	Name	Description	Connection	Type	Dir.	Main Charac.
17	RVCXO	VCXO reference resistor	Board	Analog	Bi	R = 12.5kΩ
19	CVCXO	VCXO external filter	Board	Analog	Bi	External cap
21	AVDD25DAC	DAC analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 2.5V
16	AVSS25DAC	DAC analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
13	AVDD5BIAS	Bias analog positive supply	Ana supply	Direct	Bi	Z≈0Ω; 5V
12	AVSS5BIAS	DAC analog negative supply	Ana supply	Direct	Bi	Z≈0Ω
9	RBIAS	Biasing current – R = 25kΩ 1%	R network	Analog	Bi	DC current
7	Vrefin	5V reference voltage	Input	Analog	In	Z≈0Ω
8	Vrefcap	Decoupling cap	Board	Analog	Bi	External cap
34	REGIN	Regulator input (3.3V)	Ana supply	Direct	Bi	Z≈0Ω
35	REGOUT	Regulator output (2.5V)	Ana supply	Direct	Out	Z≈0Ω
36	VSENSE	Regulator sense	Input	Analog	In	High Z
Mode selection interface						
72	TEST	Test mode selection (static)	Strap	Schmitt	In	High Z
Analog test access interface						
14	T3N	Neg. diff input/output test access	Test	Analog	Bi	V_{CM}=AVDD5/2
15	T3P	Pos. diff. Input/output test access	Test	Analog	Bi	V_{CM}=AVDD5/2
41	T2N/RX3N	Neg. diff input/output access for test and annex C	Test	Analog	Bi	V_{CM}=AVDD5/2
42	T2P/RX3P	Pos. diff. Input/output access for test and annex C	Test	Analog	Bi	V_{CM}=AVDD5/2
44	T1P	Pos. diff output test access	Test	Analog	Bi	V_{CM}=AVDD5/2
43	T1N	Neg. diff output test access	Test	Analog	Bi	V_{CM}=AVDD5/2
Others						
38	SW1N	Neg. diff input/output test access	Hybrid	Analog	Bi	V_{CM}=AVDD25/2
37	SW1P	Pos. diff. Input/output test access	Hybrid	Analog	Bi	V_{CM}=AVDD25/2
40	SW2N	Pos. diff output test access	Hybrid	Analog	Bi	V_{CM}=AVDD25/2
39	SW2P	Neg. diff output test access	Hybrid	Analog	Bi	V_{CM}=AVDD25/2

N.B. The digital interface can be supplied at a voltage below 3.3V if needed (Min.=2.7V).

5.5 PACKAGE AND PIN-OUT

A TQFP 100 pin package is used. The pin pitch is 0.5mm. The package dimension is 14*14*1.4mm. The pinout is shown in the Figure below.

Figure 16. Package ST20184

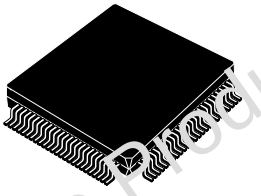


6 Package Information

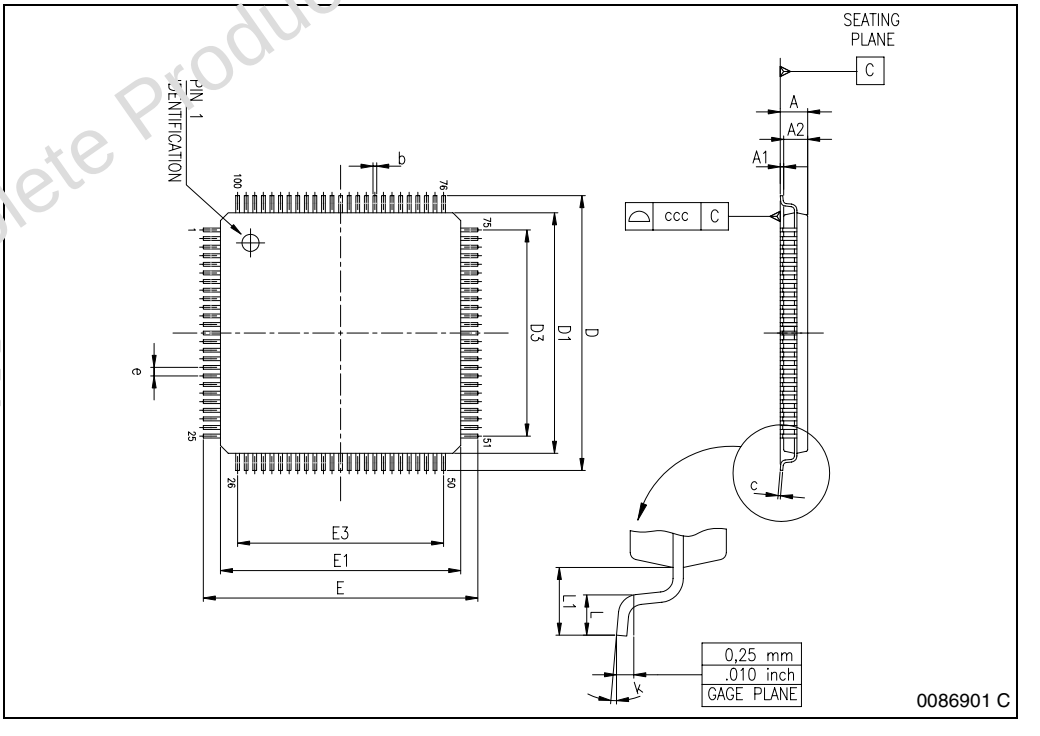
Figure 17. Xxxxx Mechanical Data & Package Dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.020	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0° (min.), 3.5° (typ.), 7°(max.)					
ccc		0.080			0.003	

OUTLINE AND MECHANICAL DATA



TQFP100
(14x14x1.40mm)



7 Revision History

Table 29. Revision History

Date	Revision	Description of Changes
February 2005	1	First Issue

Table of Contents

1 OVERVIEW 1
2 FEATURES 1
3 GENERAL DESCRIPTION 2
4 FUNCTIONAL DESCRIPTION 2
4.1 THE RECEIVER (RX) 2
4.2 THE TRANSMITTER (TX) 3
4.3 FILTER TUNING AND DYING GASP 3
4.4 THE DIGITAL INTERFACE 3
4.5 ATU-R BLOCK DIAGRAM 4
4.6 ST20184 RX PATH 5
4.6.1 LOW NOISE AMPLIFIER (LNA1) 5
4.6.2 RX INTEGRATED HIGH PASS FILTER 7
4.6.3 LOW NOISE AMPLIFIER (LNA2) 7
4.6.4 RX LOW PASS FILTER 8
4.6.5 A/D CONVERTER 8
4.7 ST20184 TX PATH 8
4.7.1 TX DRIVER 8
4.7.2 TX LOW PASS FILTER 9
4.7.3 DIGITAL TO ANALOG CONVERTER (DAC) 10
4.7.4 PLL BASED FREQUENCY MULTIPLIER 10
4.7.5 DYING GASP 10
4.7.6 VOLTAGE REGULATOR 11
4.7.7 POWER-ON-RESET CIRCUIT 11
4.7.8 HYBRID SWITCHES 12
4.8 DIGITAL INTERFACE 12
4.8.1 DIGITAL INTERFACE BLOCKS 12
4.8.2 MASTER AND WORD CLOCK 12
4.8.3 CONTROL INTERFACE (CTRLIN/OUT PINS) 13
4.8.4 WRITE ACCESS TO THE ST20184 INCLUDE THE CONTROL INTERFACE BIT MAPPING (SEE EXTRA WORD DOCUMENT) 13
4.8.5 READ ACCESS TO THE ST20184 13
4.8.6 CONTROL INTERFACE TIMING 14
4.8.7 CONTROL INTERFACE BIT MAPPING 14
4.9 RECEIVE/TRANSMIT INTERFACE 19
4.9.1 TRANSMIT INTERFACE DATA REPRESENTATION 19
4.9.2 RECEIVE/TRANSMIT BUSES INTERFACE TIMING 20
4.9.3 TX DATA FORMAT 20
4.9.4 RX DATA FORMAT 21
4.9.5 POWER DOWN MODE 21
4.9.6 RESET MODE 21
5 ELECTRICAL RATINGS AND CHARACTERISTICS 22
5.1 ABSOLUTE MAXIMUM RATINGS 22
5.2 OPERATING CONDITIONS 22
5.3 STATIC CHARACTERISTICS 23
5.3.1 DIGITAL INPUTS 23
5.3.2 DIGITAL OUTPUTS 23
5.3.3 CLOCK OUTPUT: CLKM 23
5.3.4 POWER BUDGET 23
5.4 PIN DESCRIPTION AND ASSIGNMENT 24
5.5 PACKAGE AND PIN-OUT 28
6 PACKAGE INFORMATION 29
7 REVISION HISTORY 30