



STL80NF3LL

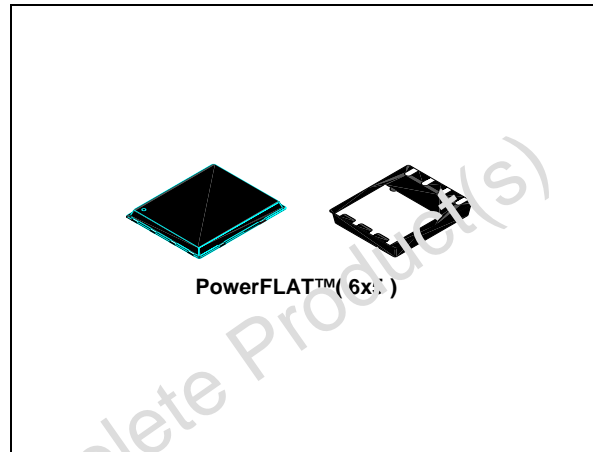
N-channel 30V - 0.0045Ω - 80A - PowerFLAT™ (6x5)
STripFET™ II Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STL80NF3LL	30V	<0.0055Ω	20A ⁽¹⁾

1. When mounted on FR-4 board of 1in², 2oz Cu.,
t<10sec

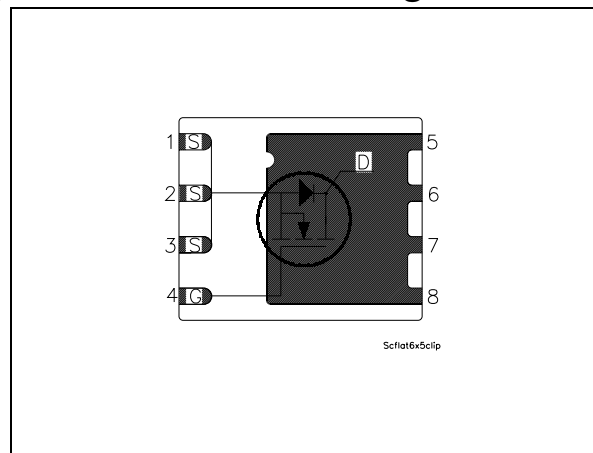
- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Conduction losses reduced
- Switching losses reduced



Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The Chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STL80NF3LL	L80NF3LL	PowerFLAT™ (6x5)	Tape & reel

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS}=0$)	30	V
V_{GS}	Gate- source voltage	± 16	V
$I_D^{(1)}$	Drain current (continuous) at $T_C=25^\circ\text{C}$	80	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100^\circ\text{C}$	50	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80	A
$I_D^{(3)}$	Drain current (continuous) at $T_C=25^\circ\text{C}$	20	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C=25^\circ\text{C}$	4	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C=25^\circ\text{C}$	30	W
	Derating factor(2)	0.03	W/ $^\circ\text{C}$
T_{stg}	Storage temperature	- 55 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. The value is rated according Rthj-c.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of 1in², 2oz Cu., t<10sec

Table 2. Thermal resistance

Symbol	Parameter	Value	Unit
R_{thj-c}	Thermal resistance junction-case (drain)	1.56	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal operating junction-pcb	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1in², 2oz Cu., t<10sec

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating, @ } 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 16 V$			± 10	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10 V, I_D = 10 A$ $V_{GS} = 4.5 V, I_D = 10 A$		0.0045 0.0055	0.0055 0.007	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10 V, I_D = 10 A$		37		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 V, f = 1 \text{ MHz},$ $V_{GS} = 0$		2160 614 98		pF pF pF
R_G	Gate input resistance	$f = 1 \text{ MHz}$ Gate DC Bias = 0 Test signal level = 20mV open drain		4.1		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15 V, I_D = 10 A,$ $V_{GS} = 4.5 V$ Figure 14		26 7 12	35	nC nC nC

1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$, $I_D = 10\text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 4.5\text{ V}$ <i>Figure 13</i>		23.5		ns
t_r	Rise time			39		ns
$t_{d(off)}$	Turn-off-delay time			47.5		ns
t_f	Fall time			37		ns

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				20	A
I_{SDM} (3)	Source-drain current (pulsed)				30	A
V_{SD} (4)	Forward on voltage	$I_{SD} = 20\text{ A}$, $V_{GS} = 0$			1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = 20\text{ A}$, $V_{DD} = 15\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}$, $T_j = 150^\circ\text{C}$ <i>Figure 18</i>		39		ns
Q_{rr}	Reverse recovery charge			45		nC
I_{RRM}	Reverse recovery current			2.3		A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

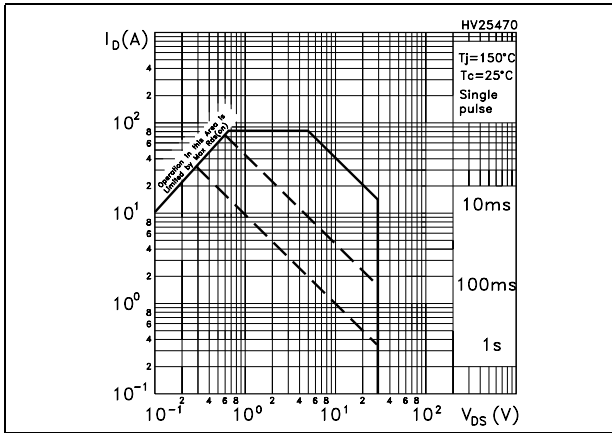


Figure 2. Thermal impedance

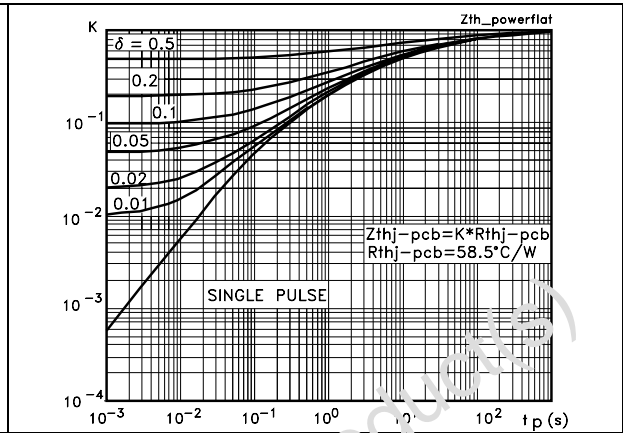


Figure 3. Output characteristics

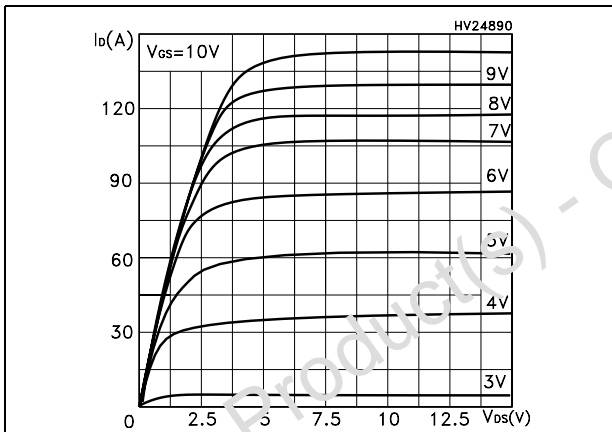


Figure 4. Transfer characteristics

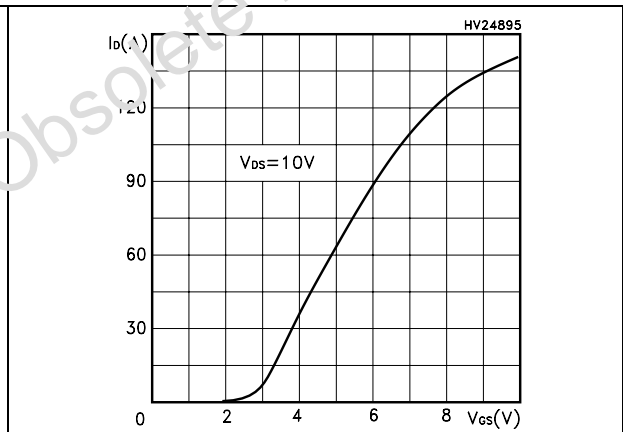


Figure 5. Transconductance

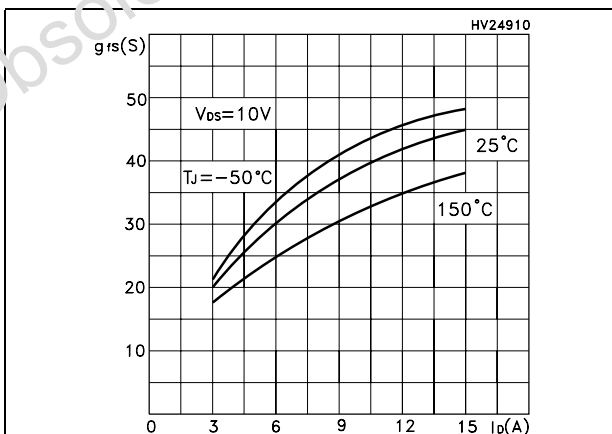


Figure 6. Static drain-source on resistance

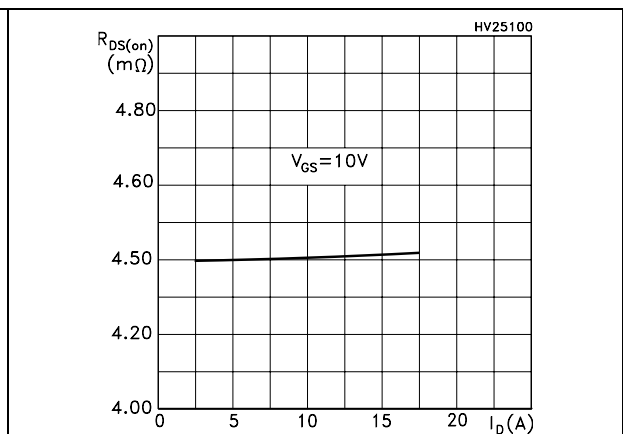


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

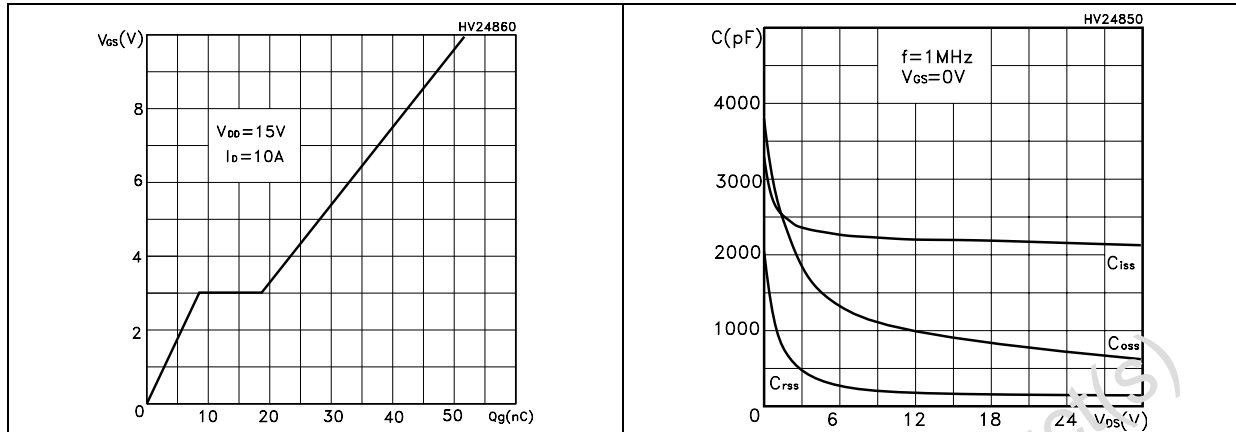


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

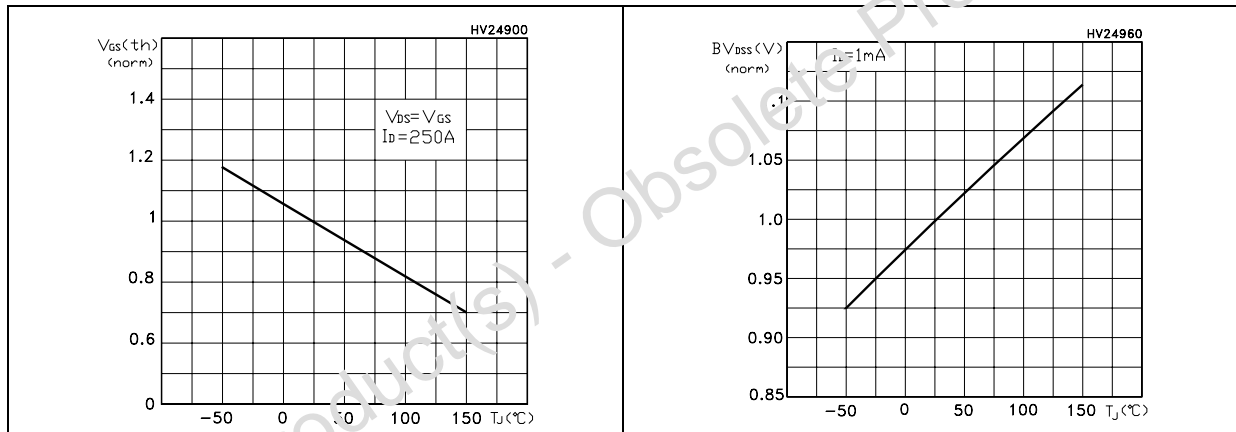
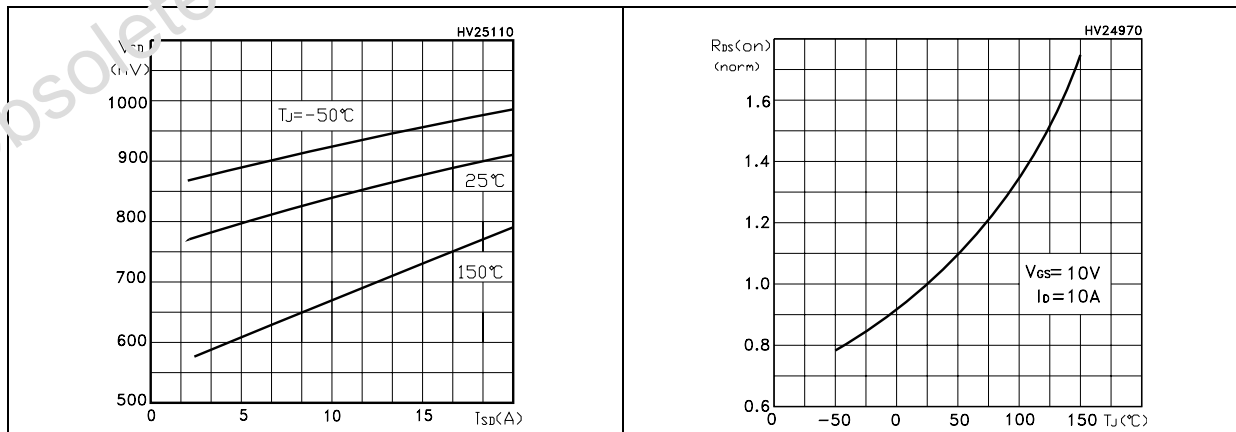


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized $B_{V_{DS}}$ vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

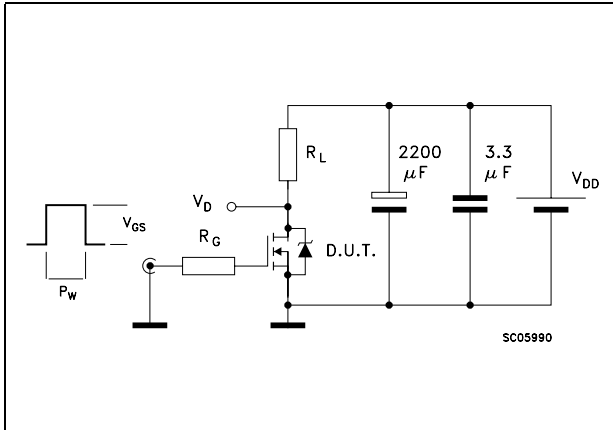


Figure 14. Gate charge test circuit

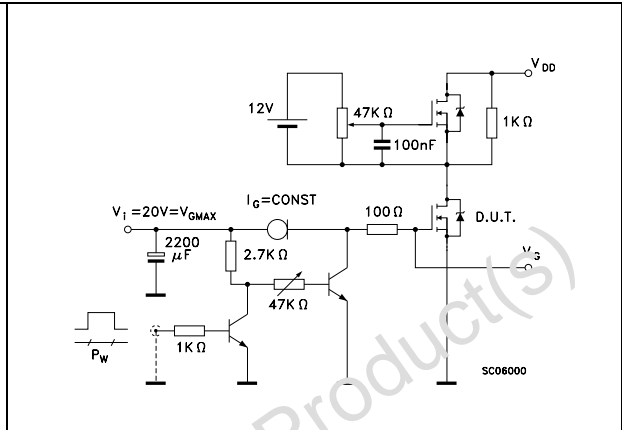


Figure 15. Test circuit for inductive load switching and diode recovery times

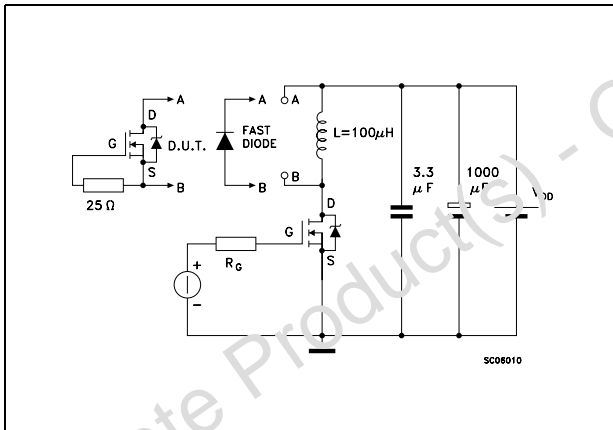


Figure 16. Unclamped inductive load test circuit

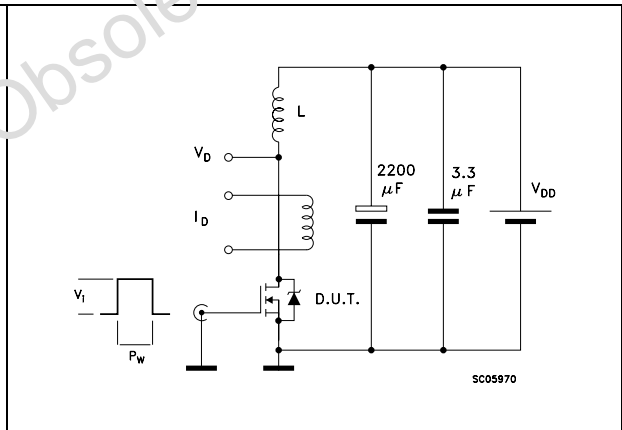


Figure 17. Unclamped inductive waveform

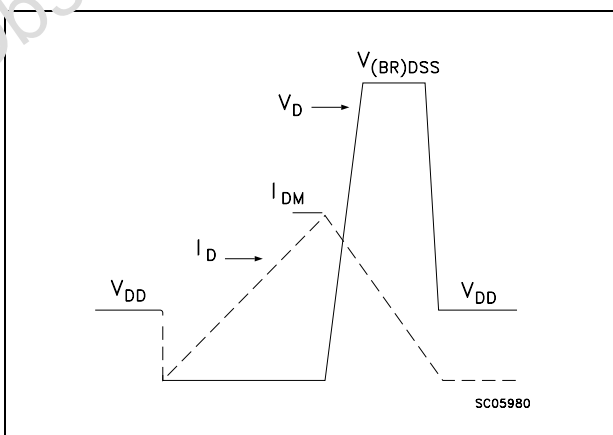
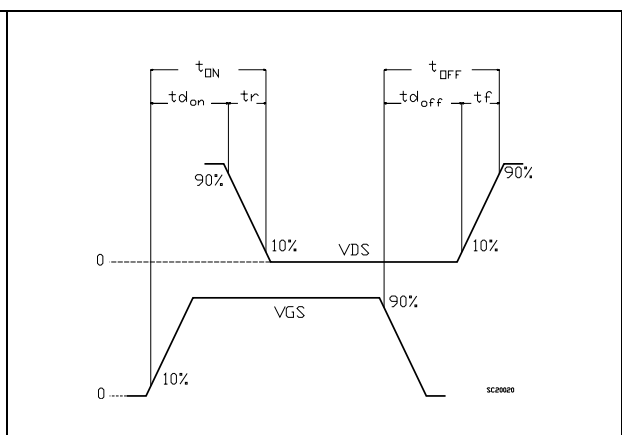


Figure 18. Switching time waveform



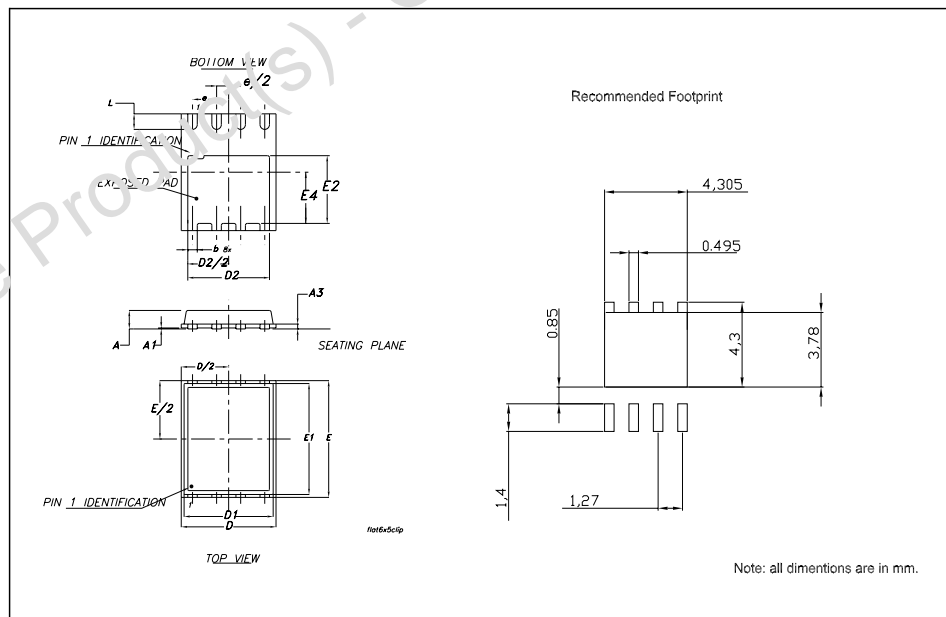
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Obsolete Product(s) - Obsolete Product(s)

PowerFLAT™ (6x5) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.80	0.83	0.93	0.031	0.032	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



5 Revision history

Table 7. Revision history

Date	Revision	Changes
18-Apr-2005	1	First release.
20-Jun-2005	2	Updated mechanical data
22-Jun-2005	3	New R_G value on table 6
09-Jan-2006	4	New footprint
10-Jul-2006	5	Modified Figure 2 , new template

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