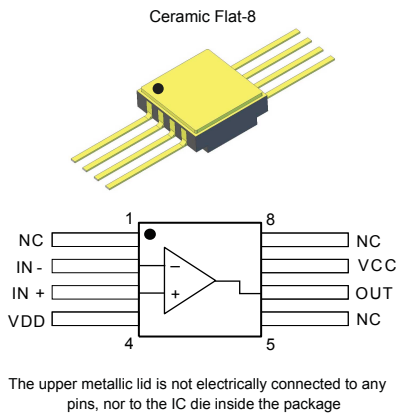


Rad-hard precision bipolar single operational amplifier



Features

- Rail-to-rail output
- Bandwidth: 8 MHz gain at 16 V
- Low input offset voltage: 100 μ V typ
- Supply current: 2.2 mA typ
- Operating from 3 to 16 V
- Input bias current: 30 nA typ
- ESD internal protection \geq 2 kV
- Latch-up immunity: 200 mA
- ELDRS free up to 300 krad
- SEL immune at 120 MeV.cm²/mg
- SMD pin: 5962F06237
- Mass: 0.4 g

Applications

- Space probes and satellites
- Defense systems
- Scientific instrumentation
- Nuclear systems

Description

The **RHF43B** is a precision, bipolar operational amplifier available in a ceramic Flat-8 package and in die form. In addition to its low offset voltage, rail-to-rail feature, and wide supply voltage, the **RHF43B** features a good immunity to radiations.

Maturity status link

[RHF43B](#)

1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage ⁽¹⁾	18	V
V_{id}	Differential input voltage ⁽²⁾	± 1.2	
V_{in}	Input voltage range ⁽³⁾	$V_{DD} - 0.3$ to 16	
I_{in}	Input current	45	mA
T_{stg}	Storage temperature	-65 to 150	°C
T_j	Maximum junction temperature	150	
R_{thja}	Thermal resistance junction to ambient area ^{(4) (5)}	125	°C/W
R_{thjc}	Thermal resistance junction to case ^{(4) (5)}	40	
ESD	HBM: human body model ⁽⁶⁾	2	kV
	Latch-up immunity	200	mA
	Lead temperature (soldering, 10 s)	260	°C

1. The supply voltage is defined as the difference between the voltages applied on the V_{CC} and V_{DD} pins.
2. The differential voltage is the non-inverting input terminal with respect to the inverting input terminal
3. The magnitude of the input and output voltage must never exceed $V_{CC} + 0.3$ V.
4. Short-circuits can cause excessive heating and destructive dissipation.
5. R_{th} are typical values.
6. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 16	V
V_{icm}	Common-mode input voltage	V_{DD} to V_{CC}	
T_{oper}	Operating free-air temperature range	-55 to 125	°C

2 Electrical characteristics

Table 3. 16 V supply: $V_{CC} = 16\text{ V}$, $V_{DD} = 0\text{ V}$, load to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
I_{CC}	Supply current	No load	125 °C		2.9	mA
			25 °C		2.5	
			-55 °C		2.9	
V_{io}	Offset voltage	$V_{icm} = V_{CC}/2$	125 °C	-500	500	μV
			25 °C	-300	100	
			-55 °C	-500	500	
DV_{io}	Input offset voltage drift			1		$\mu\text{V}/^\circ\text{C}$
I_{ib}	Input bias current	$V_{icm} = V_{CC}/2$	125 °C	-100	100	nA
			25 °C	-60	30	
			-55 °C	-100	100	
DI_{ib}	Input offset current temperature drift	$V_{icm} = V_{CC}/2$		100		$\text{pA}/^\circ\text{C}$
I_{io}	Input offset current	$V_{icm} = V_{CC}/2$	125 °C	-35	35	nA
			25 °C	-15	1	
			-55 °C	-35	35	
R_{in}	Differential input resistance between in+ and in-			0.16		M Ω
	Input resistance between in+ (or in-) and GND		25 °C	2000		
C_{in}	Differential input capacitance between in+ and in-			8		pF
	Input capacitance between in+ (or in-) and GND		25 °C	2		
CMR	Common mode rejection ratio	$0 < V_{icm} < 16\text{ V}$	125 °C	72		dB
			25 °C	72	110	
			-55 °C	72		
SVR	Supply voltage rejection ratio	$3\text{ V} < V_{CC} < 16\text{ V}$, $V_{icm} = V_{CC}/2$	125 °C	80		dB
			25 °C	90	120	
			-55 °C	80		
A_{VD}	Large signal voltage gain	$V_{out} = 0.5\text{ V to } 15.5\text{ V}$, $R_L = 1\text{ k}\Omega$, $0 < V_{icm} < 16\text{ V}$	125 °C	60		
			25 °C	74	85	
			-55 °C	60		
V_{OH}	High level output voltage	$R_L = 1\text{ k}\Omega$	125 °C	15.6		V
			25 °C	15.7	15.8	
		-55 °C	15.6			
		$R_L = 10\text{ k}\Omega$	125 °C	15.8		
V_{OH}	High level output voltage	$R_L = 10\text{ k}\Omega$	25 °C	15.9	15.96	V
			-55 °C	15.8		
V_{OL}	Low level output voltage	$R_L = 1\text{ k}\Omega$	125 °C		0.3	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit		
V_{OL}	Low level output voltage	$R_L = 1\text{ k}\Omega$	25 °C		0.1	0.2	V	
			-55 °C			0.3		
		$R_L = 10\text{ k}\Omega$	125 °C			0.1		
			25 °C		0.04	0.06		
			-55 °C			0.1		
I_{out}	Output sink current	$V_{out} = V_{CC}$	125 °C	15			mA	
			25 °C	20	30			
			-55 °C	15				
	Output source current	$V_{out} = V_{DD}$	125 °C	10				
			25 °C	15	25			
			-55 °C	10				
AC performance								
GBP	Gain bandwidth product	$f = 100\text{ kHz}, R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	125 °C	3.5			MHz	
			25 °C	6	8			
			-55 °C	3.5				
F_u	Unity gain frequency	$R_L = 1\text{ k}\Omega, C_L = 100\text{ pF}$	25 °C		5			
ϕ_m	Phase margin	Gain = 5, $R_L = 1\text{ k}\Omega,$ $C_L = 100\text{ pF}$	25 °C		50	Degrees		
SR	Slew rate	$R_L = 1\text{ k}\Omega, C_L = 100\text{ pF}$	125 °C	1.7			V/ μ s	
			25 °C	2	3			
			-55 °C	1.7				
e_n	Equivalent input noise voltage	$f = 1\text{ kHz}$	25 °C		7.5	nV/ $\sqrt{\text{Hz}}$		
i_n	Equivalent input noise current	$f = 1\text{ kHz}$	25 °C		1	pA/ $\sqrt{\text{Hz}}$		
THD+ e_n	Total harmonic distortion + noise	$V_{out} = (V_{CC} - 1\text{ V})/5,$ Gain = -5.1, $V_{icm} = V_{CC}/2$	25 °C		0.01	%		

Table 4. 3 V supply: $V_{CC} = 3\text{ V}$, $V_{DD} = 0\text{ V}$, load to $V_{CC}/2$ (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
DC performance							
I_{CC}	Supply current	No load	125 °C		2.6	mA	
			25 °C		2.2		2.6
			-55 °C				2.6
V_{IO}	Offset voltage	$V_{icm} = V_{CC}/2$	125 °C	-500		500	μV
			25 °C	-300	100	300	
			-55 °C	-500		500	
DV_{IO}	Input offset voltage drift			1		$\mu\text{V}/^\circ\text{C}$	
I_{IB}	Input bias current	$V_{CC} = 4\text{ V}$, $V_{icm} = V_{CC}/2$	125 °C	-100		100	nA
			25 °C	-60	30	60	
			-55 °C	-100		100	
DI_{IB}	Input offset current temperature drift	$V_{CC} = 4\text{ V}$, $V_{icm} = V_{CC}/2$		100		$\text{pA}/^\circ\text{C}$	
I_{IO}	Input offset current	$V_{CC} = 4\text{ V}$, $V_{icm} = V_{CC}/2$	125 °C	-35		35	nA
			25 °C	-15	1	15	
			-55 °C	-35		35	
R_{in}	Differential input resistance between in+ and in-			0.16		M Ω	
	Input resistance between in+ (or in-) and GND			2000			
C_{in}	Differential input capacitance between in+ and in-			8		pF	
	Input capacitance between in+ (or in-) and GND			2			
CMR	Common mode rejection ratio	$0 < V_{icm} < 3\text{ V}$	125 °C	72			dB
			25 °C	72	90		
			-55 °C	72			
A_{VD}	Large signal voltage gain	$V_{out} = 0.5\text{ V to } 2.5\text{ V}$, $R_L = 1\text{ k}\Omega$, $0 < V_{icm} < 3\text{ V}$	125 °C	60			
			25 °C	74	85		
			-55 °C	60			
V_{OH}	High level output voltage	$R_L = 1\text{ k}\Omega$	125 °C	2.8			V
			25 °C	2.9	2.95		
			-55 °C	2.8			
		$R_L = 10\text{ k}\Omega$	125 °C	2.9			
			25 °C	2.94	2.98		
			-55 °C	2.9			
V_{OL}	Low level output voltage	$R_L = 1\text{ k}\Omega$	125 °C			0.2	
			25 °C		0.05	0.1	
			-55 °C			0.2	
V_{OL}	Low level output voltage	$R_L = 10\text{ k}\Omega$	125 °C			0.1	V
			25 °C		0.02	0.06	
			-55 °C			0.1	

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{out}	Output sink current	$V_{out} = V_{CC}$	125 °C	15		mA
			25 °C	20	30	
			-55 °C	15		
	Output source current	$V_{out} = V_{DD}$	125 °C	10		
			25 °C	15	25	
			-55 °C	10		
AC performance						
GBP	Gain bandwidth product	$f = 100 \text{ kHz}, R_L = 1 \text{ k}\Omega,$ $C_L = 100 \text{ pF}$	125 °C	3.5		MHz
			25 °C	6	7.5	
			-55 °C	3.5		
F_u	Unity gain frequency	$R_L = 1 \text{ k}\Omega, C_L = 100 \text{ pF}$	25 °C		5	
ϕ_m	Phase margin	Gain = 5, $R_L = 1 \text{ k}\Omega,$ $C_L = 100 \text{ pF}$	25 °C		50	Degrees
SR	Slew rate	$R_L = 1 \text{ k}\Omega, C_L = 100 \text{ pF}$	125 °C	1.7		V/ μ s
			25 °C	2	2.7	
			-55 °C	1.7		
e_n	Equivalent input noise voltage	$f = 1 \text{ kHz}$	25 °C		7	nV/ $\sqrt{\text{Hz}}$
i_n	Equivalent input noise current	$f = 1 \text{ kHz}$	25 °C		0.8	pA/ $\sqrt{\text{Hz}}$
THD+ e_n	Total harmonic distortion + noise	$V_{out} = (V_{CC} - 1 \text{ V})/5,$ Gain = -5.1, $V_{icm} = V_{CC}/2$	25 °C		0.01	%

3 Electrical characteristic curves

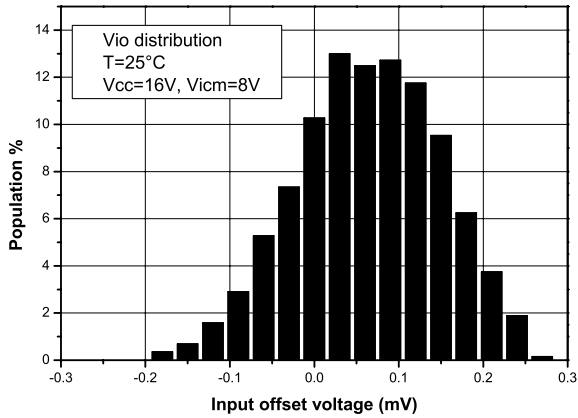
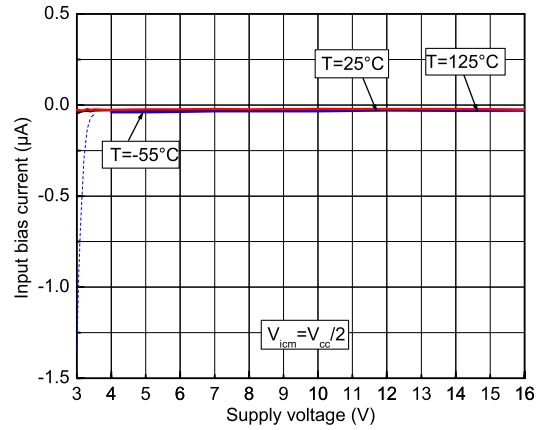
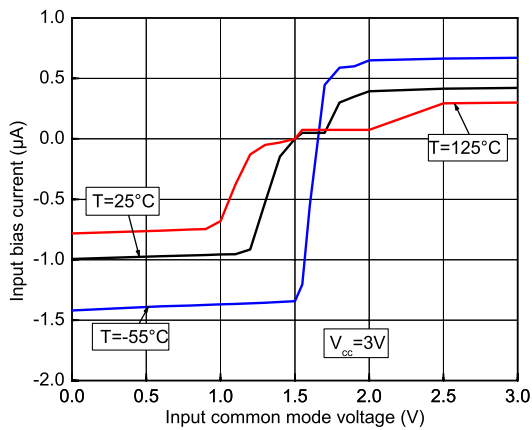
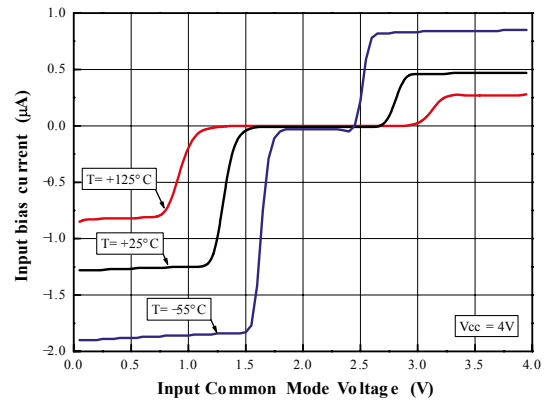
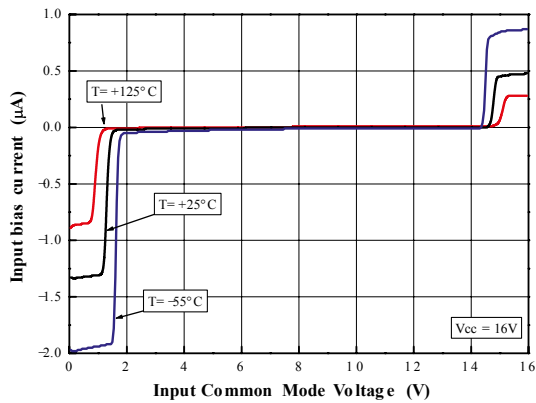
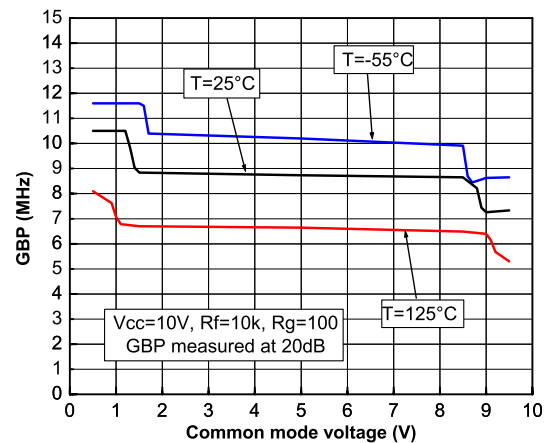
Figure 1. Input offset voltage distribution

Figure 2. Input bias current vs. supply voltage

Figure 3. Input bias current vs. Vicm at V_{CC} = 3 V

Figure 4. Input bias current vs. Vicm at V_{CC} = 4 V

Figure 5. Input bias current vs. Vicm at V_{CC} = 16 V

Figure 6. Gain bandwidth product vs. Vicm at V_{CC} = 10 V


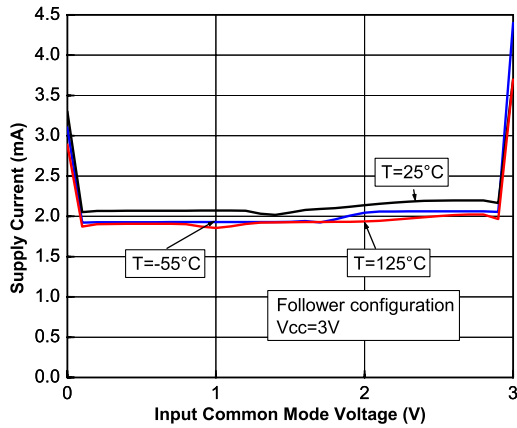
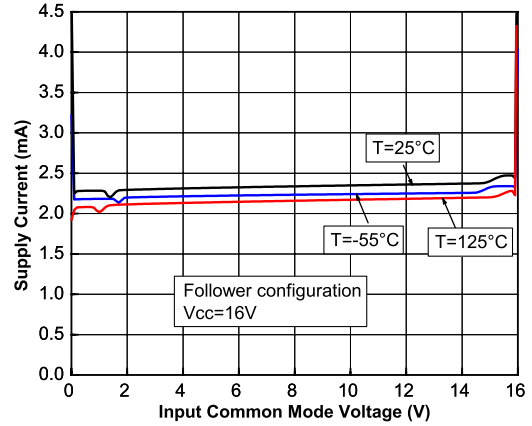
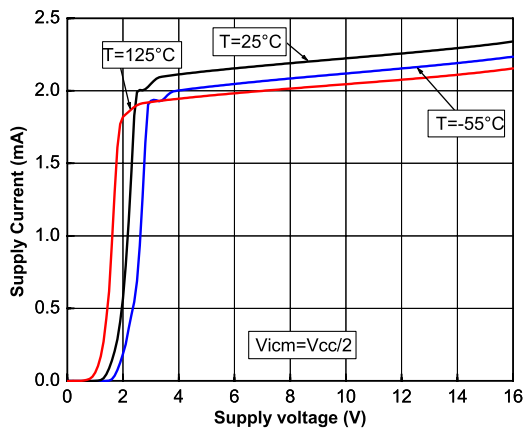
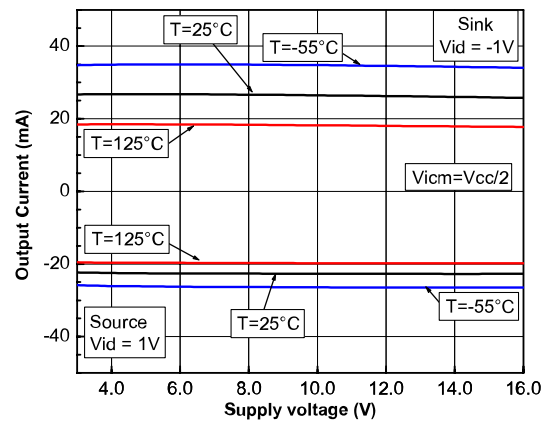
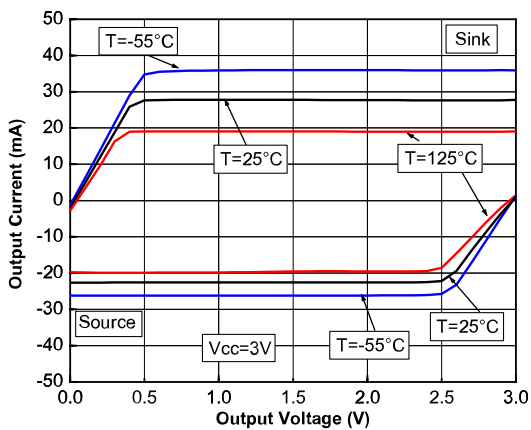
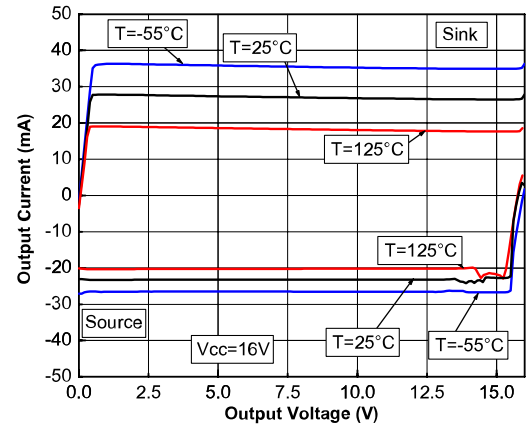
Figure 7. Supply current vs. Vicm in follower configuration at $V_{CC} = 3\text{ V}$

Figure 8. Supply current vs. Vicm in follower configuration at $V_{CC} = 16\text{ V}$

Figure 9. Supply current vs. supply voltage at $V_{icm} = V_{CC}/2$

Figure 10. Output current vs. supply voltage at $V_{icm} = V_{CC}/2$

Figure 11. Output current vs. output voltage at $V_{CC} = 3\text{ V}$

Figure 12. Output current vs. output voltage at $V_{CC} = 16\text{ V}$


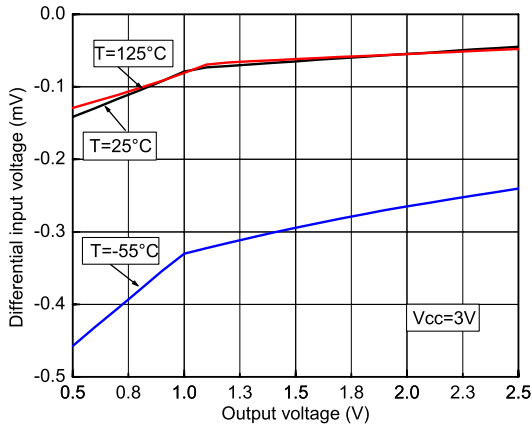
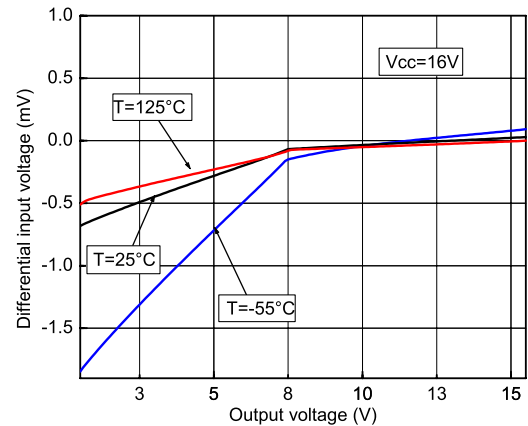
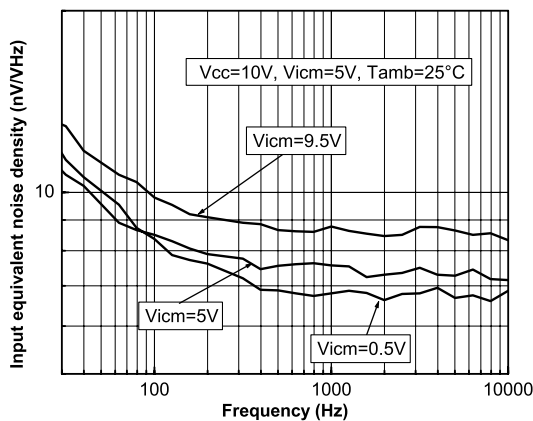
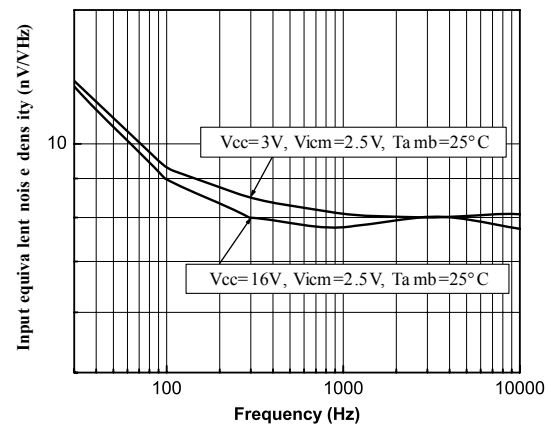
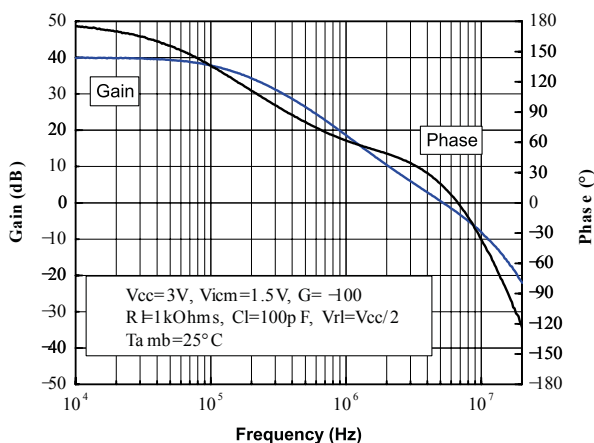
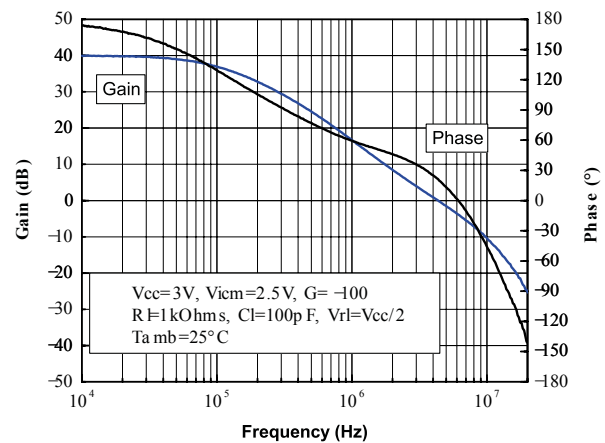
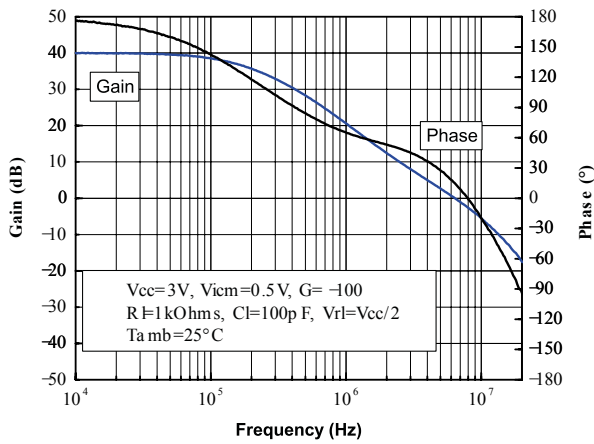
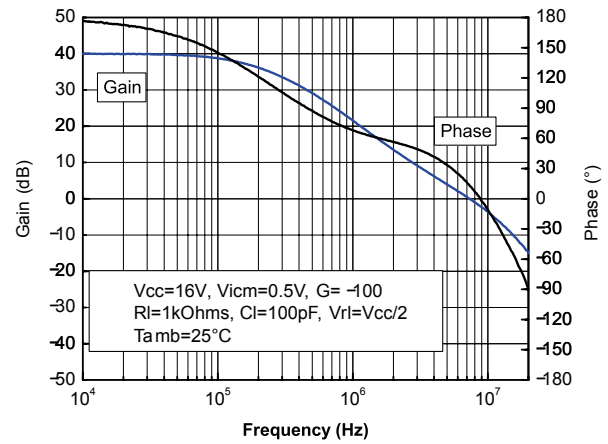
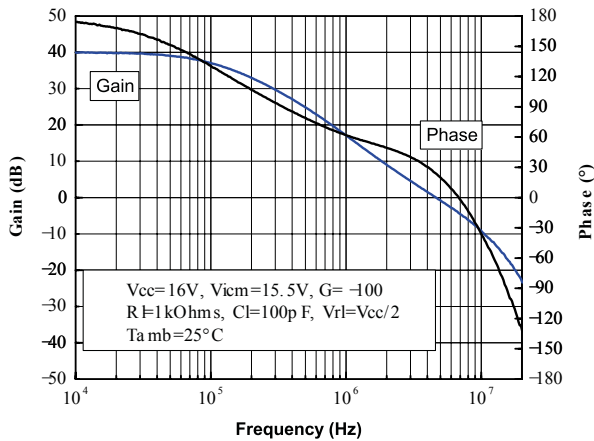
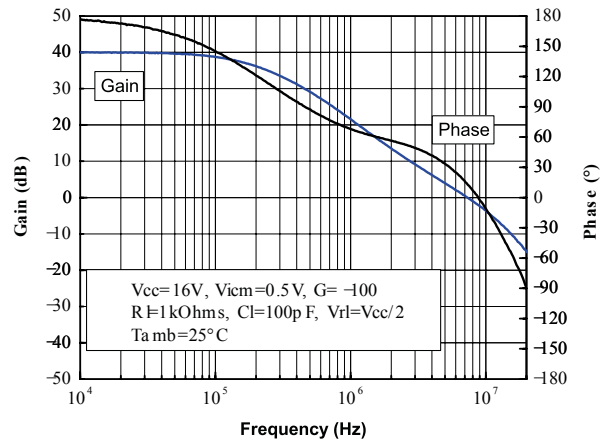
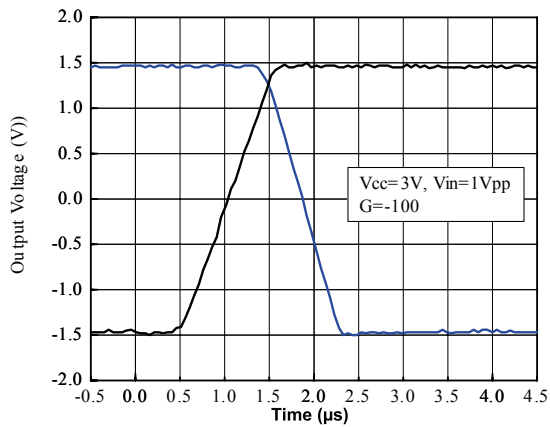
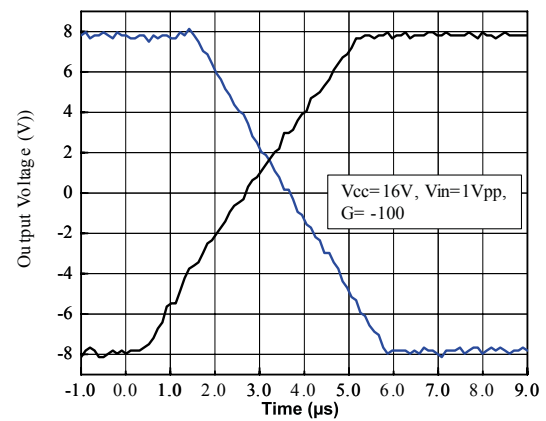
Figure 13. Differential input voltage vs. output voltage at $V_{CC} = 3\text{ V}$

Figure 14. Differential input voltage vs. output voltage at $V_{CC} = 16\text{ V}$

Figure 15. Noise vs. V_{icm} at $V_{CC} = 10\text{ V}$

Figure 16. Noise vs. frequency at $V_{CC} = 3\text{ V}$ and $V_{CC} = 16\text{ V}$

Figure 17. Voltage gain and phase vs. frequency at $V_{icm} = 1.5\text{ V}$ and $V_{CC} = 3\text{ V}$

Figure 18. Voltage gain and phase vs. frequency at $V_{icm} = 2.5\text{ V}$ and $V_{CC} = 3\text{ V}$


Figure 19. Voltage gain and phase vs. frequency at $V_{icm} = 0.5\text{ V}$ and $V_{CC} = 3\text{ V}$

Figure 20. Voltage gain and phase vs. frequency at $V_{icm} = 8\text{ V}$ and $V_{CC} = 16\text{ V}$

Figure 21. Voltage gain and phase vs. frequency at $V_{icm} = 15.5\text{ V}$ and $V_{CC} = 16\text{ V}$

Figure 22. Voltage gain and phase vs. frequency at $V_{icm} = 0.5\text{ V}$ and $V_{CC} = 16\text{ V}$

Figure 23. Inverting large signal pulse response at $V_{CC} = 3\text{ V}$, 25°C

Figure 24. Inverting large signal pulse response at $V_{CC} = 16\text{ V}$, 25°C


4 Radiations

4.1 Introduction

Table 5 summarizes the radiation performance of the RHF43B.

Table 5. Radiations

Type	Features	Value	Unit	
TID	High-dose rate	300	krad	
	Low-dose rate	300		
	ELDRS	300		
Heavy ions	SEL immunity (at 125 °C) up to:		110	MeV.cm ² /mg
	SET characterized	Inverting	LET _{th} = 1	MeV.cm ² /mg
			$\sigma = 2.00E-03$	cm ² /device
		Non-inverting	LET _{th} = 0	MeV.cm ² /mg
			$\sigma = 1.00E-03$	cm ² /device
		Subtracting	LET _{th} = 0	MeV.cm ² /mg
$\sigma = 2.00E-03$			cm ² /device	

4.2 Total ionizing dose (TID)

The products guaranteed in radiation within the RHA QML-V system fully comply with the MILSTD-883 test method 1019 specification.

The RHF43B is RHA QML-V qualified, and is tested and characterized in full compliance with the MIL-STD-883 specification. It using a mixed bipolar and CMOS technology and is tested both below 10 mrad/s (low dose rate) and between 50 and 300 rad/s (high dose rate).

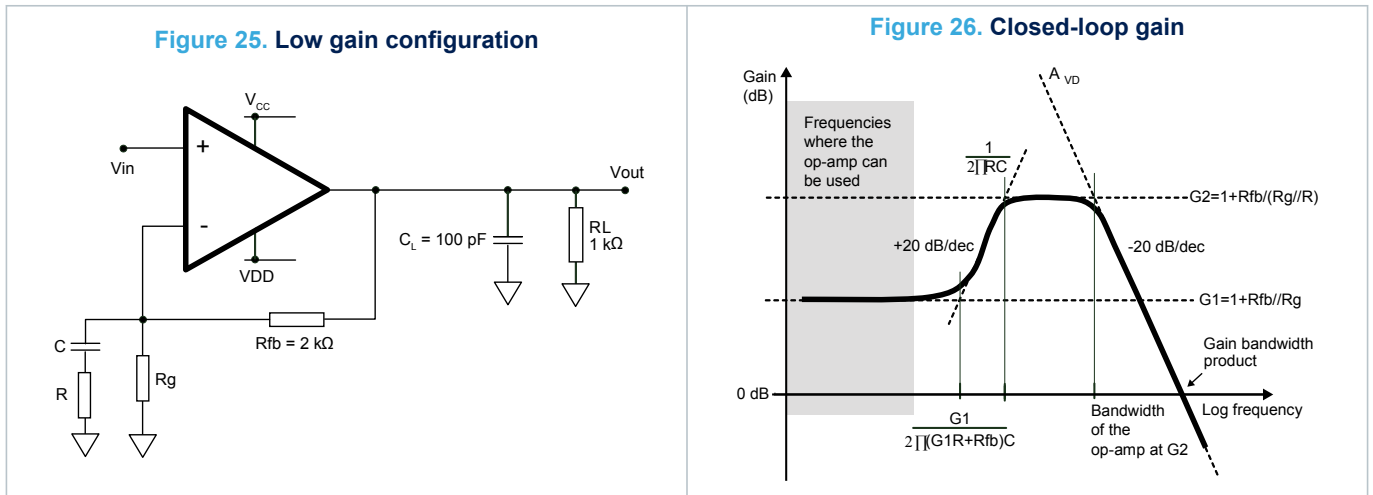
- The ELDRS characterization is performed in qualification only on both biased and unbiased parts, on a sample of ten units from two different wafer lots.
- Each wafer lot is tested at high-dose rate only, in the worst bias case condition, based on the results obtained during the initial qualification.

4.3 Heavy ions

Note: The heavy ion trials are performed on qualification lots only. No additional test is performed.

5 Achieving good stability at low gain

At low frequencies, the RHF43B can be used in a low gain configuration as shown in Figure 25. At lower frequencies, the stability is not affected by the value of the gain, which can be set close to 1 V/V (0 dB), and is reduced to its simplest expression $G1 = 1+R_{fb}/R_g$. Therefore, an R-C cell is added in the gain network so that the gain is increased (up to 5) at higher frequencies (where the stability of the amplifier could be affected). At higher frequencies, the gain becomes $G2 = 1+R_{fb}/(R_g//R)$.



R_g becomes a complex impedance. The closed-loop gain features a variation in frequency and can be expressed as Equation 1.

Equation 1

$$\text{Gain} = G1 \frac{1 + jC\omega \times \left(\frac{G1R + R_{fb}}{G1} \right)}{1 + jCR\omega}$$

Where a pole appears at $1/2\pi RC$ and a zero at $G1/2\pi(G1R+R_{fb})C$. The frequency can be plotted as shown in Figure 26.

Table 6. External components versus low-frequency gain

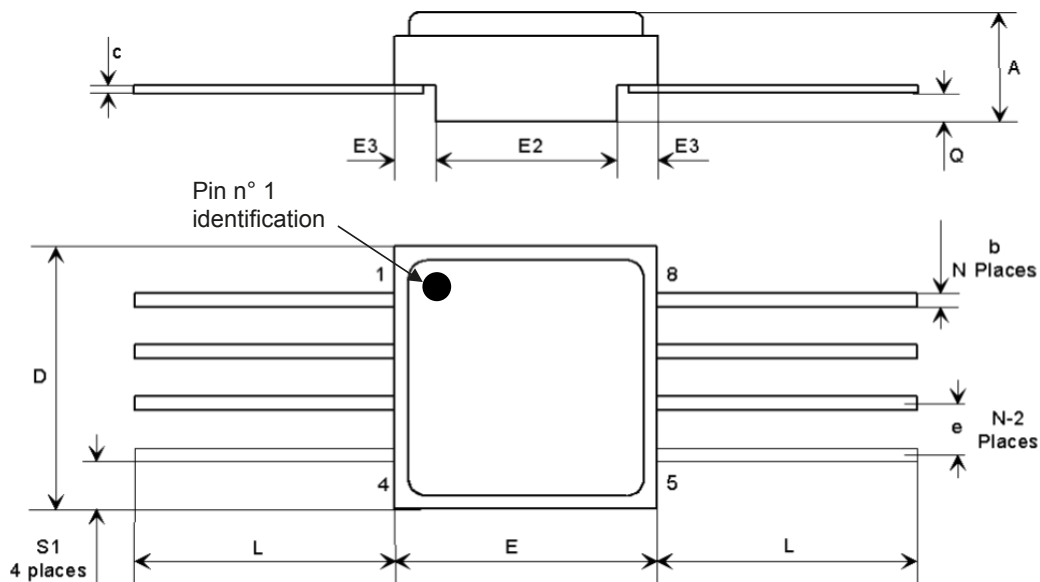
G1 (V/V)	R (Ω)	C (nF)	Rg (Ω)	Rfb (Ω)
1.1	510	1	20 k	2 k
2			2 k	
3			1 k	
4			750	
5	Not connected	Not connected	820	3.3 k

6 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 Ceramic Flat-8 package information

Figure 27. Ceramic Flat-8 package outline



Note: The upper metallic lid is not electrically connected to any pins, nor to the IC die inside the package. Connecting unused pins or metal lid to ground or to the power supply will not affect the electrical characteristics.

Table 7. Ceramic Flat-8 mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.24	2.44	2.64	0.088	0.096	0.104
b	0.38	0.43	0.48	0.015	0.017	0.019
c	0.10	0.13	0.16	0.004	0.005	0.006
D	6.35	6.48	6.61	0.250	0.255	0.260
E	6.35	6.48	6.61	0.250	0.255	0.260
E2	4.32	4.45	4.58	0.170	0.175	0.180
E3	0.88	1.01	1.14	0.035	0.040	0.045
e		1.27			0.050	
L	6.51		7.38	0.256		0.291
Q	0.66	0.79	0.92	0.026	0.031	0.036
S1	0.92	1.12	1.32	0.036	0.044	0.052
N		08			08	

7 Ordering information

Table 8. Ordering information

Order code	SMD ⁽¹⁾	Quality level	Package	Lead finish	Marking ⁽²⁾	Packing
RHF43BK1	-	Engineering model	Flat-8	Gold	RHF43BK1	Tray
RHF43BK-01V	5962F06237	QML-V flight			5962F0623701VXC	
RHF43BK-02V	5962F06237	QML-V flight		Solder Dip	5962F0623701VXA	

1. *Standard microcircuit drawing.*
2. *Specific marking only. Complete marking includes the following:*
 - ST logo
 - Date code (date the package was sealed) in YYWWA (year, week, and lot index of week)
 - Country of origin (FR = France).

Note: Contact your ST sales office for information regarding the specific conditions for products in die form and QML-Q versions.

Other information

Date code:

The date code is structured as engineering model: EM xyywwz

Where:

x = 3 (EM only), assembly location Rennes (France)

yy = last two digits of the year

ww = week digits

z = lot index of the week

Product documentation

Each product shipment includes a set of associated documentation within the shipment box. This documentation depends on the quality level of the products, as detailed in the table below.

The certificate of conformance is provided on paper whatever the quality level. For QML parts, complete documentation, including the certificate of conformance, is provided on a CDROM.

Table 9. Product documentation

Quality level	Item
Engineering model	Certificate of conformance including : Customer name Customer purchase order number ST sales order number and item ST part number Quantity delivered Date code Reference to ST datasheet Reference to TN1181 on engineering models ST Rennes assembly lot ID
QML-V Flight	Certificate of Conformance including: Customer name Customer purchase order number ST sales order number and item ST part number

Quality level	Item
QML-V Flight	Quantity delivered Date code Serial numbers Group C reference Group D reference Reference to the applicable SMD ST Rennes assembly lot ID
	Quality control inspection (groups A, B, C, D, E)
	Screening electrical data in/out summary
	Precap report
	PIND (particle impact noise detection) test
	SEM (scanning electronic microscope) inspection report
	X-ray plates

Revision history

Table 10. Document revision history

Date	Revision	Changes
21-May-2007	1	First public release
10-Dec-2007	2	Changed name of pins on pinout diagram on cover page Modified supply current values over temperature range in electrical characteristics. Power dissipation removed from AMR table.
29-Jan-2008	3	Added ELRS-free rad-hard design in description on cover page Modified description of heavy ion latch-up (SEL) immunity parameter in Table 2.
11-May-2009	4	Updated radiation immunity in Features and in Table 2. Updated smb reference in Features.
15-Oct-2009	5	Updated test conditions for Avd vs. Vicm in Table 4 and Table 5. Updated input current and voltage noise in Table 4. Updated order codes in Table 9.
30-Mar-2010	6	Added Figure 4 and Figure 5. Added information for ambient temperature in Table 4 and Table 5. Added Section 4: "Achieving good stability at low gain".
20-Aug-2010	7	Corrected "L" dimension in Table 8.
27-Jul-2011	8	Added note underneath Figure 27 and in the "Pin connections" diagram on the cover page.
08-Nov-2012	9	Features: added silhouette. Added Table 1: Device summary. Table 2: removed ± 9 from "Supply voltage"; updated footnote 1. Added Figure 6 and Figure 15. Figure 17 through to Figure 22: modified titles. Table 9: Ordering information: updated table and removed order code RHF43BK-01V.
06-Feb-2015	10	Replaced package name with "Flat-8S" instead of "Flat-8" Added marker to show the position of pin 1 on package silhouette, pinout and drawing. Updated Features, Table 1: Device summary and Section 6: Ordering information. Updated note concerning products in die form and QML-Q versions on the cover page. Table 2: Absolute maximum ratings (AMR): transferred radiation information to Table 6: Radiations. Table 8: updated dimension "L". Added Section 3: Radiations and Section 7: "Other information".
24-Mar-2015	11	Replaced Flat-8S silhouette, pinout, and package with Flat-8 silhouette, pinout, and package.
06-Apr-2016	12	Updated document layout. Table 1: "Device summary": updated footnote 1, SMD = standard microcircuit drawing.
05-Dec-2017	13	Updated the description in cover page. Deleted EPPL parameter in the Table 1: "Device summary".
16-Apr-2018	14	Updated figure on the cover page.
23-Feb-2024	15	Updated output source current test condition in Table 3, Table 4, Figure 10, Figure 11 and Figure 12.
08-Apr-2026	16	Changed packing from Strip Pack to Tray and added Solder Dip in Table 8. Ordering information.

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