STD65N6F3

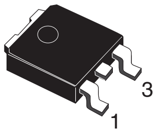
N-channel 60V - 8.0mΩ - 65A - DPAK STripFET™ Power MOSFET

PRELIMINARY DATA

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STD65N6F3	60V	< 10.5mΩ	65A	110W

- Standard threshold drive
- 100% avalanche tested



DPAK

Description

This n-channel enhancement mode Power MOSFET is the latest refinement of STMicroelectronics' unique “Single Feature Size™” strip-based process, which has decreased the critical alignment steps, offering remarkable manufacturing reproducibility. The outcome is a transistor with extremely high packing density for low on resistance, rugged avalanche characteristics and low gate charge.

Application

- Switching applications
  - Automotive

Figure 1. Internal schematic diagram

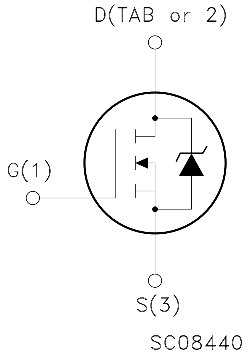


Table 1. Device summary

Order code	Marking	Package	Packaging
STD65N6F3	D65N6F3	DPAK	Tape & reel

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS}=0)	60	V
V_{GS}	Gate-Source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	65	A
I_D	Drain current (continuous) at T_C = 100°C	46	A
I_{DM} (1)	Drain current (pulsed)	260	A
P_{TOT}	Total dissipation at T_C = 25°C	110	W
	Derating factor	0.73	W/°C
dv/dt (2)	Peak diode recovery voltage slope	Tbd	V/ns
E_{AS} (3)	Single pulse avalanche energy	Tbd	mJ
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 175	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 65A$, di/dt ≤300A/µs, $V_{DD} \leq V_{(BR)DSS.}$ Tj ≤ Tjmax
3. Starting Tj = 25°C, Id = 32A, Vdd = 40V

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.36	°C/W
Rthj-pcb (1)	Thermal resistance junction-pcb max	50	°C/W
T_L	Maximum lead temperature for soldering purpose	275	°C

1. When mounted on FR-4 board of 1inch², 2oz Cu.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	I_D = 250µA, V_{GS}= 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc = 125°C			10 100	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2		4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS}= 10V, I_D= 32A		8.0	10.5	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
g_{fs} [1]	Forward transconductance	V_{DS} =25V, I_D=32A		Tbd		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1MHz, V_{GS}=0		2200 500 25		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=48V, I_D = 65A V_{GS} =10V *(see Figure 5)*		35 15 10	Tbd	nC nC nC

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 6. Switching on/off (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD}=30V, I_D= 32A, R_G=4.7Ω, V_{GS}=10V *(see Figure 4)*, *(see Figure 7)*		Tbd Tbd		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD}=30V, I_D= 32A, R_G=4.7Ω, V_{GS}=10V *(see Figure 4)*, *(see Figure 7)*		Tbd Tbd		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)(1)				65 260	A A
V_{SD}	Forward on voltage	I_{SD}=65A, V_{GS}=0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}=65A, di/dt =100A/µs, V_{DD}=30V, Tj=150°C *(see Figure 6)*		50 90 4.0		ns nC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

3 Test circuit

Figure 2. Unclamped inductive load test circuit

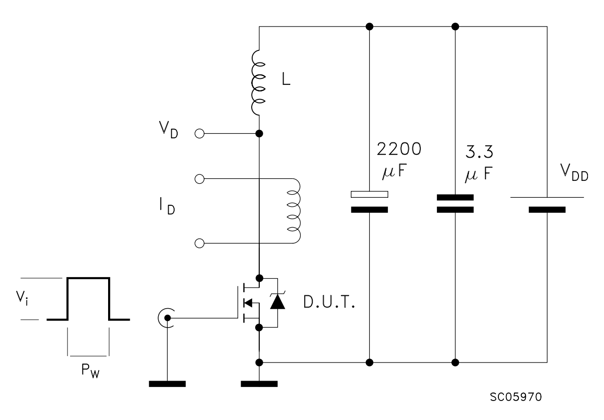


Figure 3. Unclamped inductive waveform

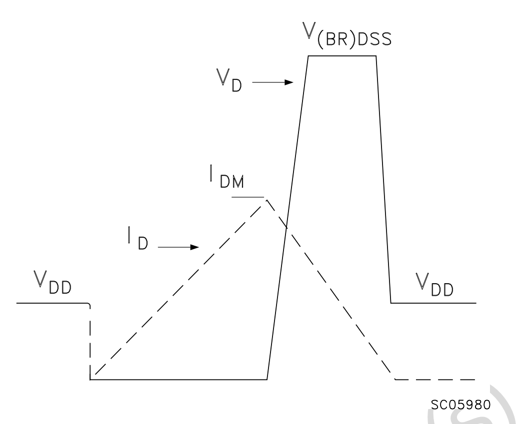


Figure 4. Switching times test circuit for resistive load

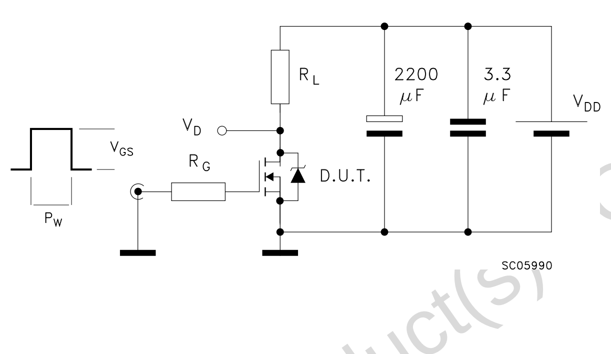


Figure 5. Gate charge test circuit

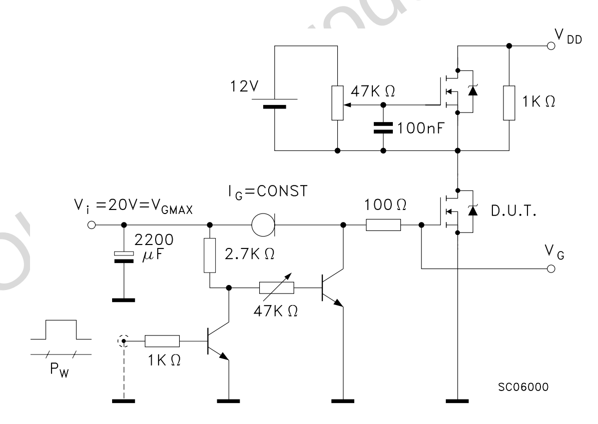


Figure 6. Test circuit for inductive load switching and diode recovery times

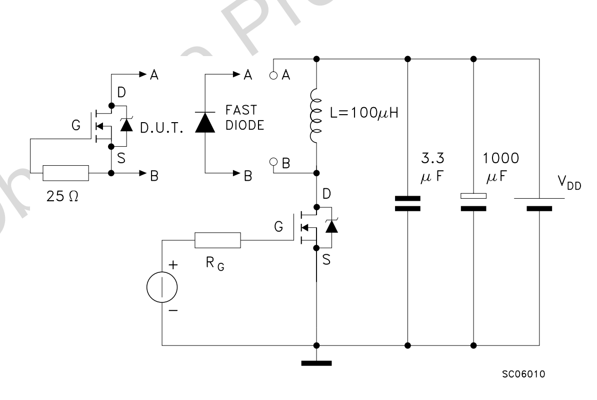
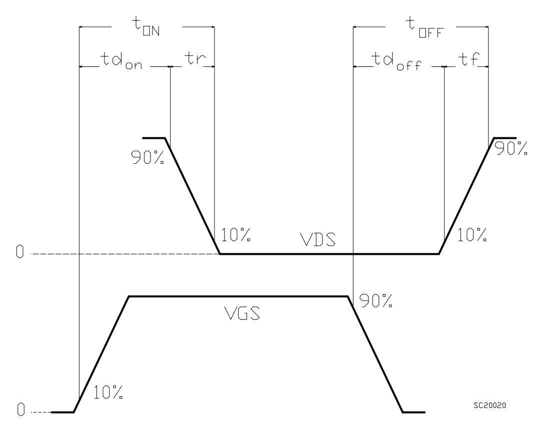


Figure 7. Switching time waveform

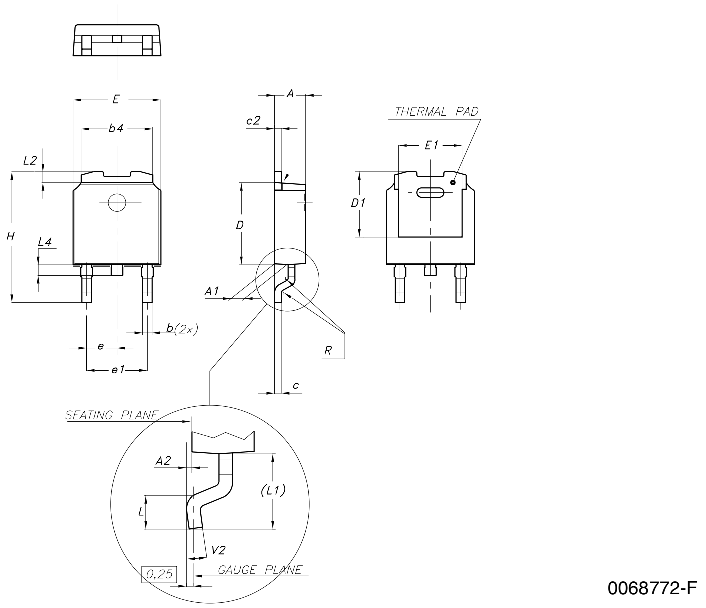


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

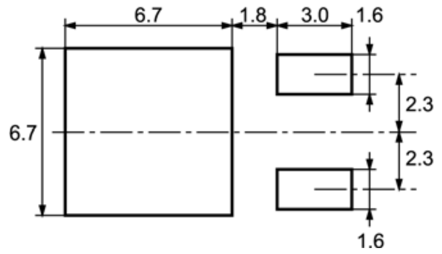
DPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
b4	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
D1		5.1			0.200	
E	6.4		6.6	0.252		0.260
E1		4.7			0.185	
e		2.28			0.090	
e1	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L	1			0.039		
(L1)		2.8			0.110	
L2		0.8			0.031	
L4	0.6		1	0.023		0.039
R		0.2			0.008	
V2	0°		8°	0°		8°



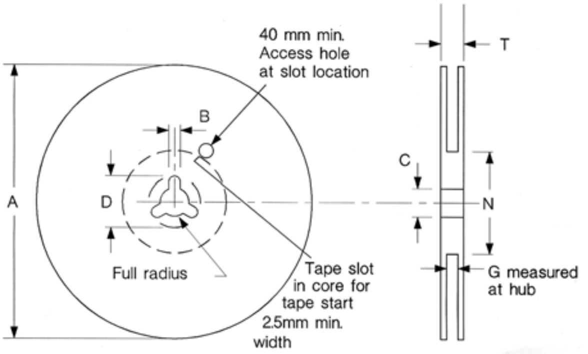
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



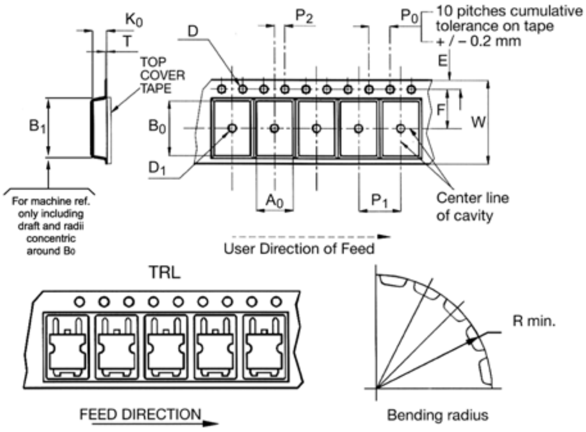
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 8. Revision history

Date	Revision	Changes
10-Jul-2007	1	First release

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