



# STW54NM65N

N-channel 650 V, 0.054  $\Omega$ , 50 A MDmesh™ II Power MOSFET  
TO-247

## Features

Type	V <sub>DSS</sub> (@T <sub>jmax</sub> )	R <sub>DS(on)</sub> max	I <sub>D</sub>
STW54NM65N	710 V	< 0.065 $\Omega$	50 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Application

- Switching applications

## Description

This series of devices is designed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the STMicroelectronics' strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

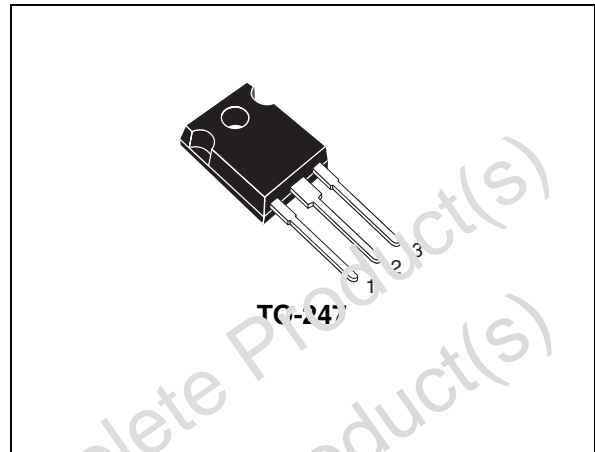


Figure 1. Internal schematic diagram

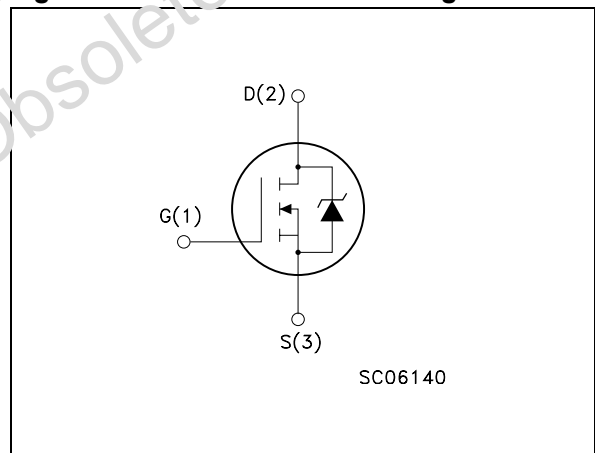


Table 1. Device summary

Order code	Marking	Package	Packaging
STW54NM65N	54NM65N	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	650	V
$V_{GS}$	Gate- source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	50	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	31.5	A
$I_{DM}^{(1)}$	Drain current (pulsed)	200	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	350	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 50$  A,  $di/dt \leq 400$  A/ $\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.36	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C/W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	14	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25^\circ\text{C}$ , $I_D = I_{AS}$ , $V_{DD} = 50$ V)	1600	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	650			V
$dv/dt^{(1)}$	Drain source voltage slope	$V_{DD} = 520\text{ V}$ , $I_D = 50\text{ A}$ , $V_{GS} = 10\text{ V}$		35		V/ns
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , @125 °C			100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 25\text{ A}$		0.054	0.065	$\Omega$

1. Characteristic value at turn off on inductive load

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 25\text{ A}$		45		S
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		6000		pF
$C_{oss}$	Output capacitance			320		pF
$C_{rfs}$	Reverse transfer capacitance			35		pF
$C_{oss\text{ eq.}}^{(2)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0$ to $520\text{ V}$		690		pF
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}$ , $I_D = 50\text{ A}$ , $V_{GS} = 10\text{ V}$ , <i>(see Figure 15)</i>		200		nC
$Q_{gs}$	Gate-source charge			20		nC
$Q_{gd}$	Gate-drain charge			110		nC
$R_g$	Gate input resistance	f=1 MHz gate DC bias=0 Test signal level = 20 mV open drain		1.9		$\Omega$

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$ , $I_D = 25 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see Figure 14)		30		ns
$t_r$	Rise time			50		ns
$t_{d(off)}$	Turn-off delay time			240		ns
$t_f$	Fall time			100		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				50	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				200	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 50 \text{ A}$ , $V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 50 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$		630		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$		18		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)		55		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 50 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$		750		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$		22		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16)		58		A

1. Pulse width limited by safe operating area

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

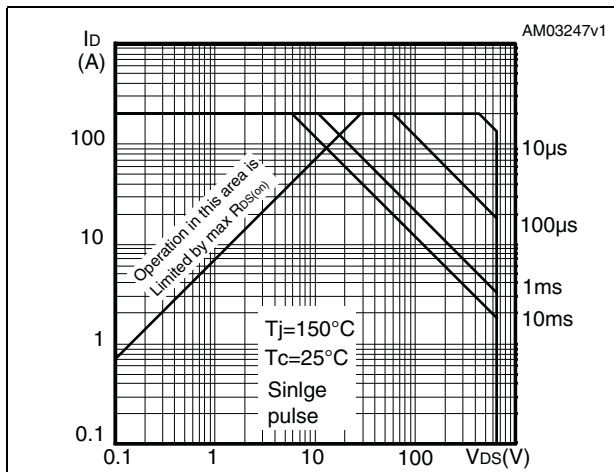


Figure 3. Thermal impedance

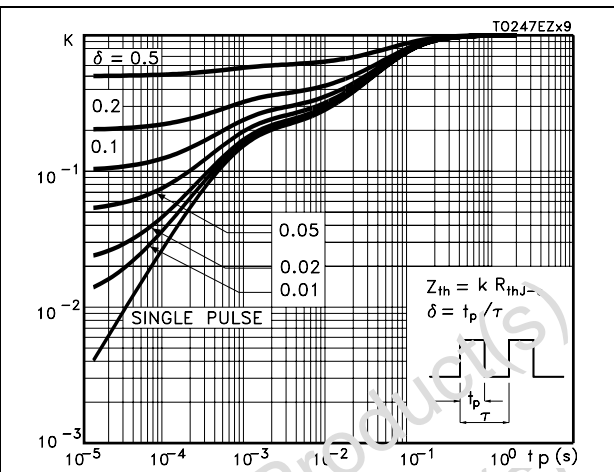


Figure 4. Output characteristics

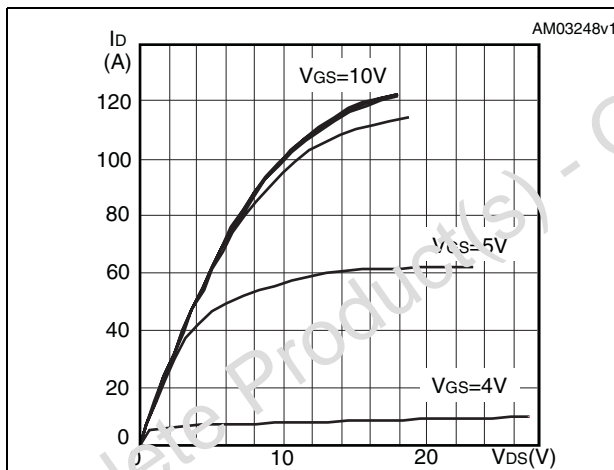


Figure 5. Transfer characteristics

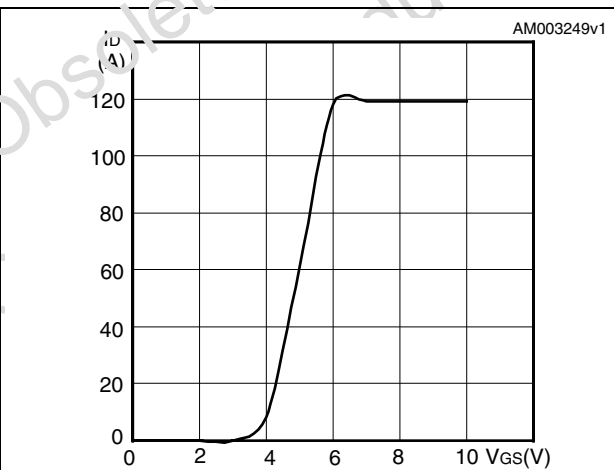


Figure 6. Transconductance

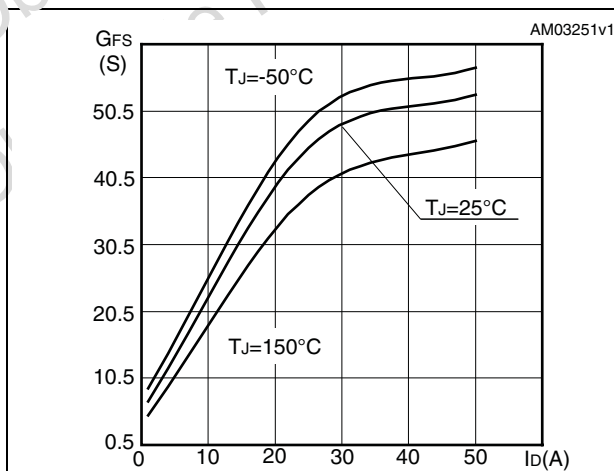


Figure 7. Static drain-source on resistance

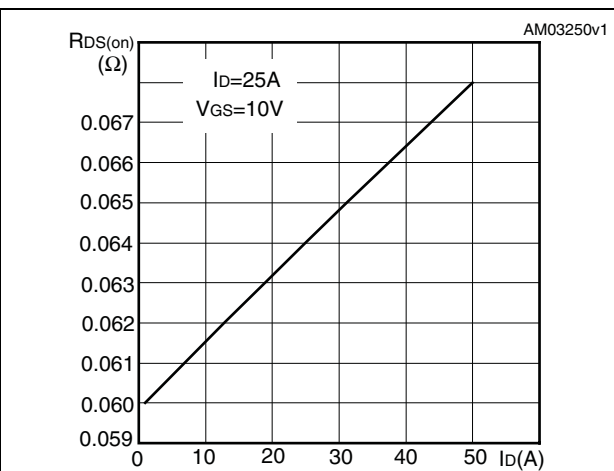


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

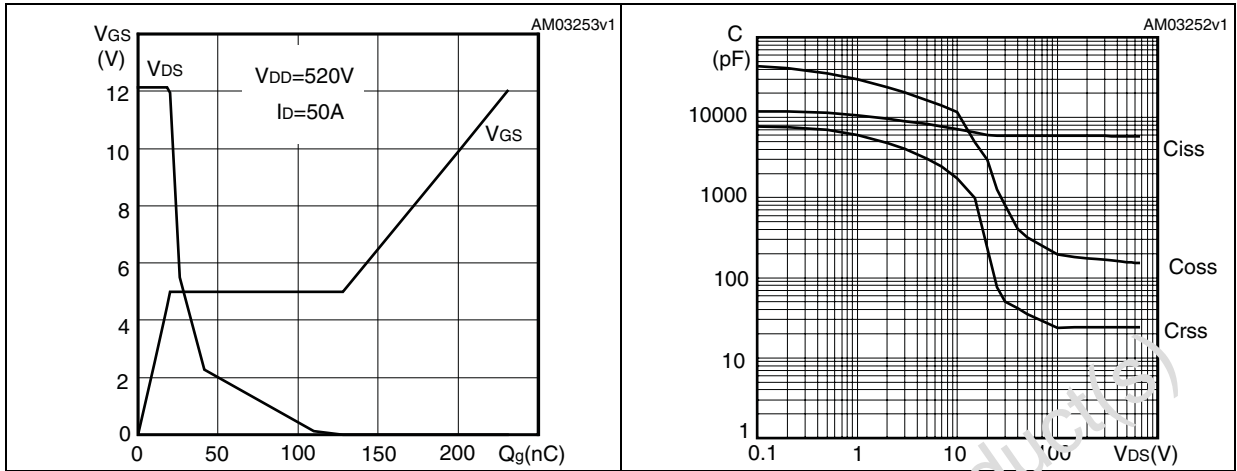


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

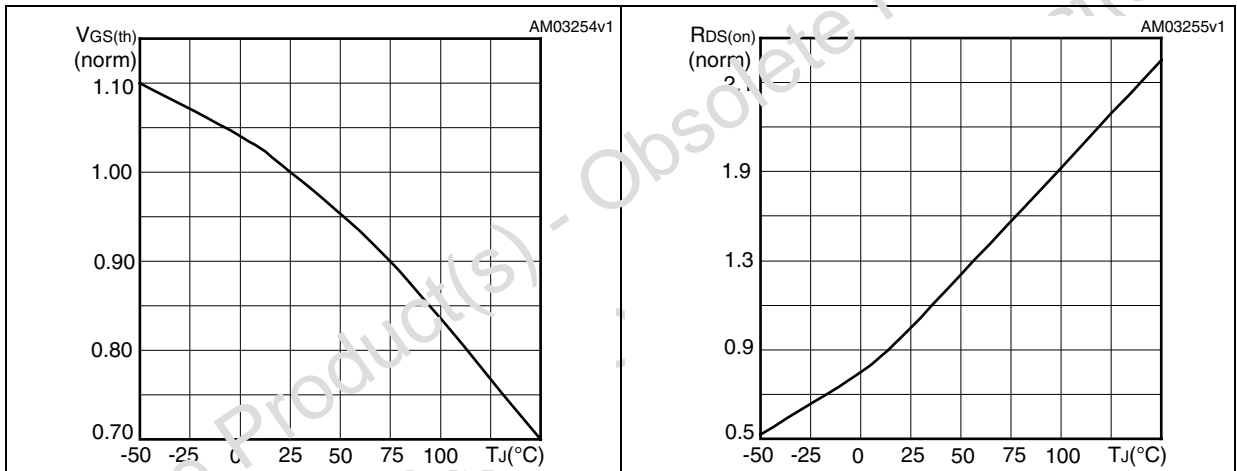
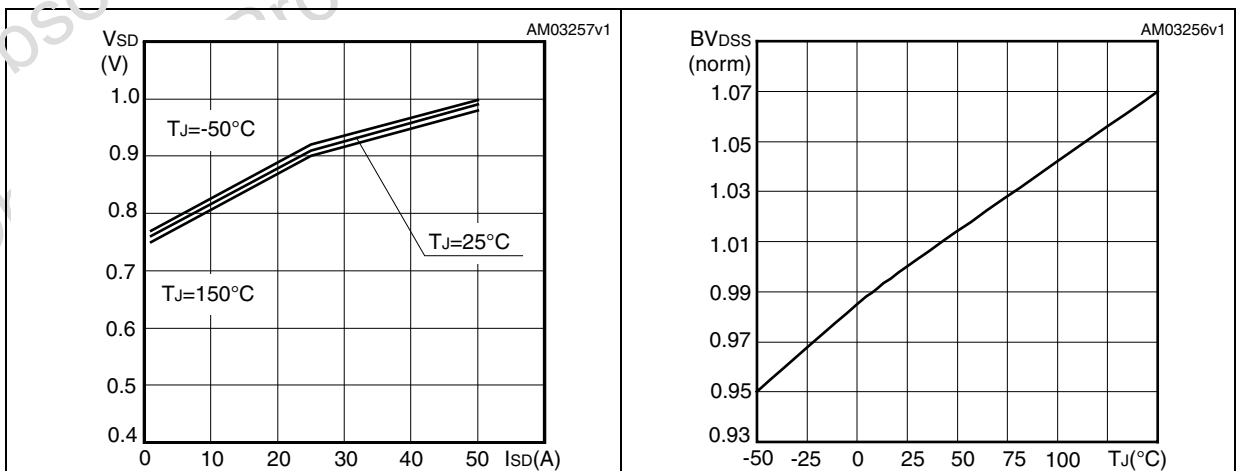


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized  $B_{V_{DS}}$  vs temperature



### 3 Test circuit

Figure 14. Switching times test circuit for resistive load

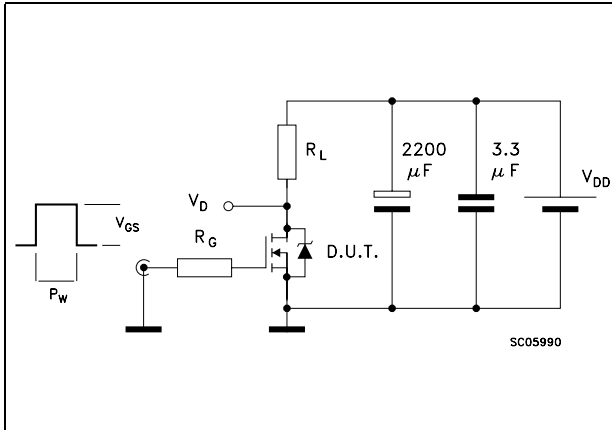


Figure 15. Gate charge test circuit

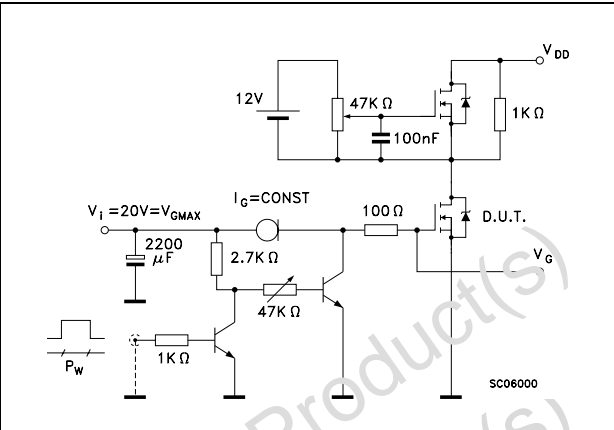


Figure 16. Test circuit for inductive load switching and diode recovery times

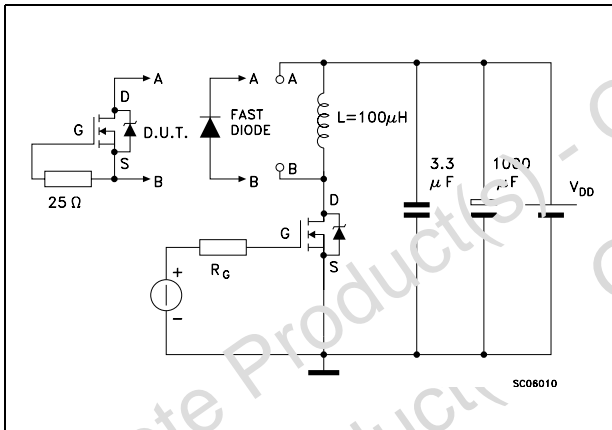


Figure 17. Unclamped inductive load test circuit

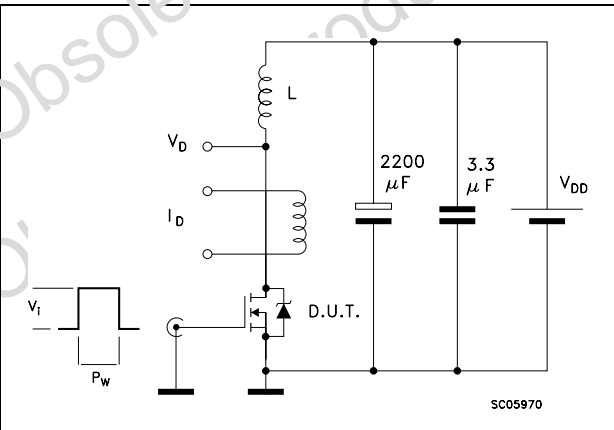


Figure 18. Unclamped inductive waveform

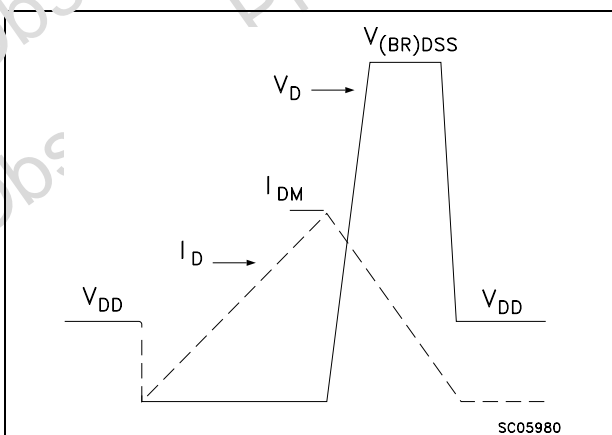
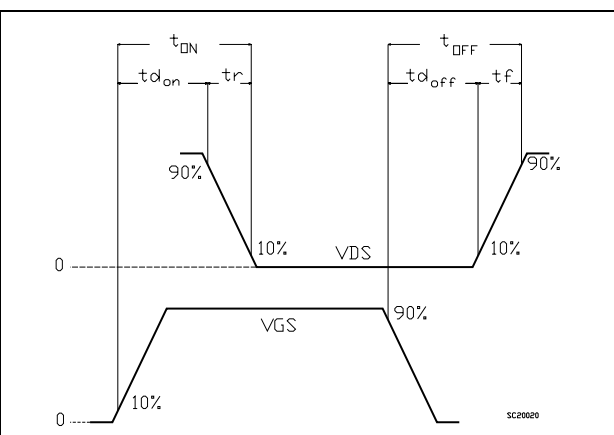


Figure 19. Switching time waveform



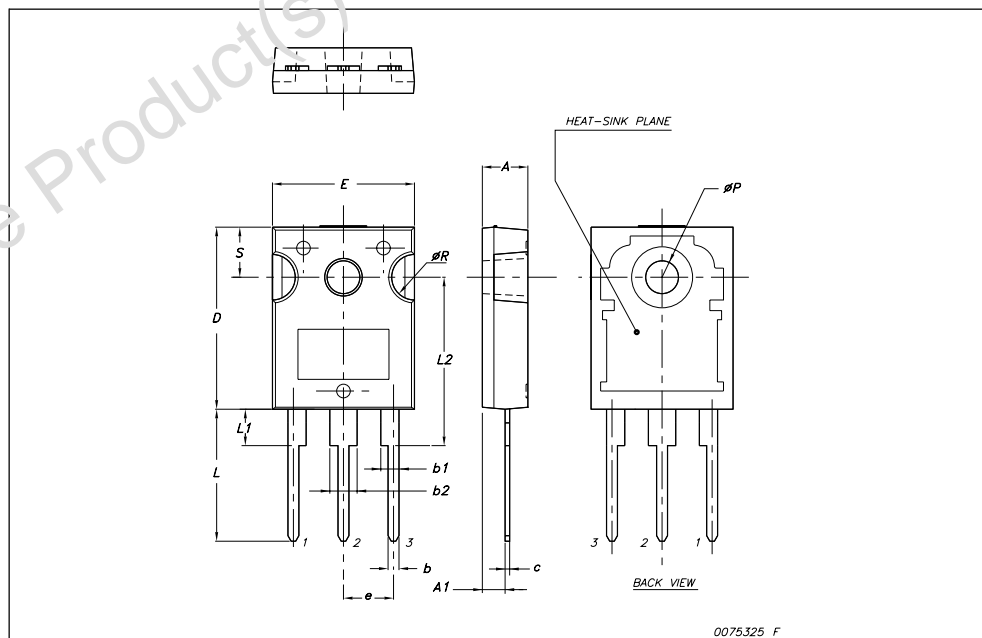
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

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**TO-247 Mechanical data**

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		19.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
24-Jul-2008	1	Initial release
20-Jan-2009	2	Document status promoted from preliminary data to datasheet.

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