

# STH85N15F4-2 STP85N15F4

# N-channel 150 V, 0.015 Ω, 85 A TO-220, H<sup>2</sup>PAK STripFET™ DeepGATE™ Power MOSFET

Preliminary data

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STH85N15F4-2	150 V	< 18.6 mΩ	85 A
STP85N15F4	150 V	< 19 mΩ	85 A

- Extremely low on-resistance R<sub>DS(on)</sub>
- 100% avalanche tested

## **Application**

■ Switching applications

### **Description**

This STripFET<sup>TM</sup> DeepGATE<sup>TM</sup> Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance, with a new gate structure, providing superior switching performance.

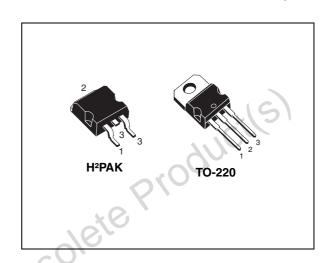


Figure 1. Internal schematic diagram

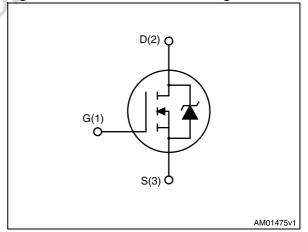


Table 1. Device summary

ipsolete Pro

Order codes	Order codes Marking		Packaging
STH85N15F4-2	85N15F4	H <sup>2</sup> PAK	Tape and reel
STP85N15F4	STP85N15F4 85N15F4		Tube

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#### **Electrical ratings** 1

Table 2. **Absolute maximum ratings** 

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	150	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	85	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	60	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	340	Α
P <sub>TOT</sub>	Total dissipation at T <sub>C</sub> = 25 °C	300	W
	Derating factor	2.0	W/°C
E <sub>AS</sub> (2)	Single pulse avalanche energy	TBD	mJ
T <sub>stg</sub>	Storage temperature	– 55 to 175	°C
T <sub>j</sub>	Max. operating junction temperature	× C = 55 to 175	
1. Pulse wi	dth limited by safe operating area	3	
2. Starting	T <sub>j</sub> = 25 °C, I <sub>D</sub> = 50 A, V <sub>DD</sub> =25 V		
	0/03		

<sup>1.</sup> Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Val	Unit	
Syllibol	Parameter	TO-220	H <sup>2</sup> PAK	Oill
R <sub>thj-case</sub>	Thermal resistance junction-case max	0.5		°C/W
R <sub>thj-pcb</sub>	Thermal resistance junction-pcb max	35 <sup>(1)</sup>		°C/W
R <sub>thj-a</sub>	Thermal resistance junction-ambient max	62.5		°C/W
Tı	Maximum lead temperature for soldering purpose	300		°C

<sup>1.</sup> When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

<sup>2.</sup> Starting  $T_i$ = 25 °C,  $I_D$ = 50 A,  $V_{DD}$ =25 V

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25 °C unless otherwise specified)

Table 4. On/off states

Parameter	Test conditions		Min.	Тур.	Max.	Unit
Drain-source Breakdown voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$		150			٧
Zero gate voltage Drain current (V <sub>GS</sub> = 0)	$V_{DS}$ = max rating $V_{DS}$ = max rating, $T_{C}$ = 125 °C				1 100	μA μA
Gate-body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			1,10	100	nA
Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		2	Ç	4	٧
Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40 A	TO220		15.5 15.0	19 18.6	mΩ
	Drain-source Breakdown voltage  Zero gate voltage Drain current (V <sub>GS</sub> = 0)  Gate-body leakage current (V <sub>DS</sub> = 0)  Gate threshold voltage  Static drain-source on	Drain-source Breakdown voltage	$\begin{array}{ll} \text{Drain-source} \\ \text{Breakdown voltage} \\ \text{Zero gate voltage} \\ \text{Drain current } (V_{GS} = 0) \\ \text{Gate-body leakage} \\ \text{current } (V_{DS} = 0) \\ \text{Gate threshold voltage} \\ \text{Static drain-source on} \\ \end{array} \begin{array}{ll} V_{DS} = \max \text{ rating} \\ V_{DS} = \max \text{ rating}, \\ T_{C} = 125 \text{ °C} \\ \\ V_{GS} = \pm 20 \text{ V} \\ \\ \text{V}_{DS} = V_{GS},  I_{D} = 250  \mu\text{A} \\ \\ \text{TO220} \\ \end{array}$	Drain-source Breakdown voltage $I_D = 250 \; \mu\text{A}, \; V_{GS} = 0 \qquad 150$ $Zero \; \text{gate voltage} \qquad V_{DS} = \text{max rating} \qquad V_{DS} = \text{max rating}, \qquad V_{C} = 125 \; ^{\circ}\text{C}$ $Gate-body \; leakage \qquad V_{GS} = \pm 20 \; V \qquad V_{GS} = \pm 20 \; V$ $Gate \; threshold \; voltage \qquad V_{DS} = V_{GS}, \; I_D = 250 \; \mu\text{A} \qquad 2$ $Static \; drain-source \; on \qquad V_{GS} = 10 \; V, \qquad TO220$	Drain-source $I_D = 250  \mu A$ , $V_{GS} = 0$ 150         Zero gate voltage $V_{DS} = \max_{x = 100} x$ rating         Drain current ( $V_{GS} = 0$ ) $V_{DS} = \max_{x = 100} x$ rating, $V_{CS} = 125  ^{\circ}C$ Gate-body leakage current ( $V_{DS} = 0$ ) $V_{GS} = \pm 20  V$ Gate threshold voltage $V_{DS} = V_{GS}$ , $V_{DS} = 0$ Static drain-source on $V_{GS} = 10  V$ ,         TO220       15.5	Drain-source Breakdown voltage

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	8320	-	pF
C <sub>oss</sub>	Output capacitance	$V_{DS} = 25 \text{ V}, f = 1 \text{ MHz},$	-	600	-	pF
C <sub>rss</sub>	Reverse transfer capacitance	V <sub>GS</sub> = 0	-	230	-	pF
$Q_g$	Total gate charge	$V_{DD} = 80 \text{ V}, I_D = 85 \text{ A},$	-	140	-	nC
$Q_{gs}$	Gate-source charge	V <sub>GS</sub> = 10 V	-	TBD	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 3)	-	TBD	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub>	Turn-on delay time Rise time	$V_{DD}$ = 75 V, $I_D$ = 40 A $R_G$ = 4.7 $\Omega$ V <sub>GS</sub> = 10 V (see Figure 2)	-	TBD TBD	-	ns ns
t <sub>d(off)</sub>	Turn-off-delay time Fall time	$V_{DD}$ = 75 V, $I_D$ = 40 A, $R_G$ = 4.7 $\Omega$ , $V_{GS}$ = 10 V (see Figure 2)	-	TBD TBD	-	ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Tvn	Max	Unit
-		rest conditions		Тур.		
I <sub>SD</sub>	Source-drain current		-		85	A
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		340	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	$I_{SD} = 85 \text{ A}, V_{GS} = 0$	-		TBD	V
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 85 \text{ A}, V_{DD} = 25 \text{ V}$ di/dt = 100 A/µs,		TBD		ns
$Q_{rr}$	Reverse recovery charge	· ·	-	TBD		nC
$I_{RRM}$	Reverse recovery current	(see Figure 4)		TBD		Α
2. Pulsed: F	Reverse recovery current  Oth limited by safe operating area.  Pulse duration = 300 µs, duty cycle 1.5	9%	.0	40		<i>)</i> ۱
		*EP	40			
		coleir				
	C	05				
	*(5)					
	AUCL					
	(OO,					
10						

## 3 Test circuits

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

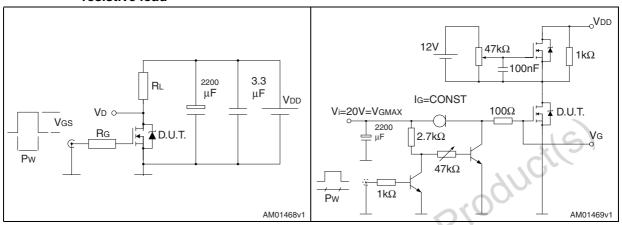


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

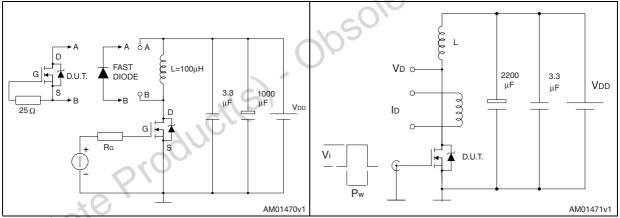
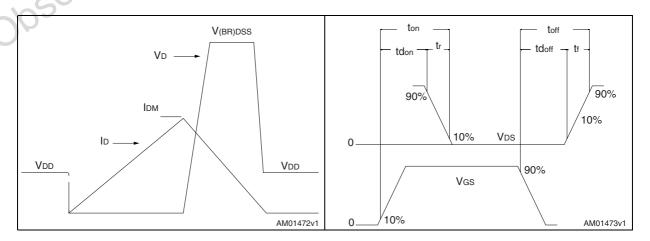


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



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# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220 mechanical data

D:	mm		
Dim.	Min.	Тур.	Max.
А	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
С	0.48		0.70
D	15.25		15.75
D1		1,27	
Е	10	0/6	10.40
е	2.40	105	2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
	3.75		3.85
Q	2.65		2.95

Figure 8. TO-220 drawing

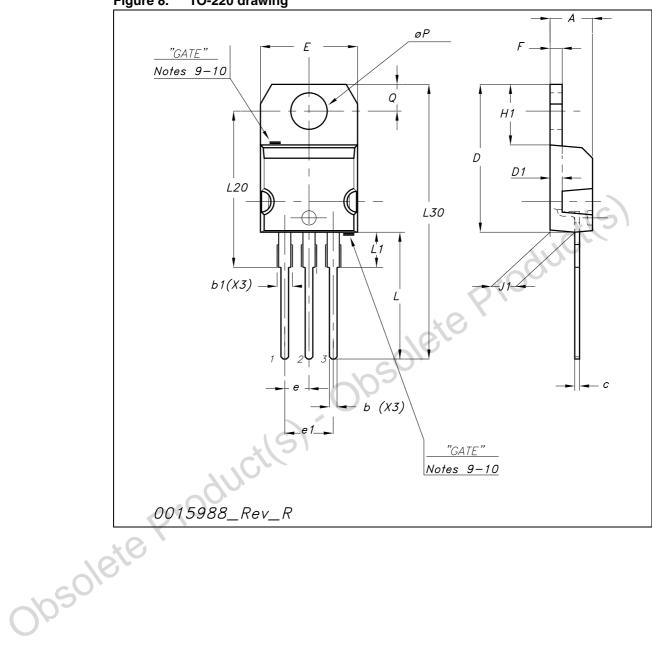
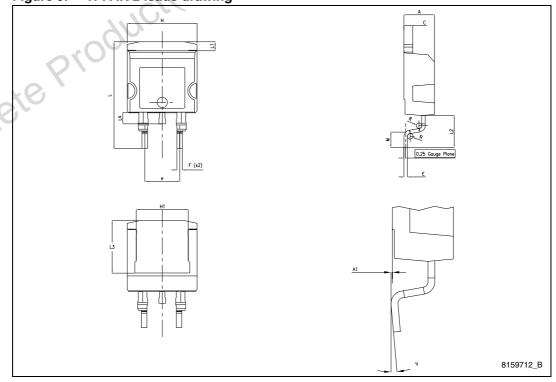


Table 9. H<sup>2</sup>PAK 2 leads mechanical data

Dim.		mm		
Dim.	Min.	Тур.	Max.	
А	4.30	-	4.80	
A1	0.03	-	0.20	
С	1.17	-	1.37	
е	4.98	-	5.18	
E	0.50	-	0.90	
F	0.78	-	0.85	
Н	10.00	-	10.40	
H1	7.171	-	7.971	
L	15.30	-	15.80	
L1	1.27	- 01	1.40	
L2	4.93	- 7	5.23	
L3	7.45	10/0	7.85	
L4	1.5	0/0	1.7	
М	2.6	W2 -	2.9	
R	0.20	-	0.60	
V	0°	-	8°	

Figure 9. H<sup>2</sup>PAK 2 leads drawing



Obsolete Product(s)

2.54 2.54 1.00

Figure 10. H<sup>2</sup>PAK 2 recommended footprint

10/12 Doc ID 15290 Rev 3

# 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
12-Jan-2009	1	First release
03-Jul-2009	2	Substituted D²PAK with H²PAK
07-Jul-2009	3	Status promoted from target specification to preliminary data

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