



STK24N4LLF5

N-channel 40 V, 0.0046 Ω , 24 A, PolarPAK[®]
STripFET[™]V Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	R _{DS(on)} *Q _g
STK24N4LLF5	40 V	< 0.0055 Ω	96 nC*m Ω

- Ultra low top and bottom junction to case thermal resistance
- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- Fully encapsulated die
- 100% matte tin finish (in compliance with the 2002/95/EC european directive)
- High avalanche ruggedness
- PolarPAK[®] is a trademark of VISHAY

Application

- Switching applications

Description

This product utilizes the 5th generation of design rules of ST's proprietary STripFET[™] technology. The lowest available R_{DS(on)} * Q_g in this chip scale package, makes this device suitable for the most demanding DC-DC converter applications, where high power density is to be achieved.

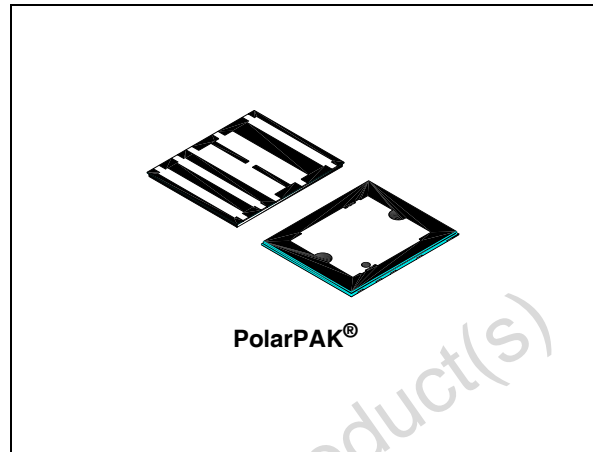


Figure 1. Internal schematic diagram

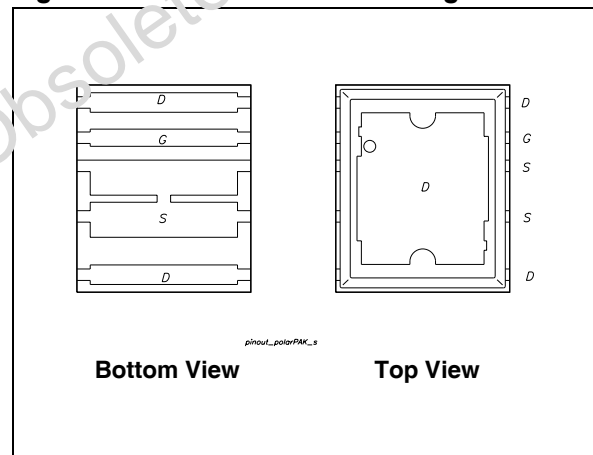


Table 1. Device summary

Order code	Marking	Package	Packaging
STK24N4LLF5	244L5	PolarPAK [®]	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	40	V
V_{GS}	Gate-source voltage	± 22	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	15.3	A
$I_{DM}^{(2)}$	Drain current (pulsed)	96	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	5.2	W
	Derating factor	0.0416	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	TBD	J
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted on FR-4 board of 1inch², 2 oz Cu and $\leq 10\text{sec}$
2. Pulse width limited by package
3. Starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = 12\text{ A}$, $V_{DD} = 25\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Typ.	Max.	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	20	24	$^\circ\text{C}/\text{W}$
$R_{thj-c}^{(2)}$	Thermal resistance junction-case (top drain)	1	1.2	$^\circ\text{C}/\text{W}$
$R_{thj-c}^{(3)}$	Thermal resistance junction-case (source)	2.8	3.4	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2 oz Cu and $\leq 10\text{sec}$
2. Steady state
3. Measured at source pin when the device is mounted on FR-4 board in steady state

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0$	40			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating}$, $T_c = 125\text{ °C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 22\ \text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\ \text{V}$, $I_D = 12\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 12\ \text{A}$		0.0046 0.0058	0.0055 0.0065	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$		2350		pF
C_{oss}	Output capacitance			335		pF
C_{rss}	Reverse transfer capacitance			50		pF
Q_g	Total gate charge	$V_{DD} = 15\ \text{V}$, $I_D = 24\ \text{A}$ $V_{GS} = 4.5\ \text{V}$ (see Figure 3)		20		nC
Q_{gs}	Gate-source charge			TBD		nC
Q_{gd}	Gate-drain charge			TBD		nC
R_G	Gate input resistance	$f = 1\ \text{MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain		TBD		Ω

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	$V_{DD}=15\text{ V}$, $I_D=12\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 2)		TBD TBD		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	$V_{DD}=15\text{ V}$, $I_D=12\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ (see Figure 2)		TBD TBD		ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)				24 96	A A
$V_{SD}^{(2)}$	Forward on Voltage	$I_{SD}=24\text{ A}$, $V_{GS}=0$			1.1	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=24\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=20\text{ V}$, $T_j=150\text{ }^\circ\text{C}$ (see Figure 7)		TBD TBD TBD		ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

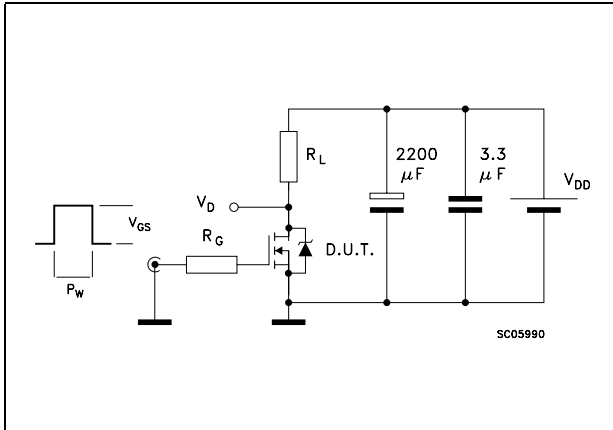


Figure 3. Gate charge test circuit

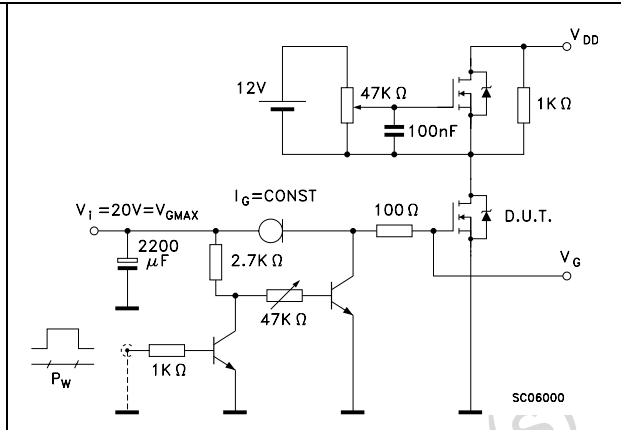


Figure 4. Test circuit for inductive load switching and diode recovery times

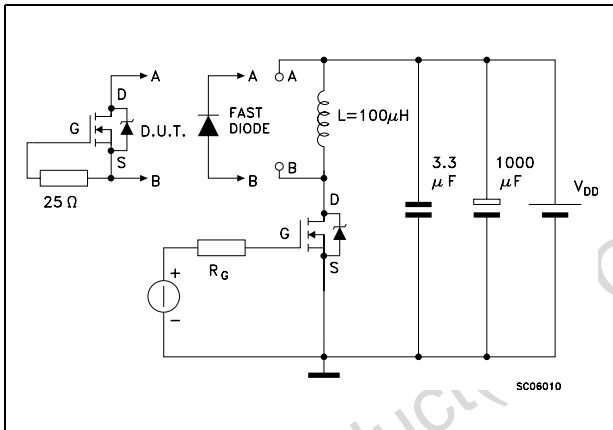


Figure 5. Unclamped inductive load test circuit

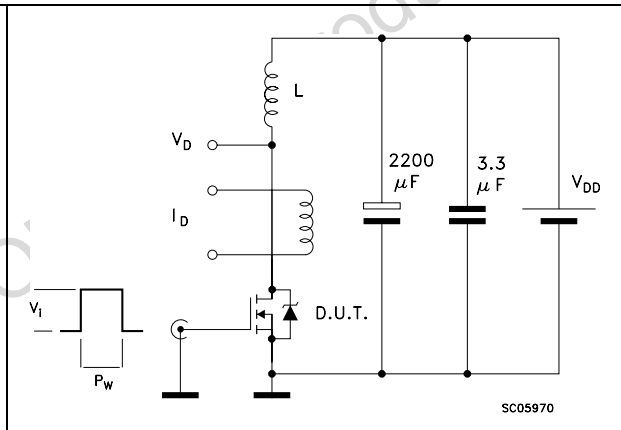


Figure 6. Unclamped inductive waveform

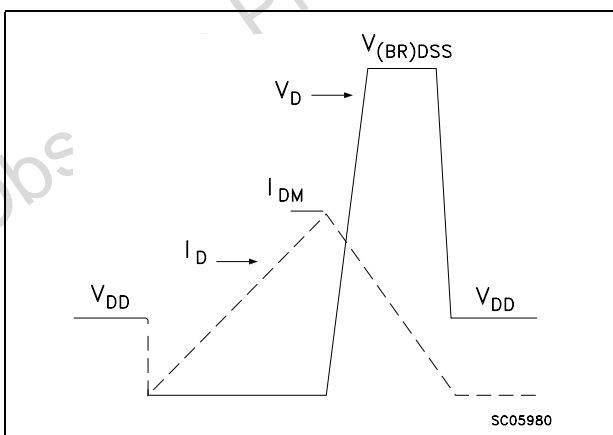


Figure 7. Switching time waveform

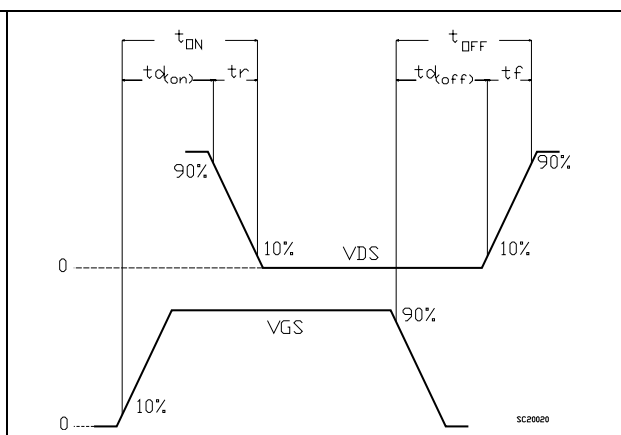
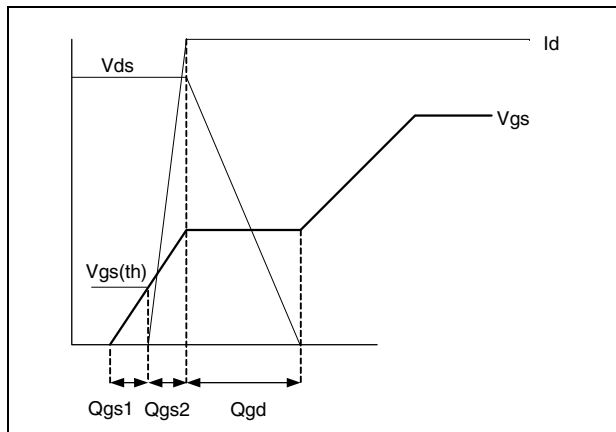


Figure 8. Gate charge waveform



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4 Package mechanical data

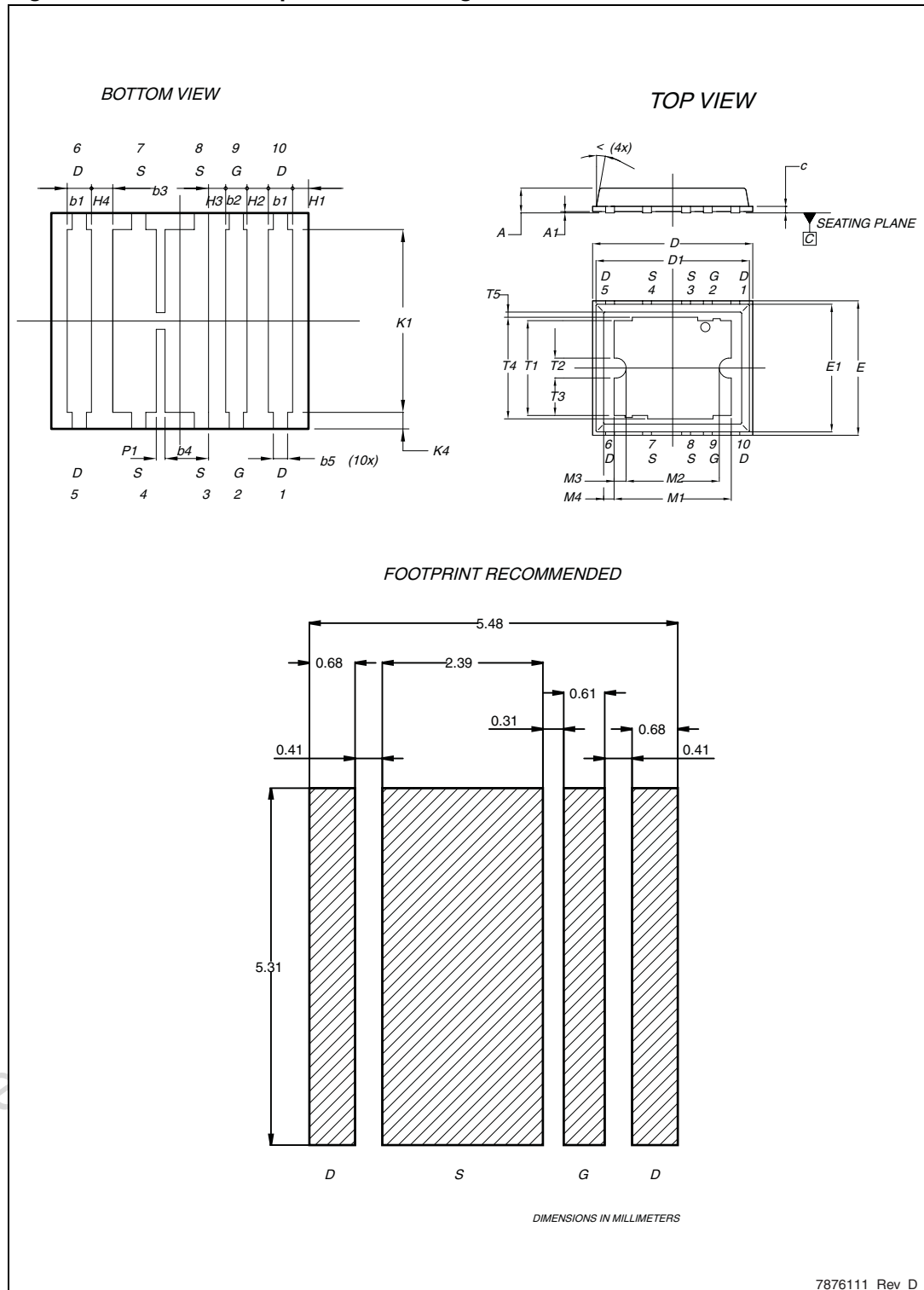
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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Table 8. PolarPAK® option "S" mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.75	0.80	0.85
A1			0.05
b1	0.48	0.58	0.68
b2	0.41	0.51	0.61
b3	2.19	2.29	2.39
b4	0.89	1.04	1.19
b5	0.23	0.33	0.43
c	0.20	0.25	0.30
D	6	6.15	6.30
D1	5.74	5.89	6.04
E	5.01	5.16	5.31
E1	4.75	4.90	5.05
H1	0.23	0.38	
H2	0.45	0.51	0.56
H3	0.31	0.41	0.51
H4	0.45	0.51	0.56
K1	4.22	4.37	4.52
K2	1.08	1.13	1.18
K3	1.37		
K4	0.24		
M1	4.30	4.50	4.70
M2	3.43	3.58	3.73
M3	0.22		
M4	0.05		
P1	0.15	0.20	0.25
T1	3.48	3.64	4.10
T2	0.56	0.76	0.95
T3	1.20		
T4	3.90		
T5		0.18	0.36
<	0°	10°	12°

Figure 9. PolarPAK® option “S” drawing



7876111_Rev_D

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
19-Jan-2009	1	First release

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