



# STL17NF25

N-channel 250 V, 0.14  $\Omega$ , 17 A, PowerFLAT™ (6x5)  
low gate charge STripFET™ II Power MOSFET

Preliminary data

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL17NF25	250 V	< 0.165 $\Omega$	17 A

- Improved die-to-footprint ratio
- Very low profile package (1 mm max)
- Exceptional dv/dt capability
- Low gate charge

## Application

- Switching applications

## Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

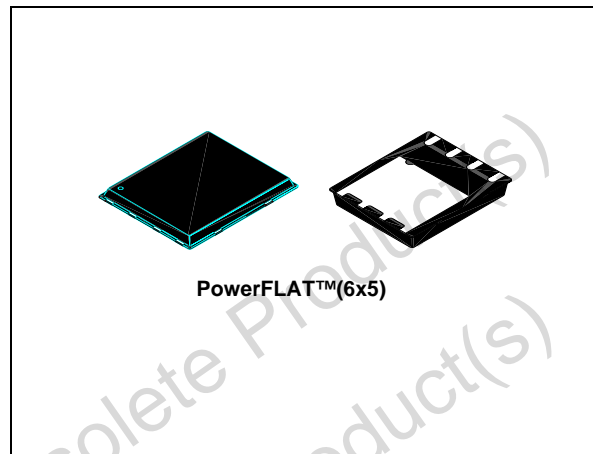


Figure 1. Internal schematic diagram

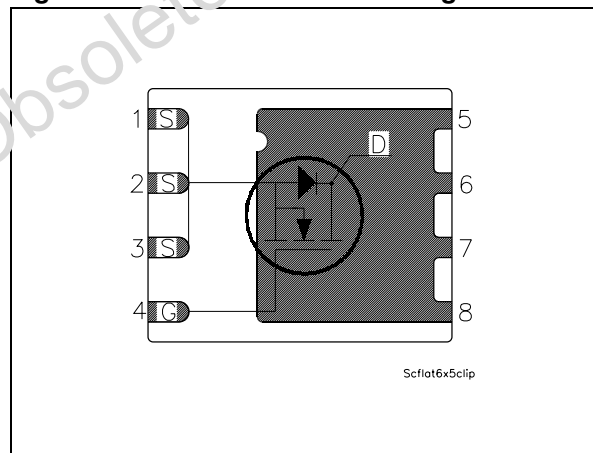


Table 1. Device summary

Order code	Marking	Package	Packaging
STL17NF25	17NF25	PowerFLAT™ (6x5)	Tape and reel

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	250	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	17	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	10	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	3.5	A
$I_{DM}^{(3)}$	Drain current (pulsed)	68	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	4	W
$dv/dt^{(4)}$	Peak diode recovery voltage slope	10	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_J$	Max. operating junction temperature	150	$^\circ\text{C}$

1. This value is rated according  $R_{thj-c}$
2. This value is according to  $R_{thj-pcb}$
3. Pulse width limited by safe operating area
4.  $I_{SD} \leq 17\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient max	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu,  $t < 10\text{ sec}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	250			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ , $T_c = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8.5\text{ A}$		0.14	0.165	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$ , $I_D = 8.5\text{ A}$	-	14	-	S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1000 178 28	-	pF pF pF
$C_{oss\text{ eq}}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }200\text{ V}$	-	135	-	pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 200\text{ V}$ , $I_D = 17\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3)	-	29.5 4.8 15.6	-	nC nC nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ gate DC bias = 0 test signal level = 20 mV open drain	-	2	-	$\Omega$

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=125\text{ V}$ , $I_D=8.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 2)</i>	-	8.8 17.2	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=125\text{ V}$ , $I_D=8.5\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ <i>(see Figure 2)</i>	-	21 8.8	-	ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		17 68	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=17\text{ A}$ , $V_{GS}=0$	-		1.6	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 50\text{ V}$ <i>(see Figure 4)</i>	-	157 0.91 11.6		ns $\mu\text{C}$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 50\text{ V}$ , $T_j=150\text{ }^\circ\text{C}$ <i>(see Figure 4)</i>	-	196 1.34 13.7		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu\text{s}$ , duty cycle 1.5%



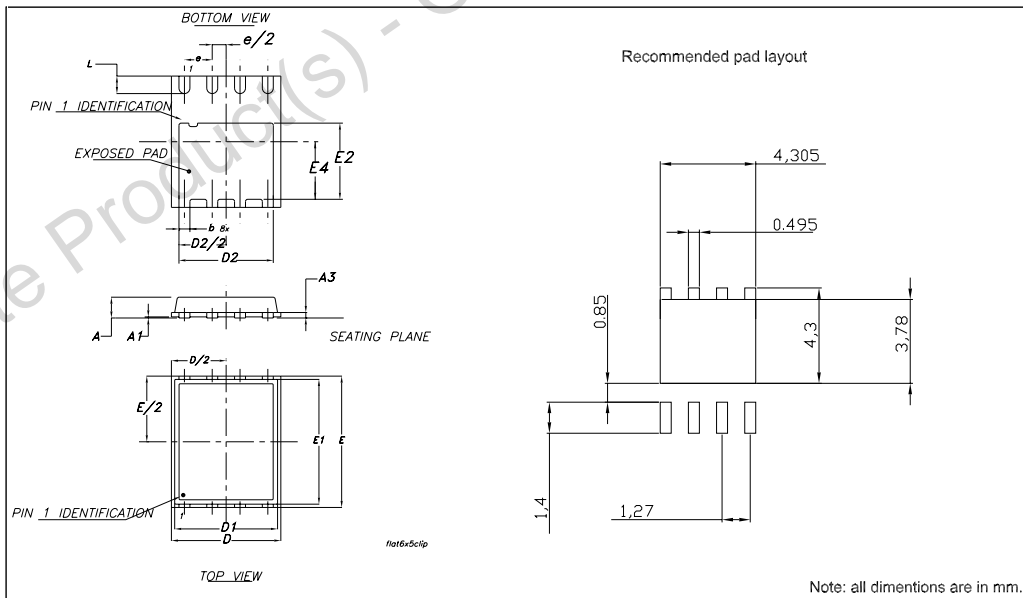
## 4 Package mechanical data

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Obsolete Product(s) - Obsolete Product(s)  
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PowerFLAT™ (6x5) mechanical data

DIM .	mm .			inch		
	Min .	Typ .	Max .	Min .	Typ .	Max .
A	0.80	0.83	0.93	0.031	0.32	0.036
A1		0.02	0.05		0.0007	0.0019
A3		0.20			0.007	
b	0.35	0.40	0.47	0.013	0.015	0.018
D		5.00			0.196	
D1		4.75			0.187	
D2	4.15	4.20	4.25	0.163	0.165	0.167
E		6.00			0.236	
E1		5.75			0.226	
E2	3.43	3.48	3.53	0.135	0.137	0.139
E4	2.58	2.63	2.68		0.103	0.105
e		1.27			0.050	
L	0.70	0.80	0.90	0.027	0.031	0.035



## 5 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
17-Apr-2008	1	First release

Obsolete Product(s) - Obsolete Product(s)  
Obsolete Product(s) - Obsolete Product(s)

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