

STHDLS101A

Enhanced AC coupled HDMI level shifter with configurable HPD output

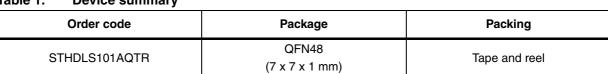
Features

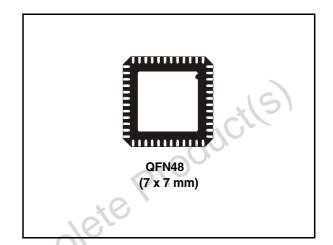
- Converts low-swing alternating current (AC) coupled differential input to high-definition multimedia interface (HDMI) rev 1.3 compliant
- HDMI level shifting operation up to 2.7 Gbps per lane
- Integrated 50 Ω termination resistors for ACcoupled differential inputs
- Input/output transition minimized differential signaling (TMDS) enable/disable
- Output slew rate control on TMDS outputs to minimize electromagnetic interference (EMI) and eliminate external components such as RC and choke
- Fail safe outputs for backdrive protection
- No re-timing or configuration required
- Inter-pair output skew < 250 ps, intra-pair output skew < 10 ps
- Single power supply of 3.3 V
- ESD protection: ±6 KV HBM on all I/O pins
- Integrated display data channel (DDC) level shifters. Pass-gate voltage limiters allow 3.3 V termination on graphics and memory controller hub (GMCH) pins and 5 V DDC termination on HDMI connector pins
- Level shifter and configurable output for HPD signal from HDMI/DVI connector
- Integrated pull-down resistor on HPD_SINK and OE_N inputs

Applications

Notebooks, PC motherboards and graphic cards

Table 1. Device summary





Description

The STHDLS101A is a high-speed high-definition multimedia interface (HDMI) level shifter that converts low-swing AC coupled differential input to HDMI 1.3 compliant open-drain current steering RX-terminated differential output. Through the existing PCI-E pins in the graphics and memory controller hub (GMCH) of PCs or notebook motherboards, the pixel clock provides the required bandwidth (1.65 Gbps, 2.25 Gbps) for the video supporting 720p, 1080i, 1080p with a total of 36-bit resolution. The HDMI is multiplexed onto the PCIe pins in the motherboard where the AC coupled HDMI at 1.2 V is output by GMCH. The AC coupled HDMI is then level shifter by this device to 3.3 V DC coupled HDMI output.

The STHDLS101A supports up to 2.7 Gbps, which is enough for 12-bits of color depth per channel, as indicated in HDMI rev 1.3.

The device operates from a single 3.3 V supply and is available in a 48-pin QFN package.

Contents STHDLS101A

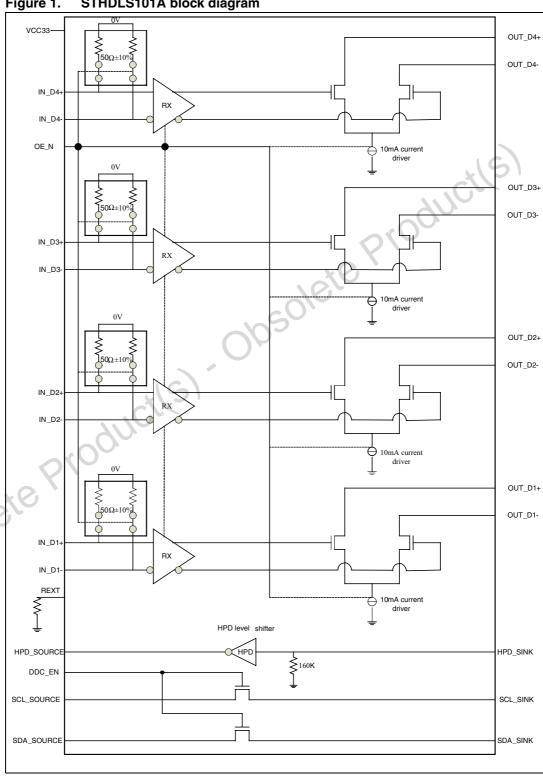
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STHDLS101A **Block diagram**

Block diagram





System interface STHDLS101A

System interface 2

Figure 2. System inferface

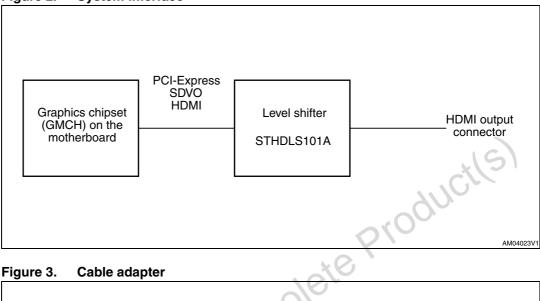
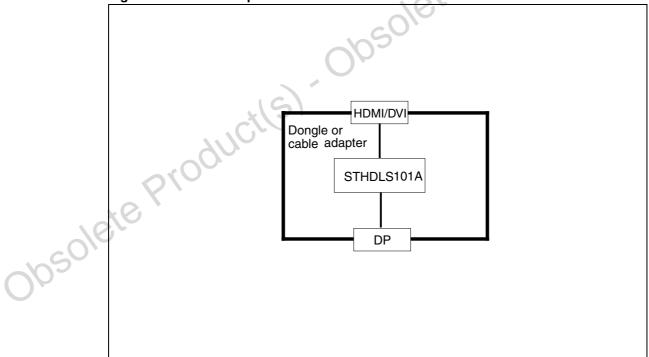


Figure 3. Cable adapter



577 4/24 Doc ID 15756 Rev 1

STHDLS101A System interface

HDMI/DVI Connector HPD HPD_SINK HPD_SOURCE HDMI/DVI DC TMDS Transmitter STHDLS101A HDMI/DVI Cable AC_TMDS AC_TMDS Adaptor DDC DDC DDC 占 Obsolete Product(s).

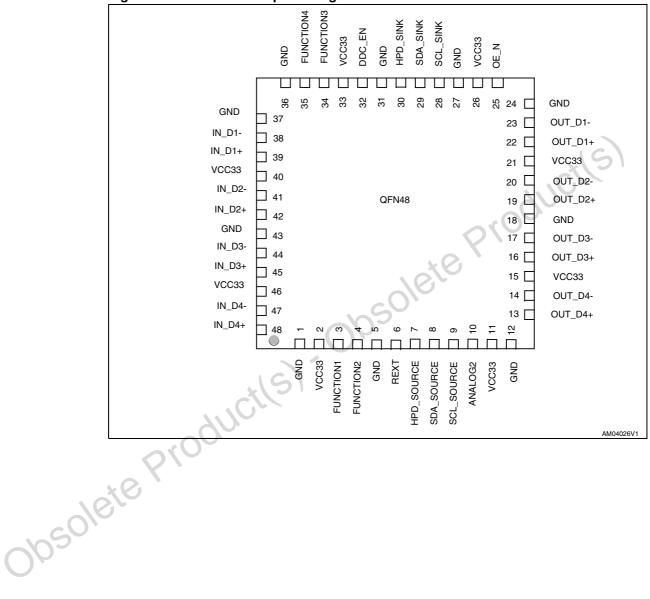
Figure 4. DP to HDMI/DVI cable adapter

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Pin configuration STHDLS101A

3 Pin configuration





6/24 Doc ID 15756 Rev 1

STHDLS101A Pin configuration

3.1 Pin description

Table 2. Pin description

	Table 2.	Pin description				
	Pin number	Name	Туре		Function	
	1	GND	Power	Ground		
	2	VCC33	Power	3.3 V±10% DC sup	ply	
	3	FUNCTION1	Vendor-specific control or test pins	Function pins are to test modes. For nor GND or VCC33 For consistent interedefault connection for 6dB lift at high frequency	mal operation, the operability, GND or these signals.	ese pins are tied to
	4	FUNCTION2	Vendor-specific control or test pins	Function pins are to test modes For normal operatio VCC33 For consistent intered default connection f equalizer gain at all	n, these pins are operability, GND or these signals.	tied to GND or
	5	GND	Power	Ground		
	6	REXT	Analog	Connection to external resistor. Resistor value specified by device manufacturer. Acceptable connections to this pin are: - Resistor to GND - Resistor to 3.3 V - NC (direct connections to V _{CC} or GND are three 0 Ω resistor for layout compatibility		
	7	100		Buffer from the 0 V to 5 V input signal. The output buffer stage is configurable based on the FUNCTION3 pin settings as desribed in the table below:		
10				FUNCTION3	HPD_SINK	HPD_SOURCE
5016		HPD_SOURCE	Output	0	Low	Open-drain, connected an external pull up to the desired supply (normally 1 V)
				0	High (5 V)	Low (0 V)
				1	Low (0 V)	Low (0 V)
				1	High (5 V)	High (3 V)
	8	SDA_SOURCE	I/O	3.3 V DDC data I/O to 3.3 V. Connected limiting integrated N	to SDA_SINK th	

Pin configuration STHDLS101A

Table 2. Pin description (continued)

		i in description (continued)			
	Pin number	Name	Туре	Function	
	9	SCL_SOURCE	Input	3.3 V DDC clock I/O. Pulled-up by external termination to 3.3 V. Connected to SCL_SINK through voltage-limiting integrated NMOS pass-gate	
	10	ANALOG2	Analog	Analog connection determined by vendor. Acceptable connections to this pin are: - Resistor or capacitor to GND - Resistor or capacitor to 3.3 V - Short to 3.3 V or to GND - NC	
	11	VCC33	Power	3.3 V ±10% DC supply	
	12	GND	Power	Ground	
	13	OUT_D4+	Output	HDMI 1.3 compliant TMDS output OUT_D4+ makes a differential output signal with OUT_D4-	
	14	OUT_D4-	Output	HDMI 1.3 compliant TMDS output OUT_D4- makes a differential output signal with OUT_D4+	
	15	VCC33	Power	3.3 V±10% DC supply	
	16	OUT_D3+	Output	HDMI 1.3 compliant TMDS output OUT_D3+ makes a differential output signal with OUT_D3-	
	17	OUT_D3-	Output	HDMI 1.3 compliant TMDS output OUT_D3- makes a differential output signal with OUT_D3+.	
	18	GND	Power	Ground	
	19	OUT_D2+	Output	HDMI 1.3 compliant TMDS output OUT_D2+ makes a differential output signal with OUT_D2	
30/e	20	OUT_D2-	Output	HDMI 1.3 compliant TMDS output OUT_D2- makes a differential output signal with OUT_D2+	
r	21	VCC33	Power	3.3 V±10% DC supply	
	22	OUT_D1+	Output	HDMI 1.3 compliant TMDS output. OUT_D1+ makes a differential output signal with OUT_D1-	
	23	OUT_D1-	Output	HDMI 1.3 compliant TMDS output. OUT_D1- makes a differential output signal with OUT_D1+	
	24	GND	Power	Ground	

STHDLS101A Pin configuration

Table 2. Pin description (continued)

	Table 2.	ble 2. Pin description (continued)				
	Pin number	Name	Туре		Function	
				Enable for level shit single-ended input. when unconnected	Internal pull-dow	
	25	OE_N	Input	OE_N	IN_D termination	OUT_D Outputs
				1	High-Z	High-Z
				0	50 Ω	Active
	26	VCC33	Power	3.3 V±10% DC sup	ply	
	27	GND	Power	Ground		4(3)
	28	SCL_SINK	Output	5 V DDC Clock I/O. to 5 V. Connected to limiting integrated N	o SCL_SOURCE	through voltage-
	29	SDA_SINK	I/O	5V DDC Data I/O. Pulled-up by external termination to 5V. Connected to SDA_SOURCE through voltage-limiting integrated NMOS pass-gate		
30 HPD_SINK Input signal comes from the Hi indicates "plugged" state				the HDMI connect state; voltage lo HPD_SINK is pul	5V (nominal) input signal. This e HDMI connector. Voltage high ate; voltage low indicates PD_SINK is pulled down by an I-down resistor	
	31	GND	Power	Ground		
	-9/1/0			Enables bias voltage to the DDC pass-gate level shifter gates. (May be implemented as a bias voltage connection to the DDC pass-gate themselves)		
	32	DDC_EN	Input	DDC_EN	Pas	s-gate
	C. Y			0 V	Disabled	
10				3.3 V	Enabled	
	33	VCC33	Power	3.3 V±10% DC sup	ply	
Ops	34	FUNCTION3	Input	Used for polarity control of the HPD_SOURCE out When L, the HPD_SOURCE is an open-drain outp sand when H, the HPD_SOURCE is a buffered ou (O V to V_{CC})		pen-drain output
	35	FUNCTION4	Vendor-specific control or test pins	Function pins are to enable vendor-specific features of test modes For normal operation, these pins are tied to GND or VCC33 For consistent interoperability, GND is the preferred default connection for these signals		
	36	GND	Power	Ground		
	37	GND	Power	Ground		

Pin configuration STHDLS101A

Table 2. Pin description (continued)

Name	Туре	Function
IN_D1-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D1- makes a differential pair with IN_D1+
IN_D1+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D1+ makes a differential pair with IN_D1-
VCC33	Power	3.3 V±10% DC supply
IN_D2-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D2- makes a differential pair with IN_D2+
IN_D2+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D2+ makes a differential pair with IN_D2-
GND	Power	Ground
IN_D3-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3- makes a differential pair with IN_D3+
IN_D3+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D3+ makes a differential pair with IN_D3-
VCC33	Power	3.3 V±10% DC supply
IN_D4-	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4- makes a differential pair with IN_D4+
IN_D4+	Input	Low-swing differential input from GMCH PCIE outputs. IN_D4+ makes a differential pair with IN_D4-
roduc	(6)	
	IN_D1- IN_D1+ VCC33 IN_D2- IN_D2+ GND IN_D3- IN_D3+ VCC33 IN_D4-	IN_D1- Input IN_D1+ Input VCC33 Power IN_D2- Input IN_D2+ Input GND Power IN_D3- Input IN_D3- Input VCC33 Power IN_D3+ Input VCC33 Power IN_D4- Input

4 Functional description

The section describes the basic functionality of the STHDLS101A device.

Power supply

The STHDLS101A is powered by a single DC power supply of 3.3 V \pm 10%.

Clocking

This device does not retime any data. The device contains no state machines. No inputs or outputs of the device are latched or clocked.

Reset

This device acts as a level shifter, reset is not required.

OE_N function

When OE_N is asserted (low level), the IN_D and OUT_D signals are fully functional. Input termina-tion resistors are enabled and any internal bias circuits are turned on.

OE_N pin has an internal pull-down that enables the chip if left unconnected.

When OE_N is de-asserted (high level), the OUT_D outputs are in high impedance state. The IN_D input buffers are disabled and the IN_D termination resistors are disabled. Internal bias circuits for the differential inputs and outputs are turned off. Power consumption of the chip is minimized.

The HPD_SINK input and HPD_SOURCE output are not affected by OE_N. The SCL and SDA pass-gates are not affected by OE_N.

Table 3. OE N description

	OE_N	Device state	Comments
10	Asserted (low level) or unconnected	Differential input buffers and output buffers enabled. Input impedance = 50Ù	Normal functioning state for IN_D to OUT_D level shifting function.
Obsoli		Low-power state. Differential input buffers and terminations are disabled. Differential input buffers are in high-impedance state.	Intended for lowest power condition when: No display is plugged in or The level shifted data path is disabled
	De-asserted (high level)	OUT_D level shifting outputs are disabled. OUT_D level shifting outputs are in a high-impedance state. Internal bias currents are turned off.	HPD_SINK input and HPD_SOURCE output are not affected by OE_N. SCL_SOURCE, SCL_SINK, SDA_SOURCE and SDA_SINK signals and functions are not affected by OE_N.

Table 4. OE_N function

	OE_N	IN_Dx	OUT_Dx (TMDS outputs)	Notes
	De-asserted (high level)	High-Z	High-Z	Device disabled. Low power state. Internal bias currents are disabled.
	Asserted or unconnected (low level)	50 Ω termination	Enabled	Level shifting mode enabled.
Obsole	ite Produc	31(6)	oletePi	oduci(s)

STHDLS101A Maximum ratings

5 Maximum ratings

Stressing the device above the rating listed in the "Absolute maximum ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute maximum rating conditions for extended periods may affect device reliability.

Table 5. Absolute maximum ratings

Symbol	Parame	Parameter		
V _{CC}	Supply voltage to ground potentia	al	-0.5 to +4.0	V
VI	DC input voltage (TMDS and PC	-0.5 to +4.0	٧	
	Control pins	-0.5 to +4.0	V	
	SDA_SINK, SCL_SINK, HPD_SI	-0.5 to +6	V	
I _O	DC output current	120	mA	
P_{D}	Power dissipation	*6,	1	W
T _{STG}	Storage temperature	16/2	-65 to +150	°C
T _L	Lead temperature (10 sec)	300	°C	
V _{ESD}	Electrostatic discharge voltage on IOs ⁽¹⁾	uman body model	±6	kV

^{1.} In accordance with the MIL standard 883 method 3015

Table 6. Thermal data

	Symbol	Parameter	QFN48	Unit
	θ_{JA}	Junction-ambient thermal coefficient	48	°C/W
Obsole	ie,			

Maximum ratings STHDLS101A

Recommended operating conditions 5.1

Power supply and temperature range 5.1.1

Table 7. Power supply and temperature range

Symbol	Parameter	Comments	Min	Тур	Max	Unit
V _{CC33}	3.3 V power supply		3.0	3.3	3.6	V
I _{CC}	Maximum power supply current	Total current from V _{CC} 3.3 V power supply	_	-	120	mA
Т	Operating temperature range		-40	_	85	°C

Differential inputs (IN_D signals) 5.1.2

Table 8. Differential input characteristics for IN_D signals

Т	Operating temperature range		-40	-	85	°C				
5.1.2	1,10,0									
Table 8. Differential input characteristics for IN_D signals Symbol Parameter Comments Min Typ Max L										
Tbit	Unit interval	Tbit is determined by the display mode. Nominal bit rate ranges from 250 Mbps to 2.5 Gbps per lane. Nominal Tbit at 2.5 Gbps = 400 ps. 360 ps = 400 ps - 10%	360	_	-	ps				
V _{RX-DIFFp-p}	Differential input peak to peak voltage	V _{RX-DIFFp-p} =2*IV _{RX-D+} - V _{RX-D-1} . Applies to IN_D signals.	0.2	_	1.2	V				
T _{RX-EYE}	Minimum eye width at IN_D input pair	The level shifter may add a maximum of 0.02UI jitter	0.8	_	_	Tbit				
V _{CM-AC-pp}	AC peak common mode input voltage	VCM-AC-pp=IVRX-D+ + VRX-D-I/2 - VRX-CM-DC. VRX-CM-DC=DC(avg) of IVRX-D+ + VRX-D-I/2 VCM-AC-pp includes all frequencies above 30 kHz.	_	-	100	mV				
Z _{RX-DC}	DC single-ended input impedance	Applies to IN_D+ as well as IN_D- pins (50 Ω ± 20% tolerance)	40	50	60	Ω				
V _{RX-Bias}	RX input termination voltage	Intended to limit power-up stress on chipset's PCIE output buffers	0	_	2	V				
Z _{RX-HIGH-Z}	Single-ended input resistance for IN_Dx when inputs are in high-Z state	Differential inputs must be in a high impedance state	100	_	_	ΚΩ				

STHDLS101A Maximum ratings

5.2 TMDS outputs (OUT_D signals)

The level shifter's TMDS outputs are required to meet the HDMI 1.3 specifications. The HDMI 1.3 specification is assumed to be the correct reference in instances where this document conflicts with the HDMI 1.3 specification.

Table 9. Differential output characteristics for TMDS OUT_D signals

Symbol	Parameter	Comments	Min	Тур	Max	Unit
V _H	Single-ended high level output voltage	AV _{CC} is the DC termination voltage in the HDMI or DVI sink. AV _{CC} is nominally 3.3 V	AV _{CC} -10 mV	AV _{CC}	AV _{CC} +10 m V	V
V _L	Single-ended low level output voltage	The open-drain output pulls down form AV _{CC}	AV _{CC} - 600 mV	AV _{CC} - 500 mV	AV _{CC} - 400 mV	V
V _{SWING}	Single-ended output swing voltage	Swing down from TMDS termination voltage (3.3 V ±10%)	400 mV	500 mV	600 mV	V
I _{OFF}	Single-ended current in high-Z state	Measured with TMDS outputs pulled up to AV $_{CC}$ max (3.6 V) through 50 Ω resistors	- *6	b.i.o.	10	μΑ
T _R	Rise time	Maximum rise/fall time at 2.7 Gbps = 148ps. 125ps = 148 - 15%	125 ps	-	0.4 Tbit	ps
T _F	Fall time	Maximum rise/fall time at 2.7 Gbps = 148 ps. 125ps = 148 - 15%	125 ps	_	0.4 Tbit	ps
T _{SKEW} -	Intra-pair differential skew	This differential skew budget is in addition to the skew presented between D+ and D-paired input pins.	_	_	10	ps
T _{SKEW} -	Inter-pair lane to lane output skew	This lane to lane skew budget is in addition to the skew between differential input pairs.	_	_	250	ps
OT JIT	Jitter added to TMDS signals	Jitter budget for TMDS signals as they pass through the level shifter. 7.4 ps = 0.02 Tbit at 2.7 Gbps	_	-	7.4	ps

Maximum ratings STHDLS101A

5.3 HPD input and output characteristics

Table 10. HPD_SINK input and HPS_SOURCE output

Symbol Parameter		Comment	Min	Тур	Max	Uni
V _{IH-HPD_SINK}	HPD_SINK input high level	Low speed input changes state on cable plug/unplug	2	5.0	5.3	V
V _{IL-HPD_SINK}	HPD_SINK input low level		0	_	0.8	٧
I _{IN-HPD_SINK}	HPD_SINK input leakage current	Measured with HPD_SINK at V _{IH-HPD} max and V _{IL-HPD} min	_	-	50	μA
V _{OL} -	HPD_SOURCE output low level when FUNCTION3 = H	V _{CC} = 3.3 V ±10%	2.5	_	V _{CC}	V
V _{OH} - HPD_SOURCE (INV)	HPD_SOURCE output high level when FUNCTION3 = L	$V_{CC} = 3.3 \text{ V} \pm 10\%$ $I_{OL} = 1 \text{ mA}$	0	1917	0.2	٧
V _{OL} -	HPD_SOURCE output low level when FUNCTION3 = H	V _{CC} = 3.3 V ±10%	0	_	0.2	٧
T _{HPD}	HPD_SINK to HPD_SOURCE propagation delay	Time from HPD_SINK changing state to HPD_SOURCE changing state. Includes HPD_SOURCE rise/fall time C _I =10 pF	_		200	ns
T _{RF-HPD}	HPD_SOURCE rise/fall time	Time required to transition from V _{OH-HPD_SOURCE} to V _{OL-HPD_SOURCE} or from V _{OL-HPD_SOURCE} to V _{OH-HPD_SOURCE} C _I =10 pF	1	_	20	ns

STHDLS101A Maximum ratings

5.4 DDC input and output chatacteristics

Table 11. SDA_SOURCE, SCL_SOURCE and SDA_SINK, SCL_SINK characteristics

Symb ol	Parameter	Comment	Min	Тур	Max	Unit
VI	Input voltage on SDA_SINK, SCL_SINK pins	Voltage on the DDC pins on connector end	0	ı	5.5	V
I _{LKG}	Input leakage current on SDA_SINK, SCL_SINK pins	V_{CC} = 3.3 V V_{I} =0.1 V_{DD} to 0.9 V_{DD} to isolated DDC inputs V_{DD} = external pull-up resistor voltage on SDA_SINK and SCL_SINK inputs (maximum of 5.5 V)	-10	-	10	μΑ
I _{OFF}	Power-down leakage current on SDA_SINK, SCL_SINK pins	$\begin{split} &V_{CC} = 0.0 \text{ V} \\ &V_I = 0.1 \text{ V}_{DD} \text{ to } 0.9 \text{ V}_{DD} \text{ to} \\ &DDC \text{ sink inputs} \\ &V_{DD} = \text{external pull-up} \\ &\text{resistor voltage on} \\ &SDA_SINK \text{ and SCL_SINK} \\ &\text{inputs (maximum of } 5.5 \text{ V)} \\ &SDA_SOURCE, \\ &SCL_SOURCE = 0.0 \text{ V} \end{split}$	-10	-	10	μА
C _{I/O}	Input/output capacitance (switch off)	V _{I(pp)} =1 V, 100 KHz V _{CC} =3.3 V, T=25C	-	5	_	pF
C _{I/O}	Input/output capacitance (switch on)	$V_{I(pp)}$ =1 V, 100KHz V_{CC} = 3.3 V, T= 25 ° C	_	_	10	pF
R _{ON}	Switch resistance	$I_O=3 \text{ mA}, V_O=0.4 \text{ V}$ $V_{CC}=3.3 \text{ V}$	_	27	40	Ω
T _{PD}	DDC_SINK to DDC_SOURCE propagation delay	Time from DDC_SINK changing state to DDC_SOURCE changing state while the pass gate is enabled. CL=10 pF RPU=1.5 K (min), 2.0 K (max)	_	8	15	ns
T _{SX}	Switch time from DDC_EN to the valid state on DDC_SOURCE	C _L = 10 pF R _{PU} = 1.5 K (min), 2.0 K (max)	_	8	15	ns

STHDLS101A **Maximum ratings**

5.5 **OE_ input characteristics**

OE_N input characteristics Table 12.

Symbol	Parameter	Comment	Min	Тур	Max	Unit
V _{IH-OE_N}	Input high level		2	_	VCC33	V
V _{IL-OE_N}	Input low level		0	_	0.8	٧
I _{IN-OE_N}	Input leakage current	Measured with OE_N at VIH-OE_N max and VIL-OE_N min	-	_	200	μΑ

5.6 **HPD** input resistor

Table 13. **HDP** input resistor

5.6 Table 13.	HPD input resistor					
Symbol	Parameter	Comment	Min	Тур	Max	Unit
R _{HPD}	HPD_SINK input pull-down resistor	Guarantees HPD_SINK is LOW when no display is plugged in	130 K	160 K	190 K	Ω

ESD performance 5.7

ESD performance Table 14.

Symbol	Parameter	Test condition	Min	Тур	Max	Unit
ESD	MIL STD 883 method 3015 (all pins)	Human Body Model (HBM)	-6	_	+6	kV
obso	lete Pro					

6 Application information

6.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply V_{CC} before applying any signals to the input/output or control pins.

6.2 Supply bypassing

Bypass each of the V_{CC} pins with 0.1 μ F and 1nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the V_{CC} pin of the device as possible.

6.3 Differential traces

The high-speed inputs and TMDS outputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

- (a) Maintain 100 Ω differential transmission line impedance into and out of the device.
- (b) Keep an uninterrupted ground plane below the high-speed I/Os.
- (c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.
- (d) Layout of the TMDS differential outputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STHDLS101A. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

7 Package mechanical data

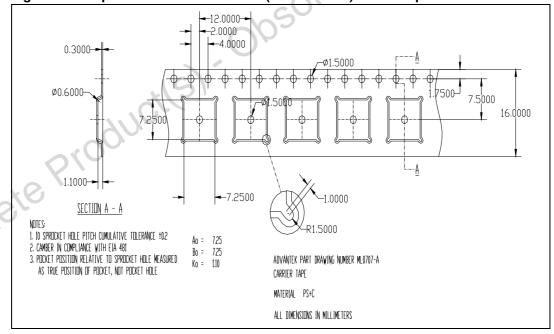
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 6. Package outline for QFN48 (7 x 7 x 1 mm) - 0.5 mm pitch **SEATING** PLANE С A3 PIN #1 ID R=0.20 Josole te R 24 D2 BOTTOM VIEW

Table 15. Package mechanical data for QFN48 (7 x 7 x 1 mm) - 0.5 mm pitch

Symbol	Min	Тур	Max	Min	Тур	Max
Α	0.80	0.90	1.00	0.80	0.85	1.00
A1	_	0.02	0.05	_	0.01	0.05
A2	_	0.65	1.00	_	0.65	_
A3	_	0.25	_	_	0.20	_
b	0.18	0.23	0.30	0.18	0.23	0.30
D	6.85	7.00	7.15	6.90	7.00	7.10
D2	2.25	4.70	5.25	SEE EXPOSED PAD VARIATIONS		
Е	6.85	7.00	7.15	6.90	7.00	7.10
E2	2.25	4.70	5.25	SEE EXPOSED PAD VARIATIONS		
е	0.45	0.50	0.55	0.45	0.50	0.55
L	0.30	0.40	0.50	0.30	0.40	0.50
ddd	_	_	0.08	10.	_	0.08

Figure 7. Tape information for QFN48 (7 x 7 x 1 mm) - 0.5 mm pitch



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Figure 8. Reel information for QFN48 (7 x 7 x 1 mm) - 0.5 mm pitch

Table 16. Reel mechanical data (dimensions in mm)

A	С	N	Т	
330.2	13 ±0.25	100	16.4	

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Table 17. Document revision history

Date	Revision	Changes
22-Jun-2009	1	Initial release.

Obsolete Product(s). Obsolete Product(s)

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