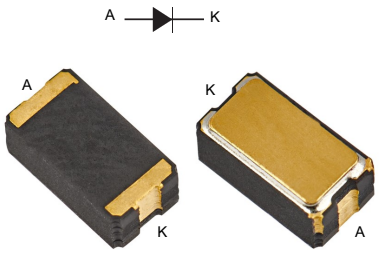
Aerospace 75 V, 0.5 A switching rectifier in LCC-2D package



Leadless chip-carrier 2 (LCC-2D)

Product status link
1N6640U

Product summary	
$I_{F(AV)}$	0.5 A
V_{RRM}	75 V
V_F(max.)	0.89 V at 50 mA and 25 °C
T_J(max.)	175 °C

Features

- Surface mount hermetic LCC-2D package
  - Low thermal case resistance: 60 °C/W
  - Low package mass, 120 mg
- Low leakage off state, I_R = 40 nA at 50 V
- Low forward voltage: V_F = 0.89 V at 50 mA and T_j = 25 °C
- Ultrafast switching, t_{rr} = 9 ns at I_F = I_R = 10 mA and T_j = 25 °C
- Radiation performance
  - 3 Mrad (Si) high dose rate
- ESCC qualified: detail specification 5101/027

Applications

- Satellite and spacecraft power systems
- Low power switch mode power supply
- Snubber diode for low power converter
- Auxiliary transistor driver diode
- Reverse polarity protection
- Redundancy OR-ing diode

Description

Designed for harsh cosmic radiation conditions, the 1N6640U is a 75 V low-leakage ultrafast rectifier that is housed in the lightweight, high thermal conductive LCC-2D package.

This hermetic surface mount package exhibits an industry standard compatible footprint, such as the D-5D.

This full planar technology 1N6640U rectifier allows superior performances and high reliability up to 175°C and is characterized in total ionizing dose for Rad-Hard applications.

This rectifier is ESCC qualified, which makes it eligible for use in space programs. It is typically used in low voltage switch-mode power converters, high frequency DC-to-DC, step-down regulators, or chopper drives, performing as free-wheeling diode, transistor driver diode, reverse polarity protection, or redundancy OR-ing diode.

1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
V_{RRM}	Repetitive peak reverse voltage		75	V
V_{RWM} (1)	Peak working reverse voltage		75	V
$I_{F(RMS)}$	RMS forward current		500	mA
$I_{F(AV)}$	Average forward current(2)		300	mA
I_{FSM}	Non repetitive surge forward current	t_p = 8.3 ms sinusoidal	2	A
T_{stg}	Storage temperature range		-65 to +175	°C
T_{op}	Operating temperature range (case temperature)		-65 to +175	°C
T_j	Maximum operating junction temperature		175	°C
T_{sol}	Maximum soldering temperature(3)		245	°C
ESD	Electro static discharge, air discharge, HBM model, class 3B		5.8	kV

1. *See Figure 1.*
2. *T_{case} = +155 °C derate linearly to 0 A at T_J = 175 °C.*
3. *Maximum duration 5 s. The same package cannot be re-soldered until 3 minutes have elapsed after initial soldering.*

Figure 1. V_{RRM} and V_{RWM} definition with their waveform

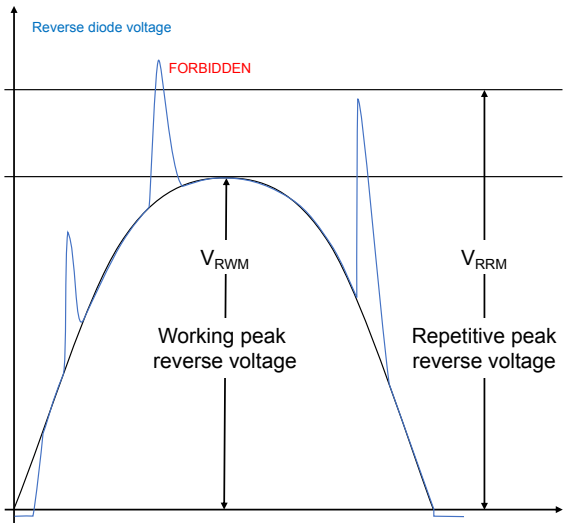


Table 2. Thermal parameters

Symbol	Parameter	Max. value	Unit
$R_{th(j-c)}$	Junction to case (DC) , mounted on infinite heat sink	60	°C/W
$R_{th(j-a)}$	Junction to ambient (DC)	280	°C/W

For more information, refer to the application note:

- AN5088: Rectifiers thermal management, handling and mounting recommendation

Table 3. Static electrical characteristics

Symbol	Parameter	Test conditions		Min.	Max.	Unit
V_{BR} (1)	Breakdwon voltage	I_R = 10 µA	T_j = 25 °C	75		V
I_R (1)	Reverse leakage current	V_R = 50 V	T_j = 25 °C		40	nA
			T_j = 150 °C		30	µA
V_F (2)	Forward voltage drop	I_F = 200 mA	T_j = -55 °C		1.2	V
		I_F = 200 mA	T_j = 25 °C	0.87	1.1	
		I_F = 100 mA	T_j = 25 °C	0.82	0.98	
		I_F = 50 mA	T_j = 25 °C	0.76	0.89	
		I_F = 1 mA	T_j = 25 °C	0.54	0.63	

1. *Pulse test: t_p = 5 ms, δ < 2%, δ = duty cycle*
2. *Pulse test: t_p = 680 µs, δ < 2%*

To evaluate the conduction losses, use the following equation:

$P = 0.74 \times I_{F(AV)} + 1.00 \times I_F{}^2{}_{(RMS)}$

For more information, refer to the following application notes related to the power losses:

- AN604: Calculation of conduction losses in a power rectifier
- AN4021: Calculation of reverse losses on a power diode

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Test conditions	Max.	Unit
t_{RR}	Reverse recovery time	$I_F = I_R$ = 10 mA(1)	T_j = 25 °C	9	ns
		I_F = 1 A, dI_F/dt = -15 A/µs, V_R = 30 V		20	
C_j	Total diode capacitance	V_{AC} = 50 mV, V_R = 0 V, F = 1 MHz	T_j = 25 °C	3	pF
V_{FP}	Forward recovery voltage	I_F = 200 mA	T_j = 25 °C	5	V
t_{FR}	Forward recovery time	I_F = 200 mA, V_{FR} = 1.1 x V_F(0.2A)	T_j = 25 °C	20	ns

1. *Guaranteed by design.*

1.1 Characteristics (curves)

Figure 2. Forward voltage drop versus forward current (typical values)

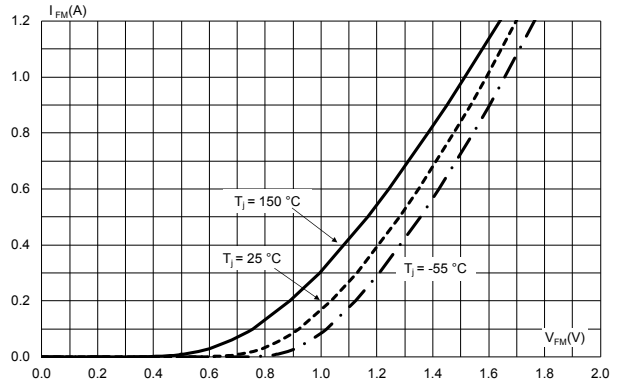


Figure 3. Forward voltage drop versus forward current (maximum values)

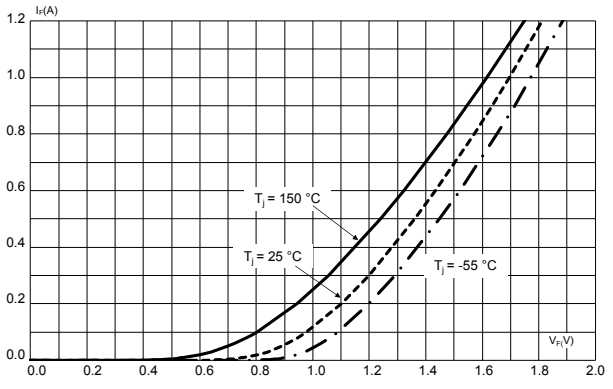


Figure 4. Reverse leakage current versus reapplied reverse voltage (typical values)

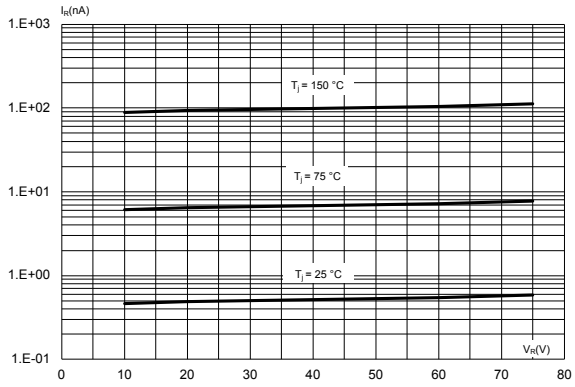


Figure 5. Relative variation of thermal impedance junction to case versus single square pulse duration

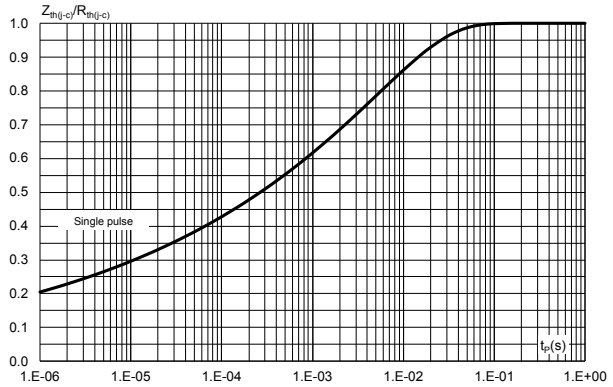
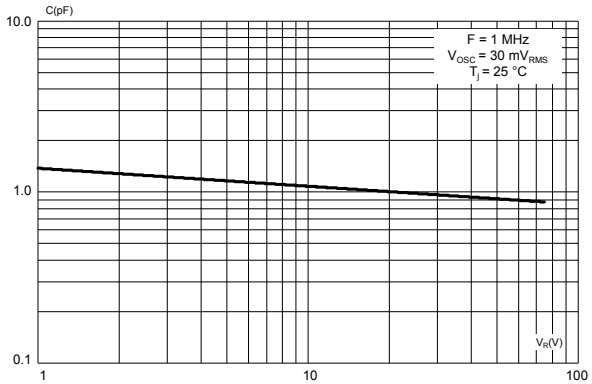


Figure 6. Junction capacitance versus reapplied reverse voltage (typical values)

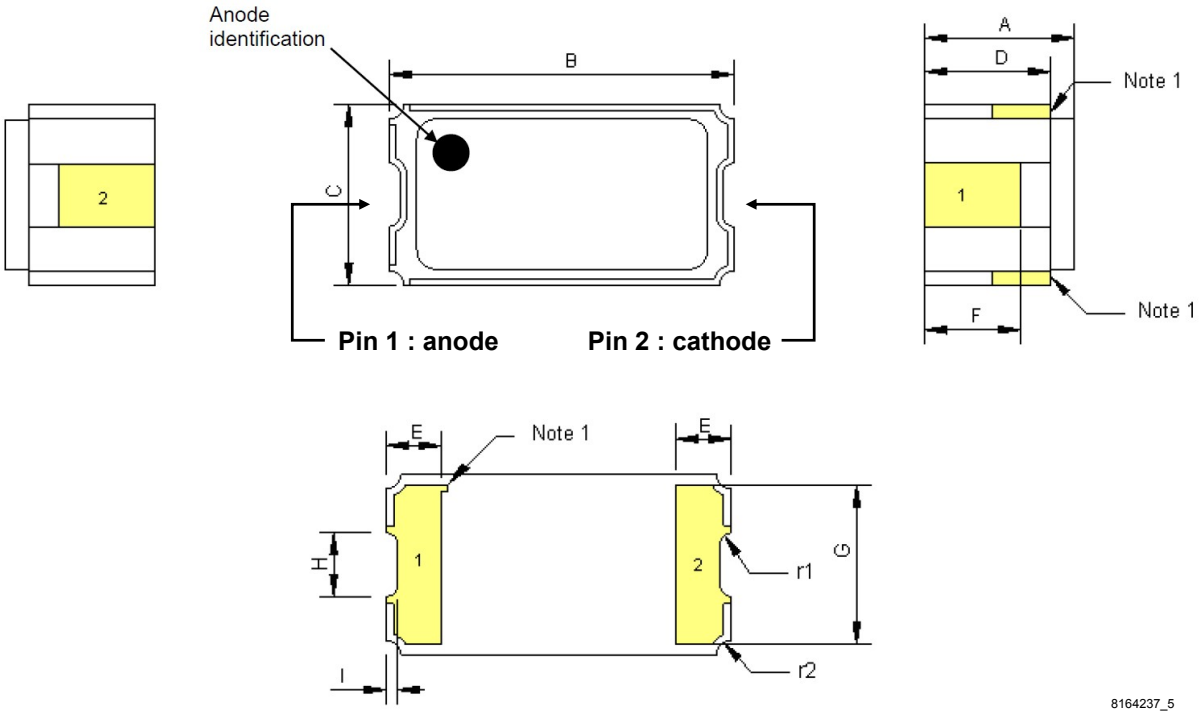


2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 LCC-2D package information

Figure 7. LCC-2D package outline



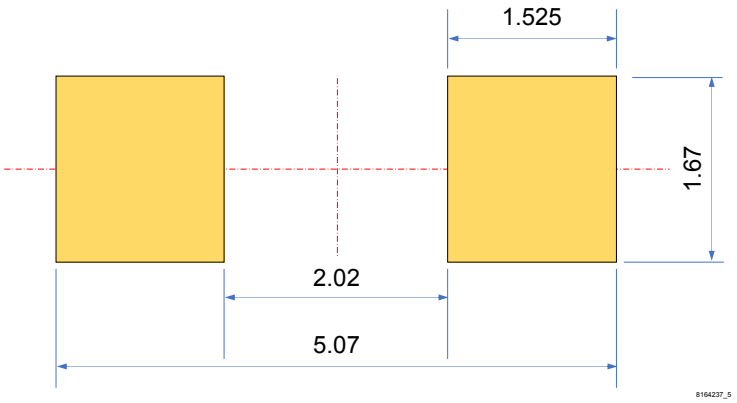
Note: The anode is identified by a metallization in two top angle castellations and by the index mark on the bottom metallization n° 1.

Table 5. **LCC-2D package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches (for reference only)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.86	2.03	2.20	0.073	0.080	0.087
B	4.44	4.57	4.77	0.175	0.180	0.188
C	1.84	1.97	2.10	0.072	0.078	0.083
D	1.53	1.70	1.87	0.060	0.067	0.074
E	0.48		0.71	0.019		0.028
F		1.3			0.051	
G		1.67			0.066	
H		0.37			0.015	
I		0.15			0.006	
r1		0.15			0.006	
r2		0.20			0.008	

Dimension data specified for the gold plated version and the solder dip version before tinning.

Figure 8. **LCC2-D footprint density level B**



3 Ordering information

Table 6. **Ordering information**

Order code	ESCC detail specification	Quality level	Package	Lead finishing	Product marking	Mass	Bulk qty.	Packing
1N6640UD1	-	Engineering model	LCC-2D	Gold	1N6640UD1	120 mg	50	Waffle pack
1N6640U01D	5101/027/07	Flight model		Gold	510102707			
1N6640U02D	5101/027/08	Flight model		Hot solder dip	510102708			

4 Other information

4.1 Product marking description

Here below is described the marking of the package of both the engineering and flight models.

Figure 9. ESCC flight model marking outline

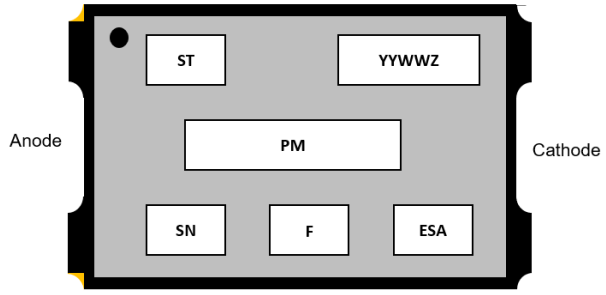


Table 7. ESCC flight model marking

Field	Description
ST	ST logo
YYWWZ	Date code and lot index in the week(1)
PM	Product marking
SN	Serialization number
F	Country of origin
ESA	ESA logo

1. *Date cote includes YY = two-digit year, WW = two-digit week, Z = assembly plant code.*

Figure 10. Engineering model marking outline

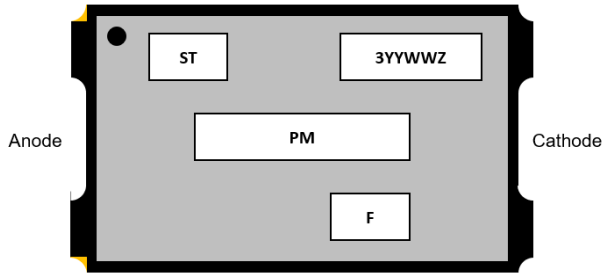


Table 8. Engineering model marking

Field	Description
ST	ST logo
YYWWZ	Date code and lot index in the week(1)
PM	Product marking
F	Country of origin

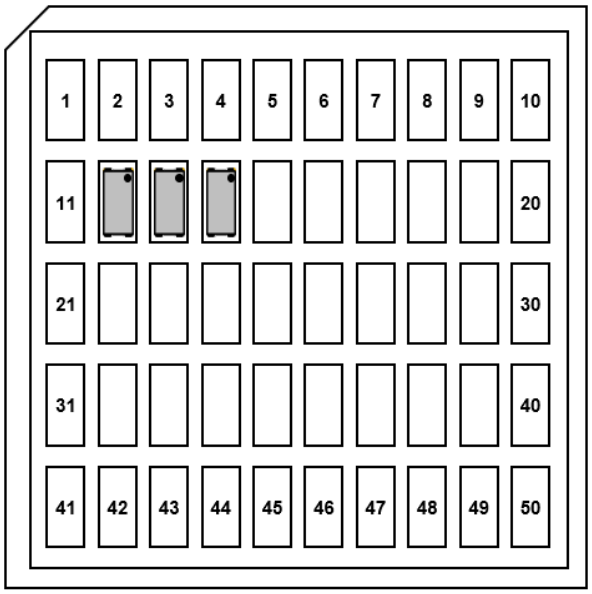
1. *Date cote includes YY = two-digit year, WW = two-digit week, Z = assembly plant code.*

4.2 Packing information

The 1N6640U versions are delivered in a 50-position, 50.8 x 50.8 mm² waffle pack consecutively populated from position 1.

The Figure 11 shows how to identify position 1, the orientation of the product in the waffle pack.

Figure 11. 1N6640U waffle pack outline



The diode anode is on the top pin of the device, and the anode identification dot is orientated at the opposite of the waffle pack truncated corner.

4.3 Documentation

In the Table 9 is a summary of the documentation provided with each type of products.

Table 9. Documentation provided for each type of product

Quality level	Documentation
Engineering model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Reference data sheet • Reference to TN1181 on engineering models • ST Rennes assembly lot ID
Flight model	Certificate of conformance including : • Customer name • Customer purchase order number • ST sales order number and item • ST part number • Quantity delivered • Date code • Serial numbers • Diffusion line (plant + wafer size) • Diffusion run (wafer lot number) and wafer ID • Reference of the applicable ESCC qualification maintenance lot • Reference to the ESCC detail specification • ST Rennes assembly lot ID number

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
26-Mar-2010	1	First issue.
23-Sep-2011	2	Updated order codes in *Table 1 Table 7*.
8-Nov-2013	3	Updated *Table 1*, *Table 5* and *Table 7* and inserted *Other information*.
04-Dec-2015	4	Updated *Table 7* and reformatted to current standard.
10-Feb-2026	5	Updated Section Features, Section Description, and Section 4: Other information. Added Section Applications and Section 4.2: Packing information. Minor text changes.

Contents

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