



STL100N1VH5

N-channel 12 V, 0.0022 Ω , 25 A PowerFLAT™ (5x6)
STripFET™ V Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D
STL100N1VH5	12 V	<0.003 Ω	25 A ⁽¹⁾

1. The value is rated according to R_{thj-pcb}

- R_{DS(on)} * Q_g industry benchmark
- Extremely low on-resistance R_{DS(on)}
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

Application

Switching applications

Description

This device is a 12 V N-channel STripFET™ V Power MOSFET which has been designed to achieve very low on-state resistance providing also one of the best-in-class figure of merit (FOM).



Figure 1. Pin-out configuration

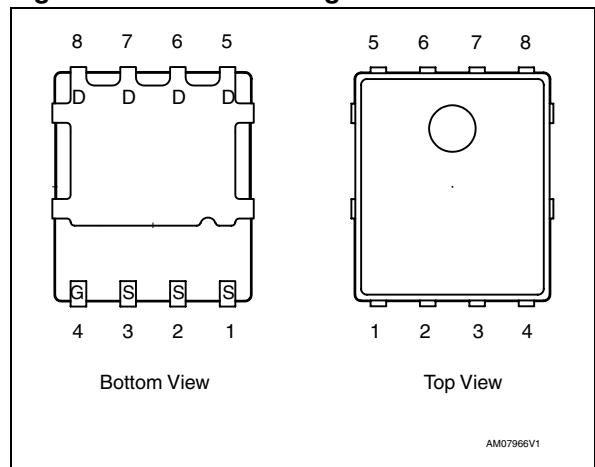


Table 1. Device summary

Order code	Marking	Package	Packaging
STL100N1VH5	100N1VH5	PowerFLAT™ (5x6)	Tape and reel

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Obsolete Product(s) - Obsolete Product(s)



1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	12	V
V_{GS}	Gate-source voltage	± 8	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	100	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	62.5	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	25	A
$I_D^{(2)}$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	15.6	A
$I_{DM}^{(3)}$	Drain current (pulsed)	100	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	60	W
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25^\circ\text{C}$	4	W
	Derating factor	0.03	W/ $^\circ\text{C}$
T_J T_{stg}	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. The value is rated according R_{thj-c}
2. The value is rated according $R_{thj-pcb}$
3. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case (Drain) (steady state)	2.08	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	31.3	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch², 2oz Cu, $t < 10$ sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current (pulse width limited by T_J Max)	12.5	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_D = I_{AV}$, $V_{DD} = 12$ V)	300	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	12			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ }^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.5			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 12.5\text{ A}$ $V_{GS} = 2.5\text{ V}$, $I_D = 12.5\text{ A}$		0.0022 0.0032	0.003 0.004	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 10\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	2085	-	pF
C_{oss}	Output capacitance			949		pF
C_{rss}	Reverse transfer capacitance			240		pF
Q_g	Total gate charge	$V_{DD} = 6\text{ V}$, $I_D = 12.5\text{ A}$	-	26.5	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		5.2		nC
Q_{gd}	Gate-drain charge	Figure 14		4.8		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD}=6\text{ V}$, $I_D=12.5\text{ A}$, $R_G=4.7\ \Omega$, $V_{GS}=4.5\text{ V}$ <i>Figure 13</i>	-	14.4	-	ns
t_r	Rise time			31.6		ns
$t_{d(off)}$	Turn-off delay time			50		ns
t_f	Fall time			16		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		25	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		100	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=25\text{ A}$, $V_{GS}=0$	-		1.1	V
t_{rr}	Reverse recovery time	$I_{SD}=25\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$, $V_{DD}=10\text{ V}$, $T_J=150\text{ }^\circ\text{C}$	-	49		ns
Q_{rr}	Reverse recovery charge			54		nC
I_{RRM}	Reverse recovery current			2.2		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration= 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

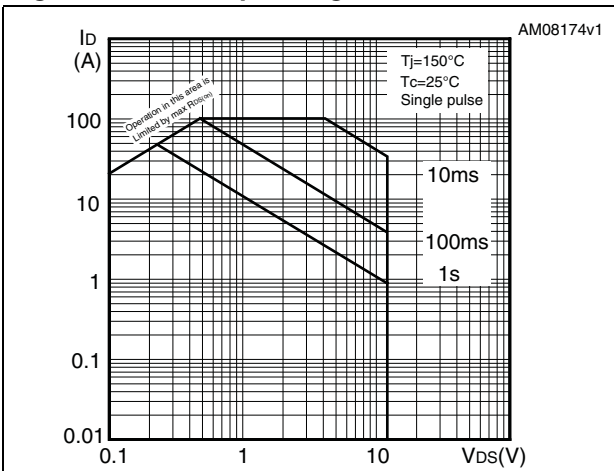


Figure 3. Thermal impedance

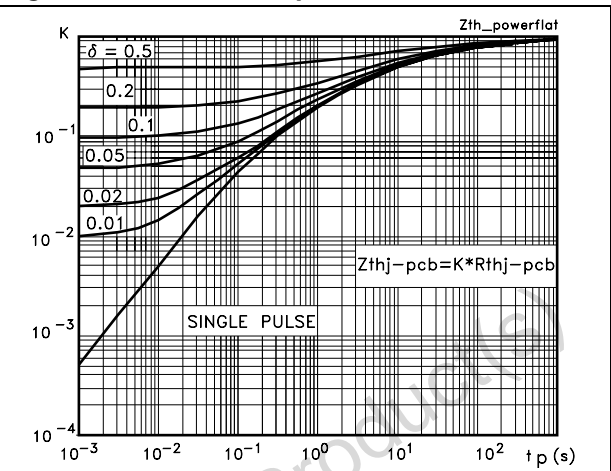


Figure 4. Output characteristics

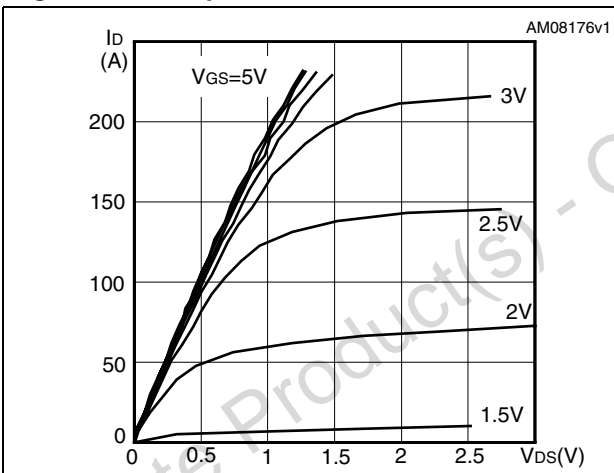


Figure 5. Transfer characteristics

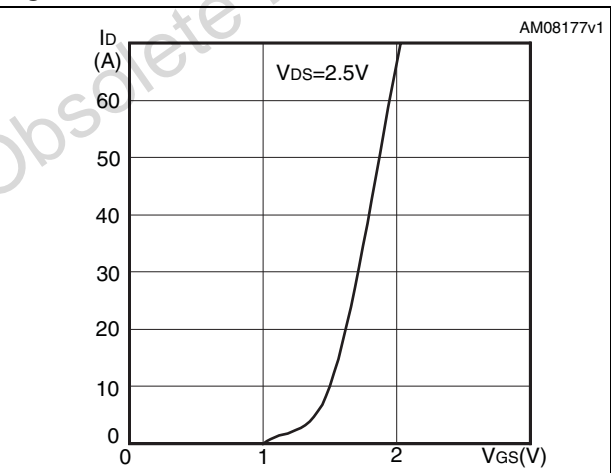


Figure 6. Normalized $B_{V_{DSS}}$ vs temperature

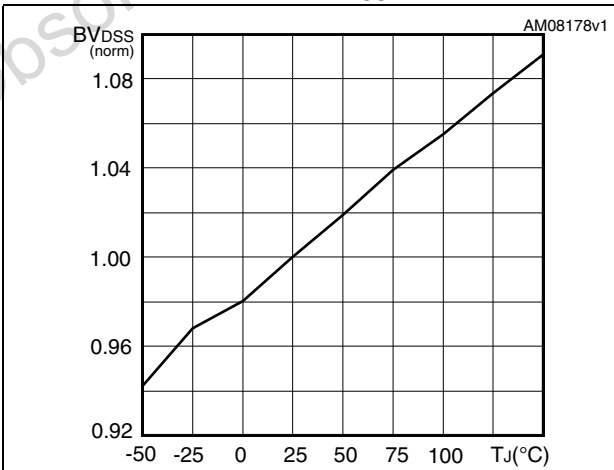


Figure 7. Static drain-source on resistance

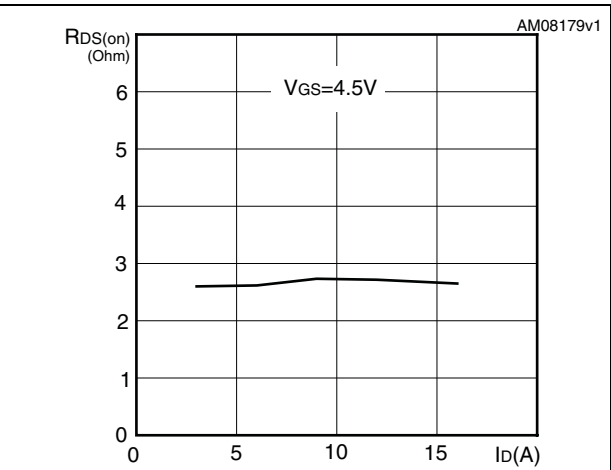


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

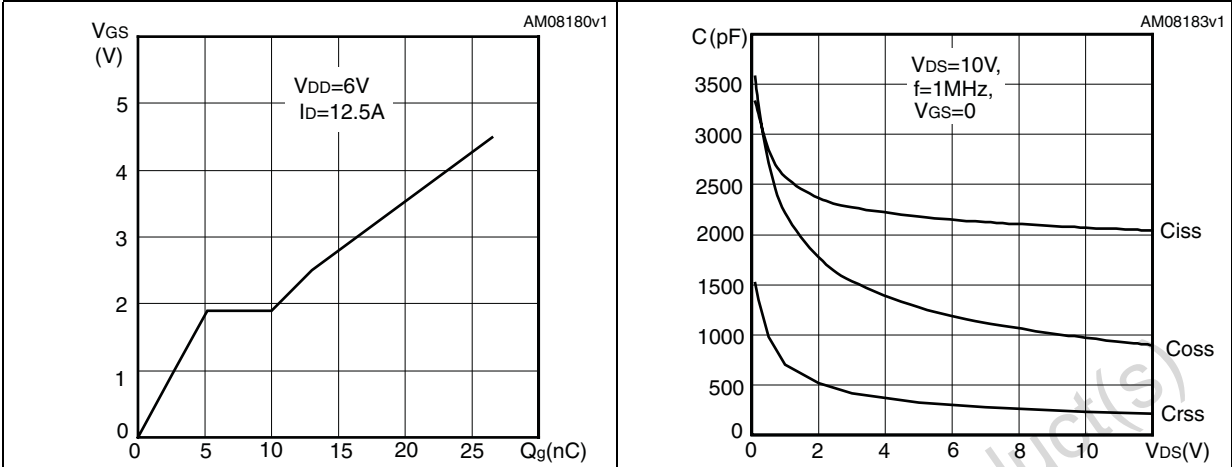


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

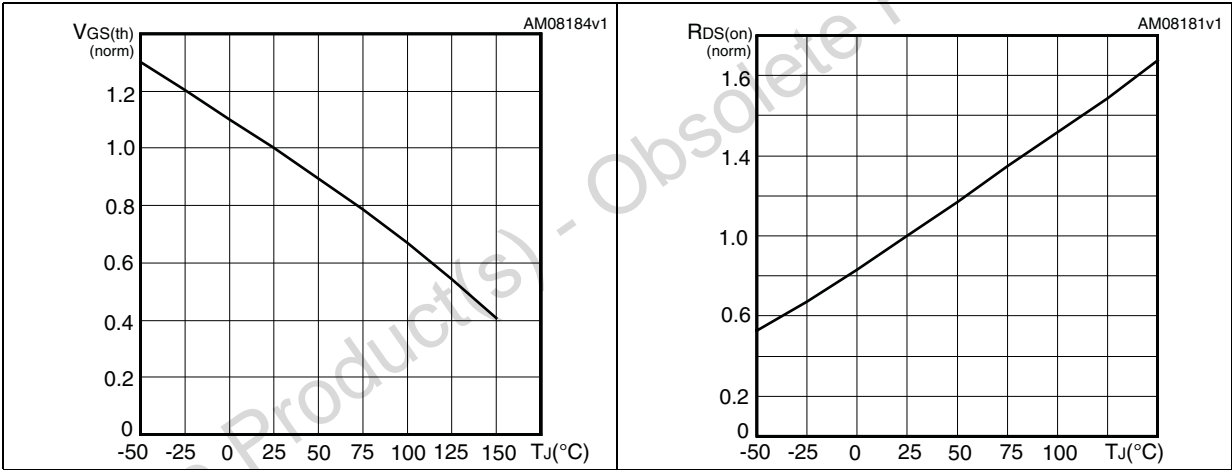
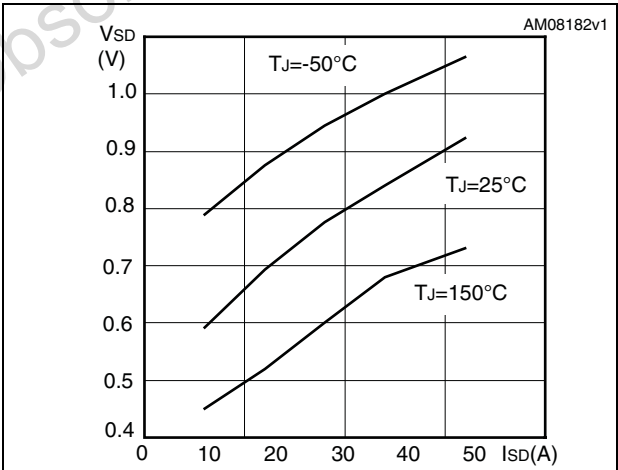


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

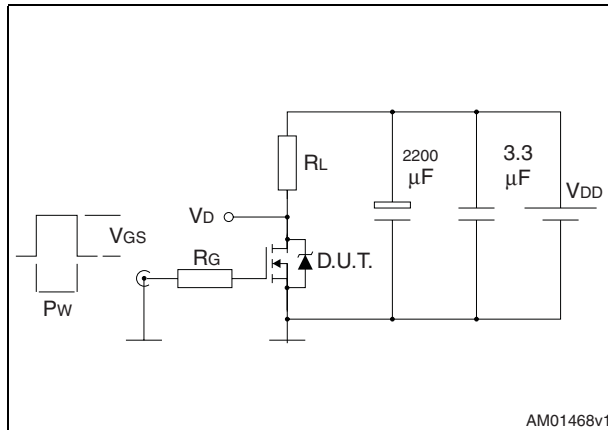


Figure 14. Gate charge test circuit

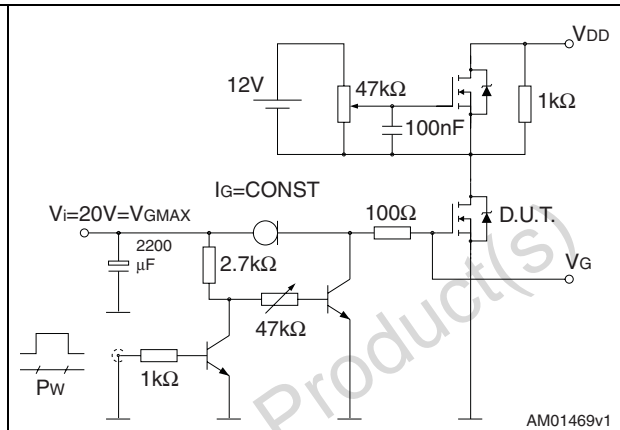


Figure 15. Test circuit for inductive load switching and diode recovery times

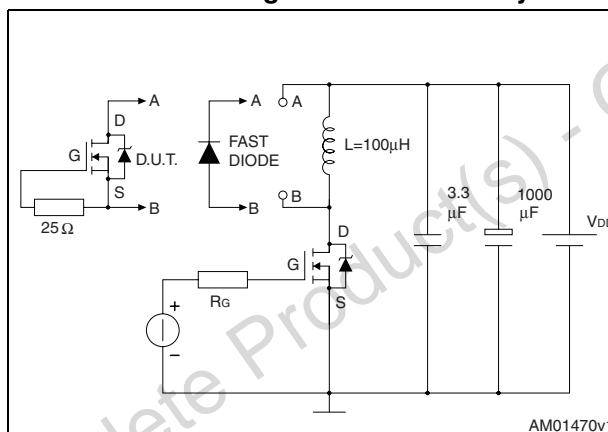


Figure 16. Unclamped inductive load test circuit

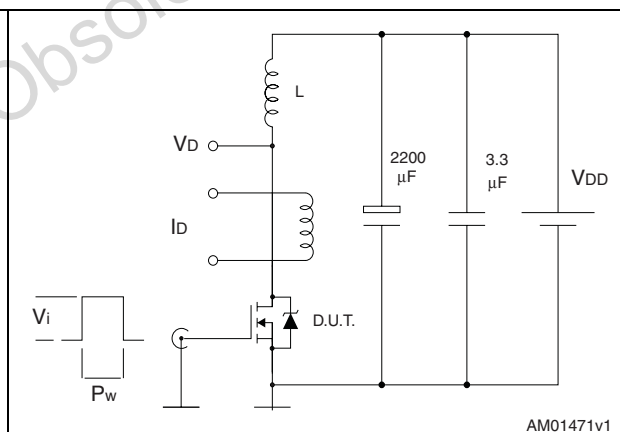


Figure 17. Unclamped inductive waveform

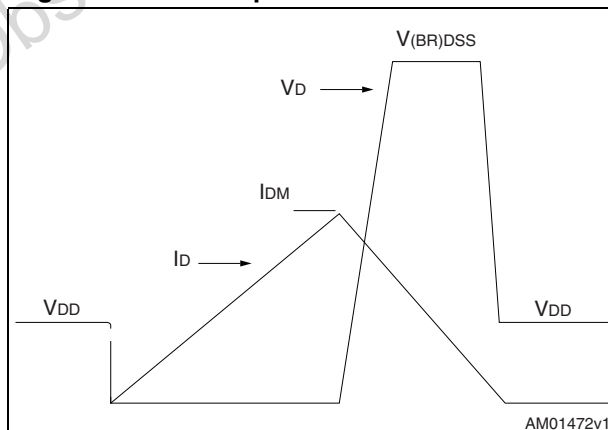
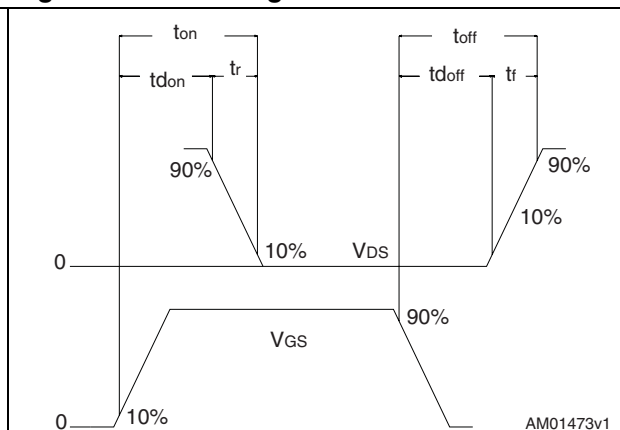


Figure 18. Switching time waveform



4 Package mechanical data

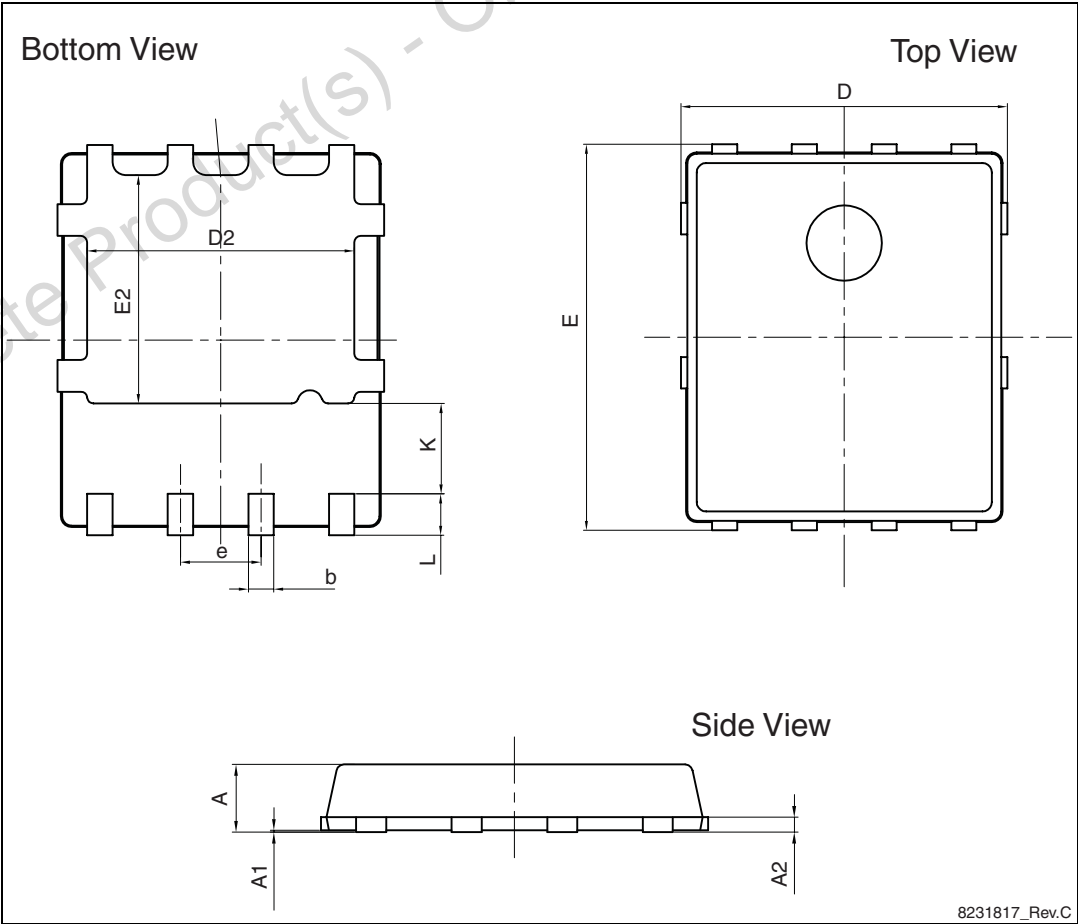
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Obsolete Product(s) - Obsolete Product(s)

Table 9. PowerFLAT 5x6 mechanical data

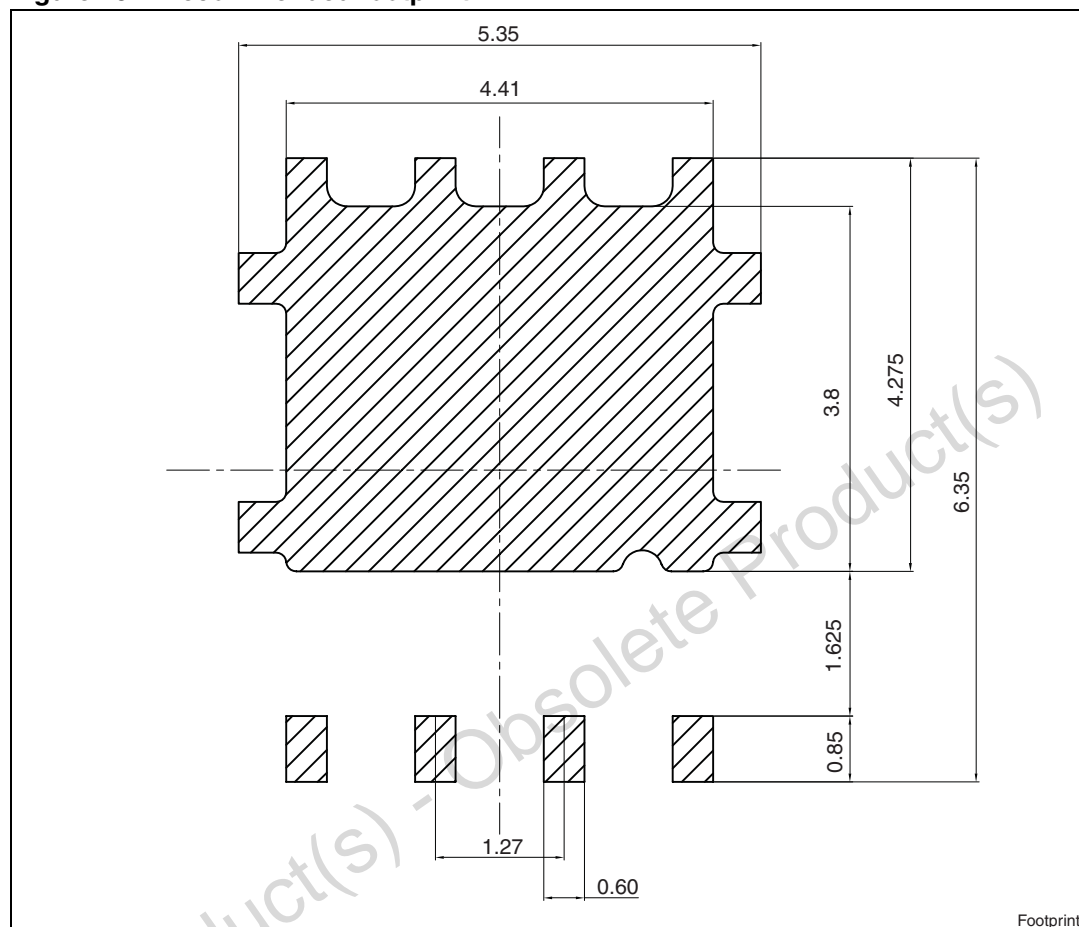
Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D		5.20	
E		6.15	
D2	4.11		4.31
E2	3.50		3.70
e		1.27	
e1		0.65	
L	0.715		1.015
K	1.05		1.35

Figure 19. PowerFLAT 5x6 drawing



8231817_Rev.C

Figure 20. Recommended footprint



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
10-Mar-2011	1	First release.

Obsolete Product(s) - Obsolete Product(s)

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