AN1765
APPLICATION NOTE

LCD MONITOR POWER SUPPLY WITH VIPer53

J. Augustoni - A. Bailly

INTRODUCTION

LCD monitors are replacing aging CRT type in today's desktop PCs. The typical power supply requirement in this application is a 12V rail for the backlight and a 5V rail to supply processing ICs and display drivers. The input voltage is of wide range type (85Vac to 265Vac), as it should suite any voltage standard.

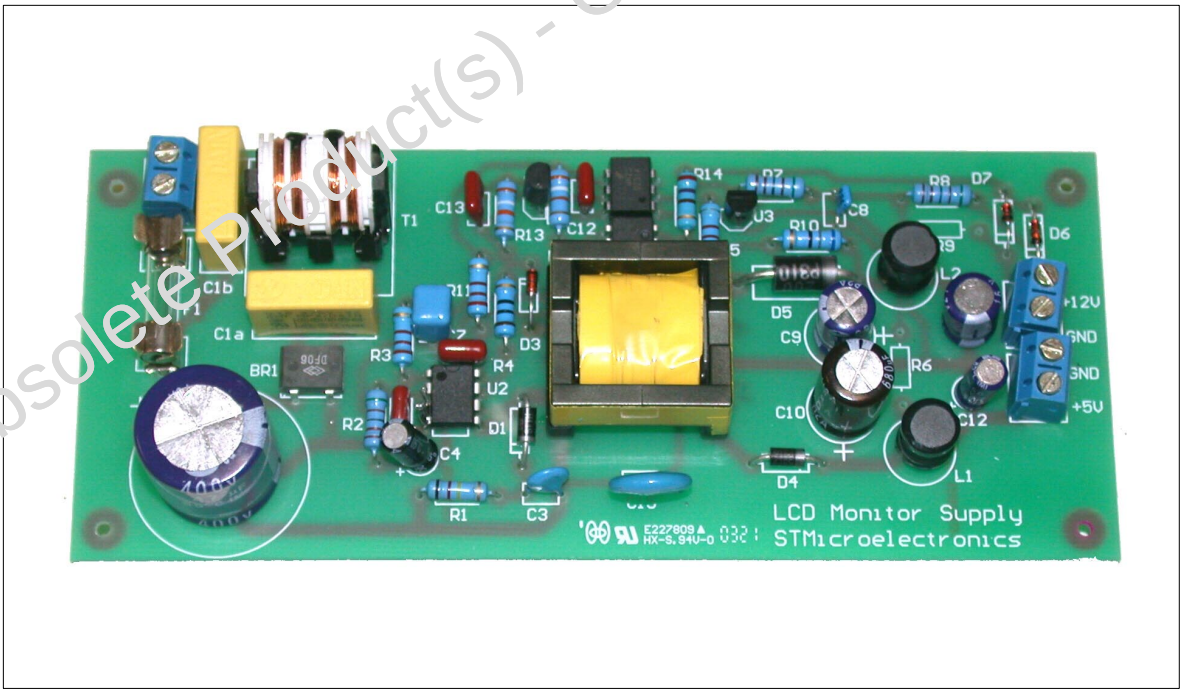
Key features for this application are high efficiency and limited height of the total power supply solution to fit the flat screen monitor package.

The specification can be summarized as shown in table 1.

Table 1: LCD Monitor specification

Screen type	OUTPUT 1 5 V +/- 5%	OUTPUT 2 12 V +/- 10%	Total output power	Efficiency	Board size (L x W x H)
15 " panel	1 A	1.7 A	25 W	> 80 %<	150 x 60 x 20 (mm)
17 " panel	1 A	2.5 A	35 W		

BOARD LAYOUT



1. VIPer53 DESCRIPTION

VIPer53, the first multichip device of the VIPer family has been chosen to fulfill the requirements. It features very low Rdson of 1Ω allowing to deliver up to 35W in wide range in a standard DIP-8 package without a heatsink, answering the need for higher efficiency and reduced space thanks to a lower power dissipation.

1.1 General features

The block diagram is given in figure 1. An adjustable oscillator drives a current controlled PWM at a fixed switching frequency. The peak drain current is set for each cycle by the voltage present on the COMP pin. The useful range of the COMP pin varies from 0.5V to 4.5V, with a corresponding drain current range from 0A to 2A.

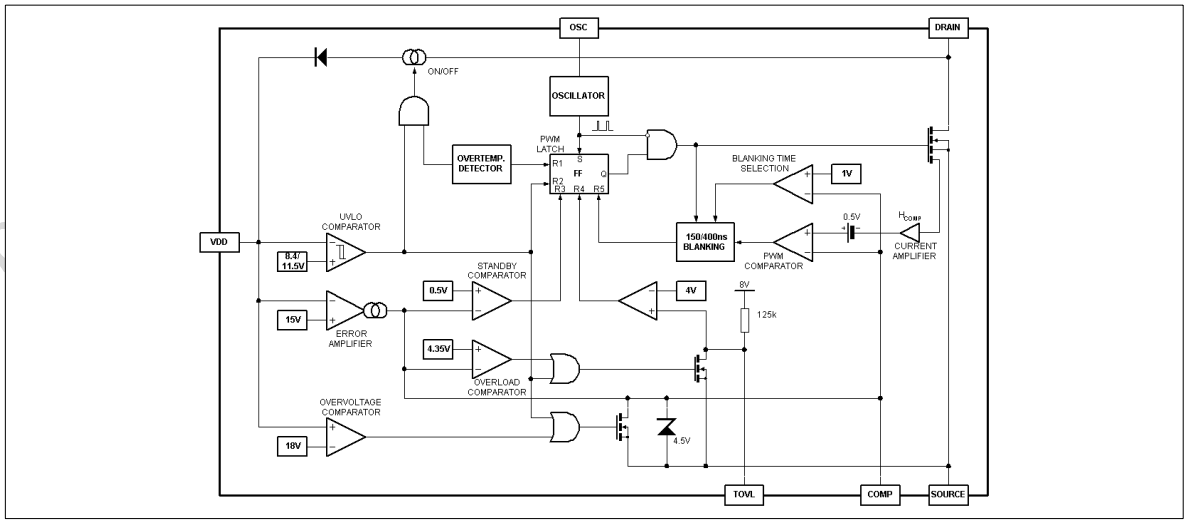
This COMP pin can be either used as an input when working in secondary feedback configuration, or as an output when the internal error amplifier connected to the VDD pin operates in primary feedback to regulate the VDD voltage to 15V.

The VDD undervoltage comparator drives a high voltage startup current source, which is switched off during the normal operation of the device. This feature together with the burst mode capability allows to reach very low level of input power in standby mode, when the converter is lightly loaded.

1.2 Overload protection

A threshold of 4.35V typical has been implemented on the COMP pin. This overload threshold is 150mV below the clamping voltage of 4.5V which corresponds to the current limitation of the device. In case of a COMP voltage exceeding the overload threshold, the pull up resistor on the TOVL pin is released and the external capacitor connected on this pin begins to charge. When reaching a value of 4V typical, the device stops switching and remains in this state until the VDD voltage reaches VDDoff, or resumes normal operation if the COMP voltage returns to a value below the overload threshold. The drain current that the device is able to deliver without triggering the overload threshold is called "current capability", specified as IDmax in the datasheet. This value must be used to size correctly the converter versus its maximum output power.

Figure 1: VIPer53 block diagram



When an overload occurs on secondary side of the converter, the output power is first limited by the current limitation of the device. If this overload lasts for more than a time constant defined by a capacitor connected to the TOVL pin, the device is reset, and a new restarting sequence is initiated by turning on the startup current source. The capacitors on the VDD pin and on the TOVL pin will be defined together in order to insure a correct startup and a low restart duty cycle in overload or short circuit operation. Here are the typical corresponding formulas:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot tss$$

$$C_{VDD} > 8 \cdot 10^{-4} \cdot \left(\frac{1}{D_{RST}} - 1\right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

$$C_{VDD} > \frac{I_{DD1} \cdot tss}{V_{DDhyst}}$$

Where tss and DRST are respectively the time needed for the output voltages to pass from 0V to their nominal values at startup, and the restart duty cycle in overload or short circuit condition. A typical value of 10% is generally set for this last parameter, as it insures that the output diodes and the transformer don't overheat. The other parameters can be found in the datasheet of the device.

As the VDD capacitor has to respect two conditions, the maximum value will be retained to define its value.

1.3 Stand-by operation

On the opposite load configuration, the converter is lightly loaded and the COMP voltage decreases until it reaches the shutdown threshold typically at 0.5V. At this point, the switching is disabled and no more energy is passed on secondary side. So, the output voltage decreases and the regulation loop rises again above the shutdown threshold, thus resuming the normal switching operation. A burst mode with pulse skipping takes place, as long as the output power is below the one corresponding to the minimum turn on of the device. As the COMP voltage works at around 0.5V, the peak drain current is very low (it is actually defined by the minimum turn on time of the device, and by the primary inductance of the transformer) and no audible noise is generated.

In addition, the minimum turn on time depends on the COMP voltage. Below 1V (VCOMPbl), the blanking time increases to 400ns, whereas it is 150ns for higher voltages. The minimum turn on times resulting from these values are respectively 600ns and 350ns, when taking into account the internal propagation time. This feature brings the following benefit:

– This brutal change induces an hysteresis between normal operation and burst mode which is reached sooner when the output power is decreased.
– A short value in normal operation insures a good drain current control in case of short circuit on secondary side.
– A long value in standby operation reinforces the burst mode by skipping more switching cycles, thus decreasing switching losses.

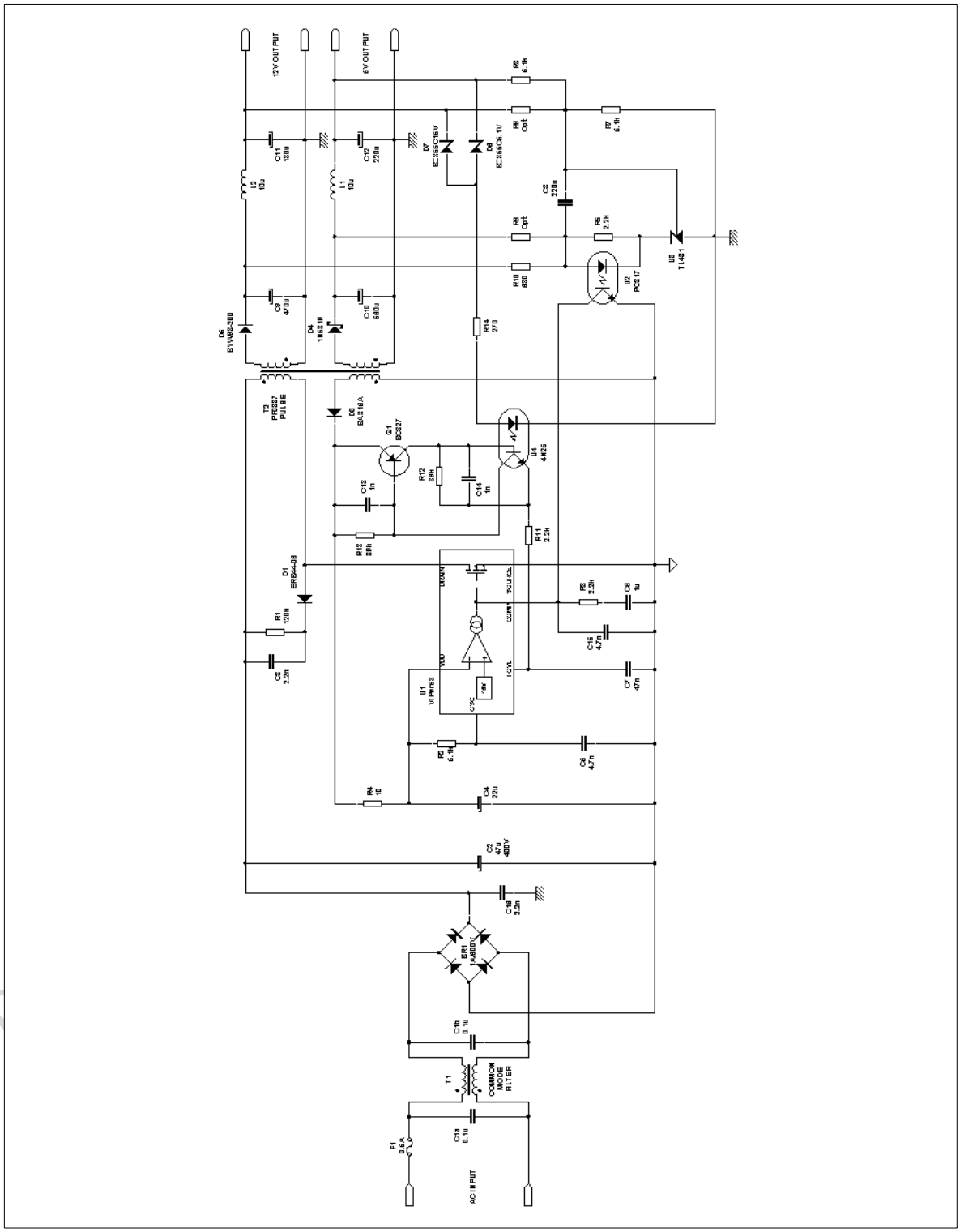
More details regarding the standby operation can be found in the datasheet. The practical results obtained in the corresponding section of this document can also be seen.

2.0 LCD MONITOR POWER SUPPLY

2.1 Schematics

The power topology is an off line flyback with dual output working at a fixed switching frequency of 70kHz. The overall schematics is presented in figure 2.

Figure 2: Schematics



2.1.1 Regulation

The board comes with a regulation based on the 5V output and dynamically coupled to the 12V one in order to insure a good stability, even when the outputs are not loaded simultaneously. The dynamic coupling is made through the connection of the optocoupler U2 to the 12V output.

This configuration allows to meet the specification given on page 1, but it is possible to improve the regulation of the 12V output by implementing a split regulation with an additional resistance R9. In this case, both resistances R9 and R8 must be defined together for suiting particular needs. Suggested values are respectively 33kΩ and 12kΩ.

2.1.2 Overload protection

The transformer primary inductance LP together with the current capability IDmax of the device are used to set the overload point, according to the formula:

$$P_{OVL} = V_{IN} \cdot d \cdot \left(I_{Dmax} - \frac{V_{IN} \cdot d \cdot T}{2 \cdot L_p} \right)$$

This formula is valid only in continuous mode, which will be the case at low line in this application. It gives a minimum value of 480µH for the primary inductance of the transformer with the following numerical parameters:

$$P_{OVL} = \frac{P_{OUT}}{\eta} = \frac{35W}{0.85} \cong 41W$$

$$V_{IN} = 100Vdc$$

$$d = \frac{V_R}{V_{IN} + V_R} = \frac{60}{100 + 60} = 0.38$$

$$I_{Dmax} = 1.6A + t_{don} \cdot \frac{V_{IN}}{L_P} \cong 1.65A$$

$$T = \frac{1}{F_{SW}} = 14\mu s$$

This computation is done at the minimum input voltage, as this leads to the minimum overload triggering point. The continuous operation needed to insure a correct coupling between the two outputs (see the transformer section) makes the overload threshold increase with the input voltage, to reach 67W of output power in the worst case for a VIPer53 with a 2.3A of current capability and an input voltage of 330Vdc. See the corresponding section for practical results.

2.1.3 Overvoltage protection

This application requires a special feature which consists in latching the overvoltage condition, i.e. To definitively shut down the converter when an overvoltage occurs on secondary side. The only way to resume the normal operation is to recycle the input voltage by switching off and on the equipment.

This feature is built around a second optocoupler fed on secondary side by zener diodes on each output. When an overvoltage occurs, the optocoupler conducts some current on primary side and charged up the TOVL capacitor, thus leading to the halt of the converter. Despite the COMP pin voltage is generally low during such an event, and the internal discharging switch on the TOVL pin is turned on as a consequence, it is still possible to make the TOVL voltage rising because of the limited current capability (1mA) and the serial resistance (4kΩ) of the internal TOVL ground switch.

At the same time, this current biases Q1 which in return maintains the on state of the optocoupler, thanks

to the available base connection for the 4N25. So, the overload state lasts until the VDD voltage collapses down to VDDoff, and the startup current source is turned on. The corresponding current is sunk to the TOVL pin which is internally connected to ground during the startup phase, and the device never starts up because the VDD voltage never reaches VDDon. The NPN-PNP structure built around Q1 and U4 can be reset by completely discharging the front bulk capacitor C2. The equipment must be switched off to recover its normal operation.

2.2 Results

2.2.1 Starting current

The overload protection delay has been adjusted to offer a low restarting cycle. As a consequence, the power supply is not able to start with the full load applied on the output. This shouldn't be a problem, as the backlight of the LCD panel starts once the digital section is initialized. The table here below gives the acceptable current on the 12V output at startup, when the 5V one is loaded at its maximum rated current of 1A.

Input voltage	100VDC	200VDC	300VDC
12V current	2.08A	2.89A	3.38A

2.2.2 Overload protection

The 12V output current is increased up to pass into hiccup mode, with a constant current of 1A on the 5V output. The input power and the output current on the 12V output when the protection is triggered are reported in the following table.

Input voltage	100 VDC	200VDC	300VDC
12V current	3.41A	2.89A	3.38A
Input power	49W	54W	60W

Note that these results are well in accordance with the 41W to 67W range of section 2.1.2. Figures 3 to 5 give the corresponding switching cycles just before triggering the overload threshold for an input voltage of respectively 100VDC, 200VDC and 300VDC.

Figure 3: switching cycle at 100VDC

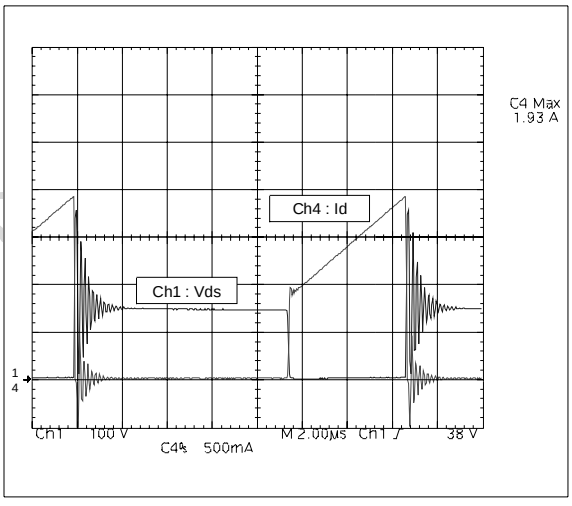


Figure 4: switching cycle at 200VDC

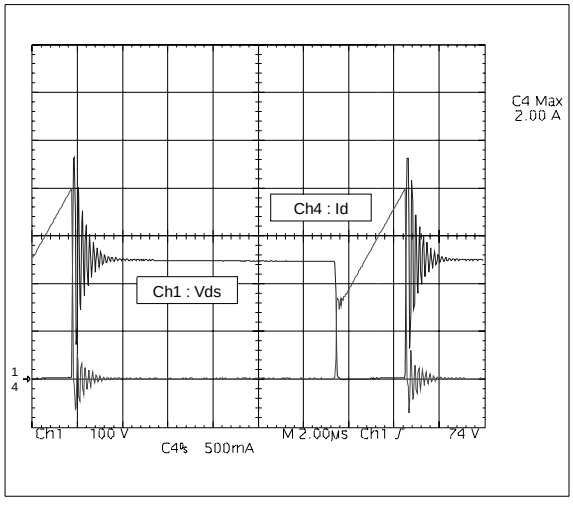


Figure 5: switching cycle at 300VDC

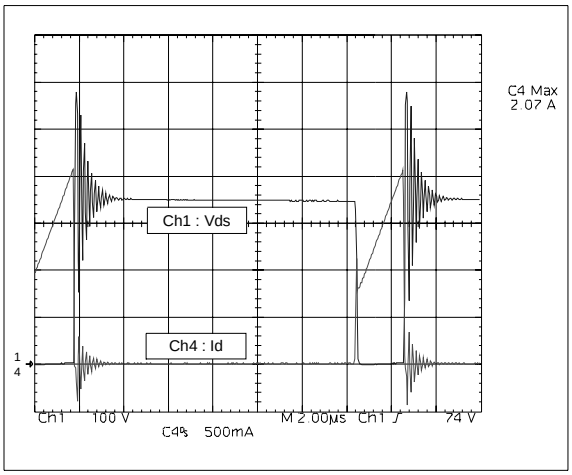
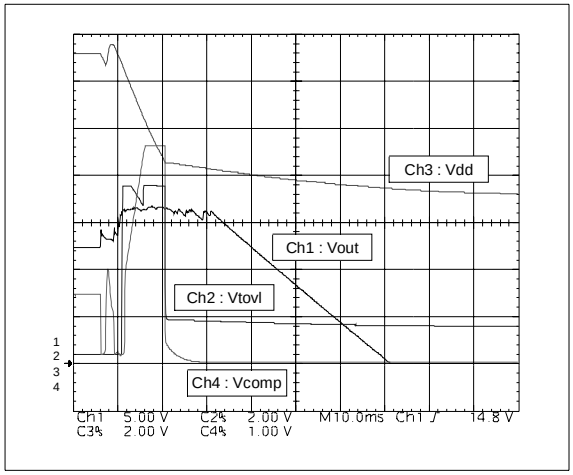


Figure 6: overvoltage event



2.2.3 Overvoltage protection

In order to test the overvoltage protection, an external power supply has been connected on the 12V output. Its voltage is slowly increased, and the converter stops operation when the voltage reaches about 16.1V. Then, the converter remains latched in the off condition, even if the overvoltage is removed. This is shown in figure 6. Note that the input voltage must be recycled (off-on cycle), with sufficient time to discharge the input capacitor C2, in order to restart the power supply.

2.2.4 Short circuit operation

Both outputs are protected against short circuits. During such an event, the COMP voltage is driven high because the optocoupler is completely off, and the overload threshold is over passed. The TOVL capacitor is charged up to the overload triggering point, and the switching is halted. The VDD voltage has to decrease down to VDDoff, and recycle to VDDon before the converter tries to restart. This leads to endless restarting cycles as illustrated in figure 7.

Figure 7: short circuit operation

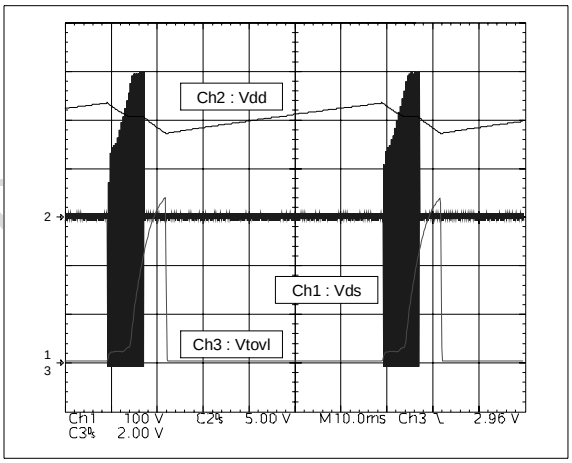
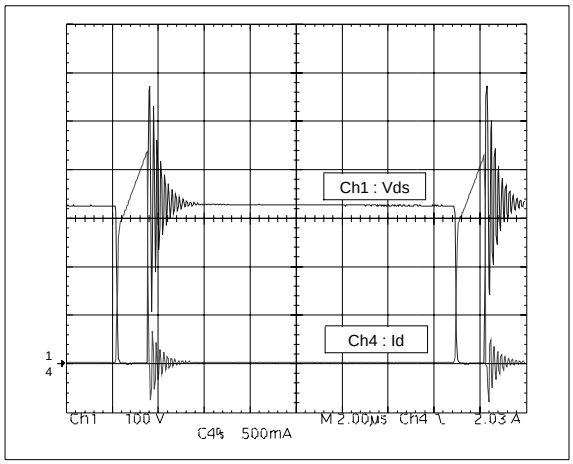


Figure 8: switching cycle in short circuit condition



As the restarting duty cycle is low (about 10%), there is no risk of overheating the output diode or the transformer. So, the short circuit can be applied indefinitely. The converter resumes normal operation when the short circuit is removed. Figure 8 shows a switching cycle in short circuit condition.

2.2.5 Line regulation

The input voltage has been increased from 100VDC to 400VDC with a fixed load on the output (1A for the 5V output, and 1.7A for the 12V one). Both voltages are reported on figure 9.

Figure 9: line regulation at full load (15")

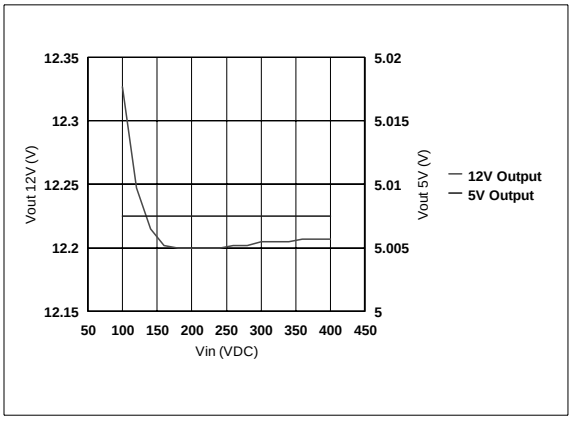
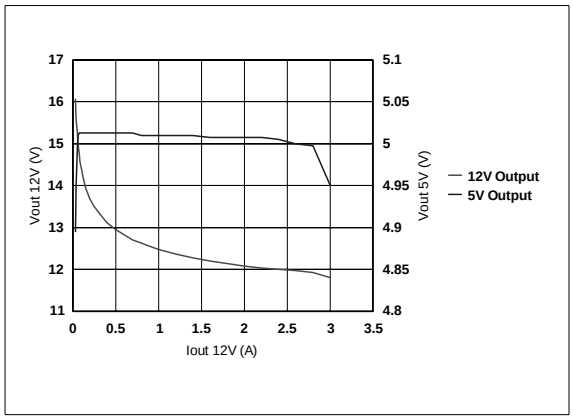


Figure 10: output regulation Vs. 12V current



2.2.6 Load and cross regulation

Figures 10 and 11 present the variation of the output voltages when the output current vary respectively from 32mA to 3A for the 12V output (1A fixed for the 5V output), and from 2.5mA to 1A for the 5V output (1A fixed for the 12V output). The current range on the 12V output is limited for low values by the overvoltage protection which stops the converter when its voltage reaches about 16V. The user will check whether overvoltages are acceptable on the 12V output when its load current is reduced. Eventually, a zener clamper could be used to limit the voltage to about 14V.

Figure 11: output regulation Vs. 5V current

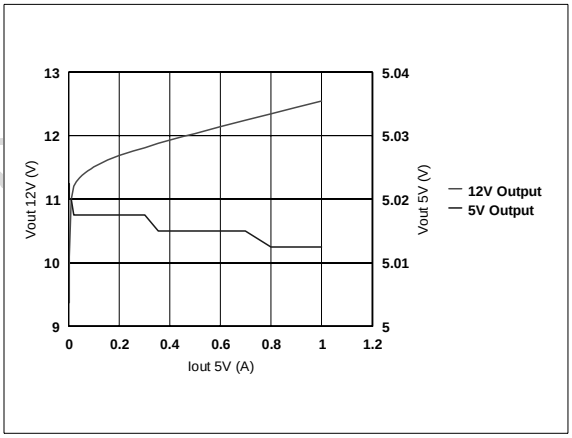
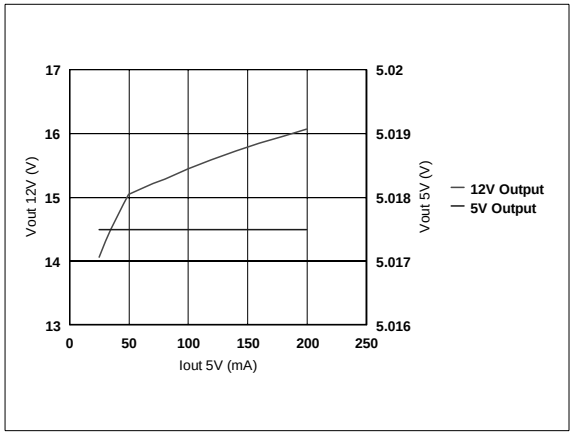


Figure 12: output voltage values in light load operation



2.2.7 Light load operation

No load is applied to the 12V output, and the current on the 5V one varies between 25mA and 200mA. This range is limited for low values by the VDDoff threshold on the VDD pin of the VIPer53 device. When the output current is too low, the auxiliary voltage decreases, and the device cannot be correctly supplied. It stops operation and enters into an endless restarting cycle. For high values, the voltage on the 12V output reaches the overvoltage protection threshold, and the converter is latched in the off mode. Figures 12 to 14 present respectively the output voltage values, the input power consumption and the burst mode operation of the VIPer53 device in this condition.

Figure 13: input consumption in light load operation

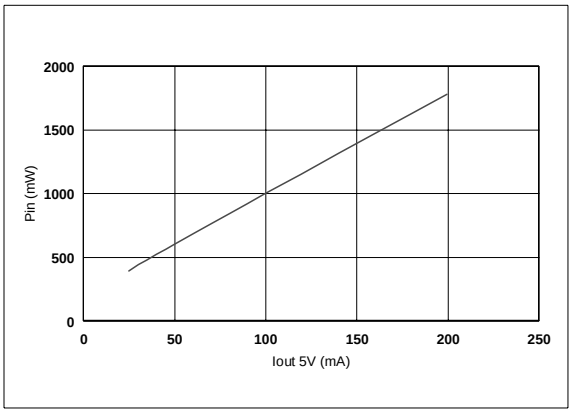
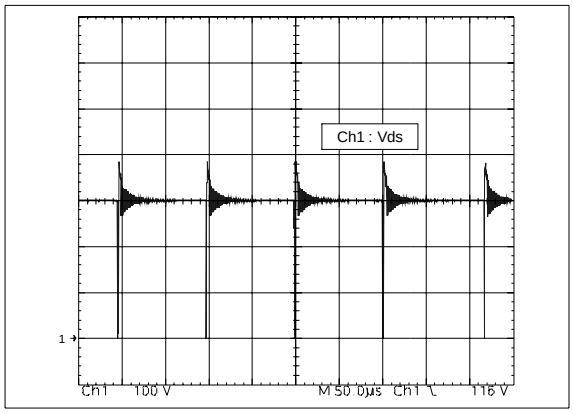


Figure 14: Burst mode on primary side for an output current of 32mA on the 5V output



2.2.8 Efficiency

The efficiency is presented in three configurations:

- The output loads are set to their maximum (15"), that is to say 1A for the 5V output and 1.7A for the 12V one. The input voltage varies between 100VDC and 400VDC.
- The load is fixed to 1A on the 5V output and varies between 32mA and 3A on the 12V one. The limitations in this configuration are the same then for section 2.2.6.
- The load is fixed to 1A on the 12V output and varies between 2.5mA and 1A on the 5V one.

The corresponding results are presented on figures 15 to 17.

Figure 15: efficiency Vs. input voltage

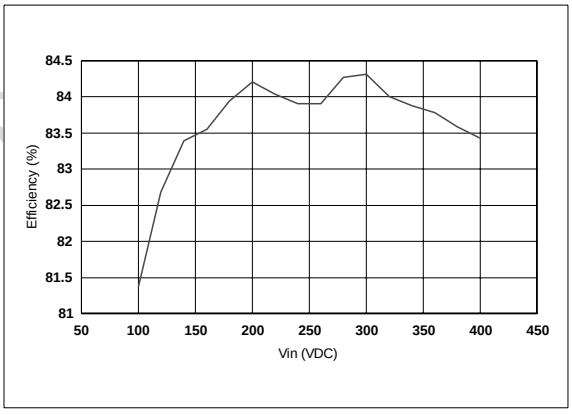


Figure 16: efficiency Vs. 12V output current

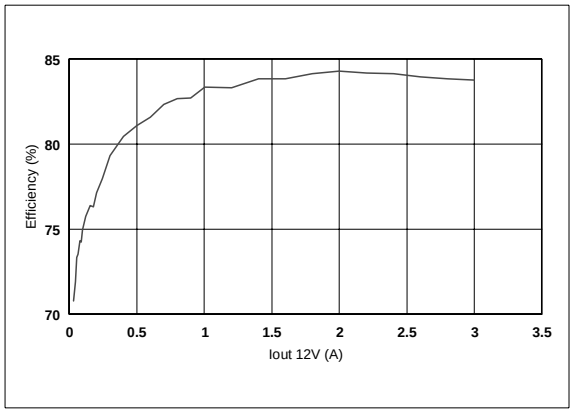
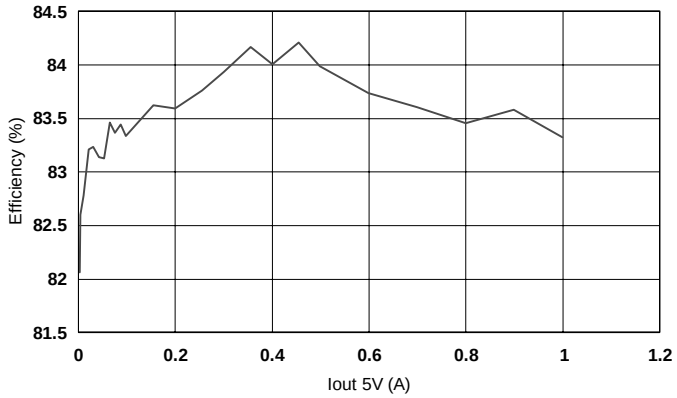


Figure 17: efficiency Vs. 5V output current



2.3 BOARD DESCRIPTION

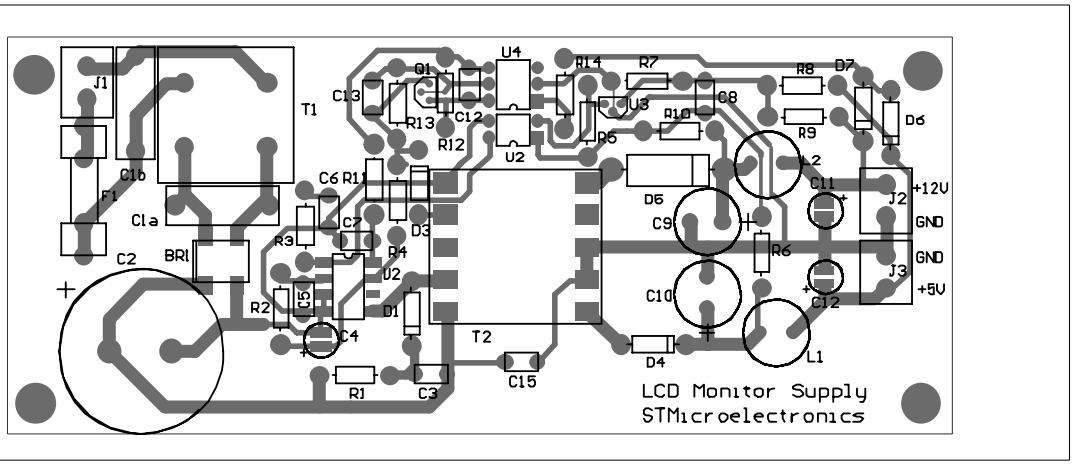
2.3.1 Bill of material

The table here after gives the list of components of the demoboard. The "Opt." ones are not fitted.

Reference	Part value	Description
R1	120kΩ	1/2W resistor
R2	5.1kΩ	1/2W resistor
R3	2.2kΩ	1/2W resistor
R4	10Ω	1/2W resistor
R5	2.2kΩ	1/2W resistor
R6	Opt.	1/2W resistor
R7	5.1kΩ	1/2W resistor
R8	5.1kΩ	1/2W resistor
R9	Opt.	1/2W resistor
R10	680Ω	1/2W resistor
R11	2.2kΩ	1/2W resistor
R12	39kΩ	1/2W resistor
R13	39kΩ	1/2W resistor
R14	270Ω	1/2W resistor
C1a	0.1µF	400V plastic capacitor
C1b	0.1µF	400V plastic capacitor
C2	47µF	400V electrolytic capacitor
C3	2.2nF	200V ceramic capacitor
C4	22µF	35V electrolytic capacitor
C5	4.7nF	Ceramic capacitor
C6	1µF	Ceramic capacitor
C7	47nF	Ceramic capacitor

C8	220nF	Ceramic capacitor
C9	470µF	16V low ESR electrolytic capacitor
C10	560µF	6.3V low ESR electrolytic capacitor
C11	180µF	16V electrolytic capacitor
C12	220µF	10V electrolytic capacitor
C13	1nF	Ceramic capacitor
C14	1nF	Ceramic capacitor
C15	4.7nF	Ceramic capacitor
C16	2.2nF	2.2kV UL/VDE approved capacitor
D1	ERB44-06	
D3	BAX16A	
D4	1N5819	
D5	BYW98-200	
D6	BZX55C5.1V	
D7	BZX55C15V	
Q1	BC327	
BR1	DF04M	Diodes bridge 1A/400V
T1	EH20-0.5-02-18M SCHAFFNER	Common mode choke
T2	PF0337 PULSE	Main transformer
L1	10µH	Drum inductor
L2	10µH	Drum inductor
U1	**VIPer53DIP**	**STMicroelectronics**
U2	PC817	
U3	TL431	
U4	4N25	
F1	0.5A	FUSE

2.3.2 Board layout



C15 is fitted on the solder side of the board.

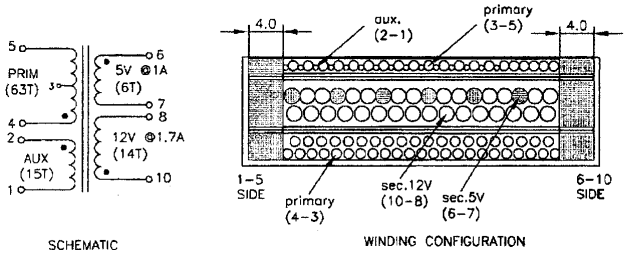
2.3.3 Transformer specification

FINAL OUTLINE NOTES:
ALL DIMENSIONS ARE IN MM.

ELECTRICAL CHARACTERISTICS:
(FOR REFERENCE ONLY. USED FOR CUSTOMER INFORMATION.)

ITEM	SPECIFICATIONS	TEST CONDITIONS	VALUE		UNIT
1	INDUCTANCE PRIM	10KHz-0.1V	±12%	0.48	mH
2	RATIO PRIM / AUX	/	NOM.	4.2	/
3	RATIO PRIM / 5V	/	NOM.	10.5	/
4	RATIO PRIM / 12V	/	NOM.	4.5	/
5	LEAKAGE INDUCTANCE PRIM WITH 5V+12V SHORTED	100KHz-0.1V	MAX.	13*	µH
6	COUPLING CAPACITANCE PRIM TO SEC	100KHz-1V	MAX.	65*	pF
7	RESISTANCE PRIM	/	MAX.	1100	mOhm
8	RESISTANCE AUX	/	MAX.	1300	mOhm
9	RESISTANCE 5V	/	MAX.	46	mOhm
10	RESISTANCE 12V	/	MAX.	52	mOhm
11	HIPOT (PRIM+AUX) TO SEC	60 SECONDS	/	3000	Vac
12	HIPOT PRIM TO SEC	60 SECONDS	/	1000	Vac

* TO BE ACCURATELY DETERMINED LATER



SCHEMATIC

WINDING CONFIGURATION