AN1865
APPLICATION NOTE

SMPS FOR LOW END TV SET WITH VIPer53

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ABSTRACT

In this paper a low cost power supply for 90º TV set (14" to 21") is introduced. The converter uses the new VIPower device VIPer53 in DCM Flyback configuration with either primary or secondary regulation. It provides 60W peak output power on 3 isolated outputs using a DIP-8 package device. The power supply has been specifically developed for European input range.

INTRODUCTION

The VIPer is a family of integrated smart power IC that makes easier size and cost optimization in switch mode power supplies. The devices are based on PWM current mode control and provide integrated high-voltage start-up circuit and protections such as current limiting, thermal shutdown and over/under voltage detection.

VIPer53 represents the latest generation of VIPer family and uses multichip approach in chip to chip fashion to integrate in a single package a PWM controller in VIPower M0 technology and a 620V MDMesh Power MOSFET. It is housed in DIP-8 and PowerSO-10 package for through-hole or SMD mounting. Although the Mosfet is based on the standard MDMesh technology, it features integrated current sense by means of a SenseFET in order to perform current mode control, avoiding the use of an external sensing resistor.

One more feature has been introduced in this last generation: the overload control, by means of a dedicated pin TOVL, which allows to manage the overload event regardless of transformer quality in hiccup mode.

The power supply provides 3 isolated outputs: 105/115V dedicated to the deflection, 13V dedicated to the audio and a 6.5V dedicated to the µP. The first output can be set to either 105V or 115V by means of a jumper in order to properly drive the 14"-21" CRT yokes. A trimmer allows manual adjustment of the output voltage. The feedback is typically taken at primary side, on the auxiliary winding of the transformer, but isolated secondary regulation on the 105/115V output can be arranged on the proposed board by means of optocoupler. Both regulations use TL431 in the feedback loop. The power supply has been specifically developed for European input range, i.e. 185-265Vac.

1. APPLICATION DESCRIPTION AND DESIGN

The proposed power supply has been designed referenced to the specifications listed in Table 1. The switching frequency has been selected considering transformer size, power losses and EMI behaviour, since according to EN55022 standard for conducted emissions the harmonics to be evaluated are in the range from 150kHz to 30MHz.

The target efficiency is higher than 70% with a maximum duty cycle of 45% at minimum input voltage, always in discontinuous conduction mode.

Primary or secondary regulation can be performed and both regulations use TL431 to provide trimmable voltage reference for the 105V/115V output. The other two outputs take advantage of transformer cross regulation by means of optimized winding layout. The 5V output is post-regulated using a standard linear voltage regulator for high accuracy and stability.

The input EMI filter consists in a Pi-filter for both differential and common mode emissions. A standard RCD circuit connected to ground is used to limit dv/dt of the drain voltage for noise issue in the TV set.

Moreover, a light RCD clamper is connected to the drain in conjunction with a peak clamp for the peak voltage management during transient conditions, as shown in the schematic in Figure 3.

The VIPer makes power supply design easier considering start-up, current sensing and no-load issues, improving the overall efficiency and simplifying the circuit. The short circuit protection is provided with hiccup mode and overload is controlled by T_{OVL} pin. However an input 5*20 fuse is used to protect the system against catastrophic failures. The input section also has an NTC to limit the inrush current of the bulk capacitor during the start-up of the power supply.

The switching frequency is set by R5 and C16 according to the diagram given in the datasheet. C13 is the VIPer supply capacitor connected on VDD pin.

Moreover, VIPer53 has a built-in burst mode circuit that allows cycle skipping under low load condition, improving stand-by performance. Such a control has been improved compared to the old VIPer generation using a variable blanking time: 150 or 400 ns.

Table 1: SMPS Specifications

Input voltage	185-265 Vac
Output power (peak)	60W
Outputs	3
Out_1	105V/115V at 450mA; P_1=47.3W, 2%
Out_2	13V at 600mA; P_2=9.1W, 2%
Out_3	6.5V at 80mA; P_3=0.52W, 2%
Switching frequency	50 kHz

1.1 FLYBACK TRANSFORMER

In the considered application the Flyback transformer has 5 windings, since one winding is dedicated to supply the VIPer, as listed in table 2. Winding arrangement is shown in Figure 1, while transformer pin-out and dimension are shown in Figure 1. Due to the presence of 105V/115V output, the reflected voltage has been set to 120V. The transformer is a slot type with ETD34 core, manufactured by TDK. A layer type transformer can be used as well, as shown in Figure 3.

Table 2: SMPS Specifications

Core	ETD34 TDK
Primary inductance Lp	740µH ± 10%63 turns
Leakage inductance	15µH max1.8% Lp
Windings specs	
Output 105V	48 turns
Output 115V	53 turns
Output 13V	6 turns
Output 6.5V	3 turns
Aux	6 turns

Figure 1: Transformer layout

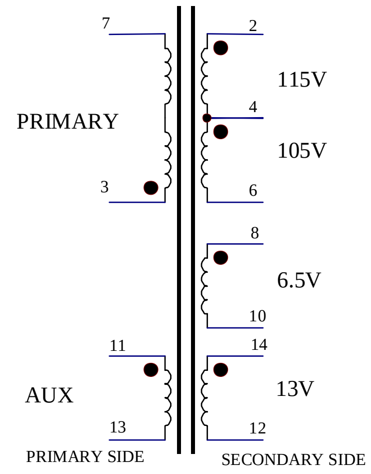


Figure 2: Transformer pin out and dimensions

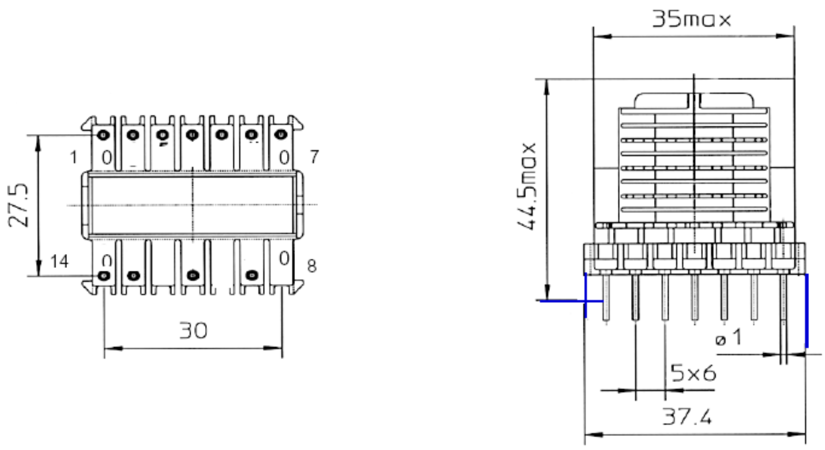
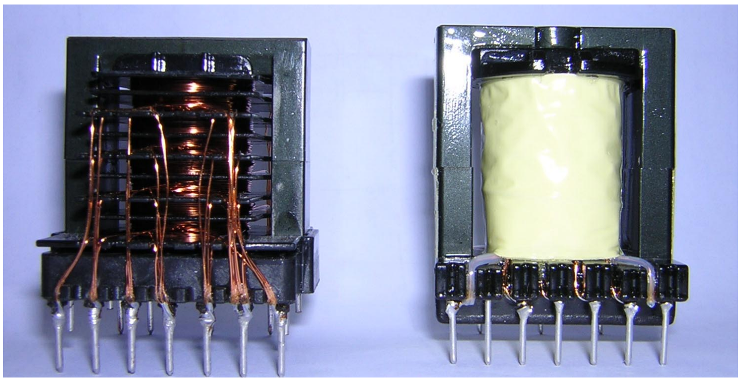


Figure 3: Transformers



1.2 VOLTAGE FEEDBACK

Voltage feedback is realized either in primary or secondary side. Both configurations use TL431 with a trimmer in the voltage divider network to adjust the reference voltage, as shown in figure 5. In primary regulation, the auxiliary winding provides both the supply voltage to the VIPer and the regulation voltage using two separated circuits, by means of two rectifier diodes, as shown in the schematic. In particular, R7 and D6 provide the supply voltage while R21 and D9 provide the regulation voltage. Doing so, it is possible to get good regulation at minimum load, with consequent improvement of the stand-by performance, and to easily provide short circuit protection in hiccup mode.

The board has been developed on a 125x80mm Cu single side 70µm FR-4 frame, as shown in figure 4.

Figure 4: PCB layout

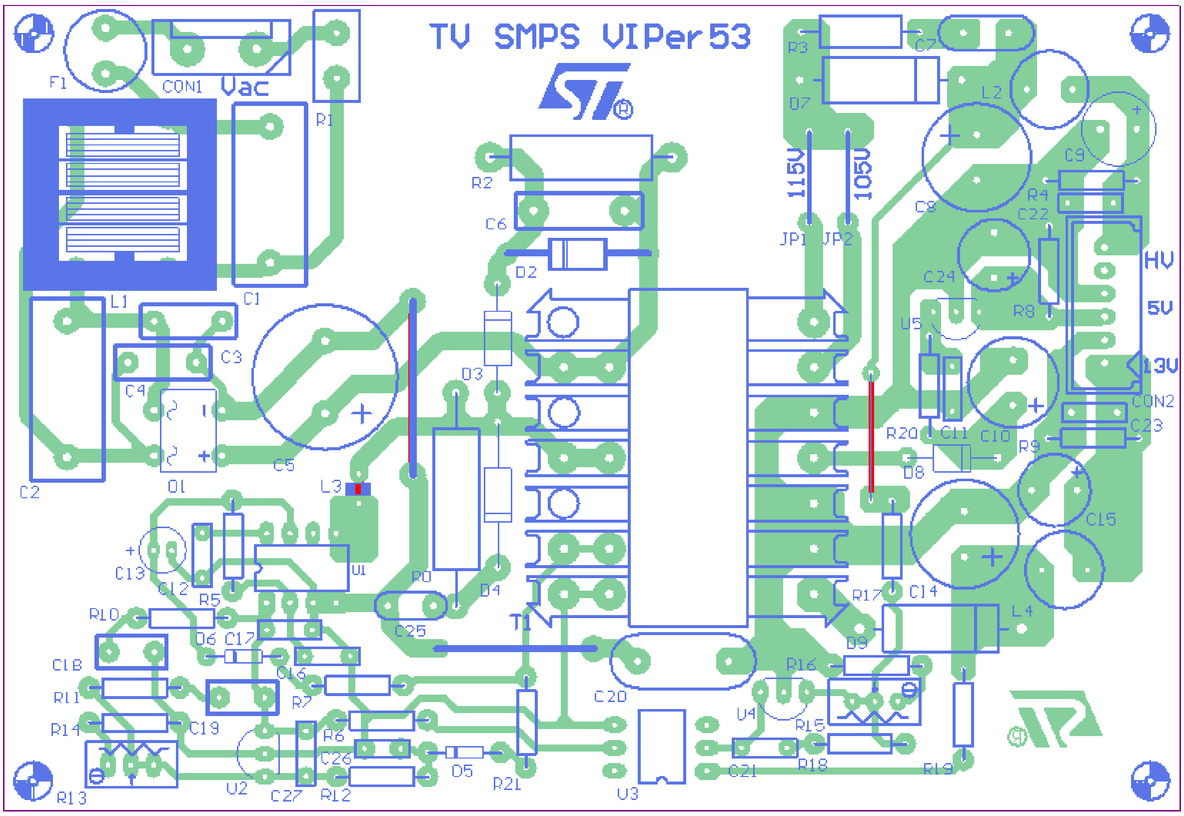


Figure 5: Circuit schematic

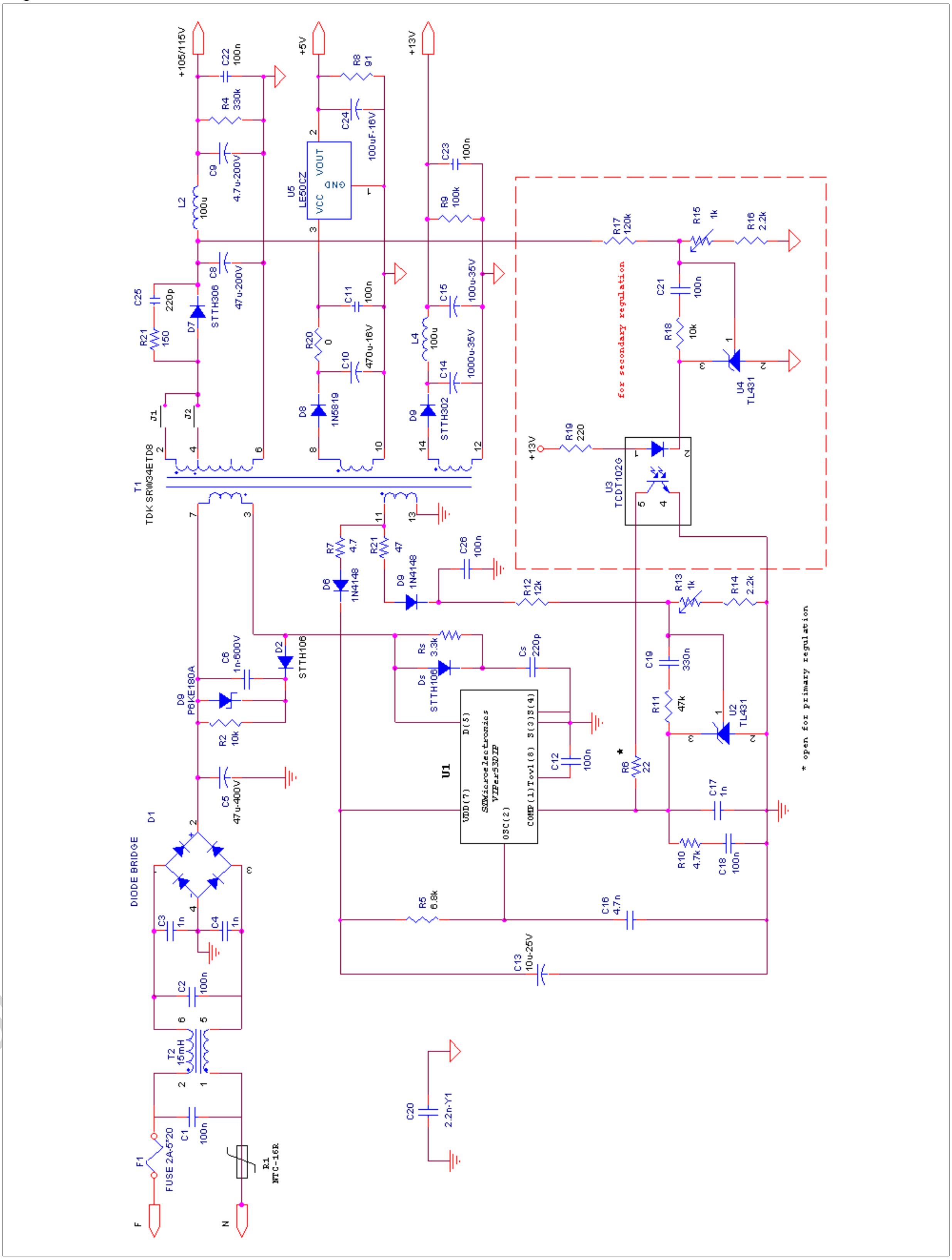


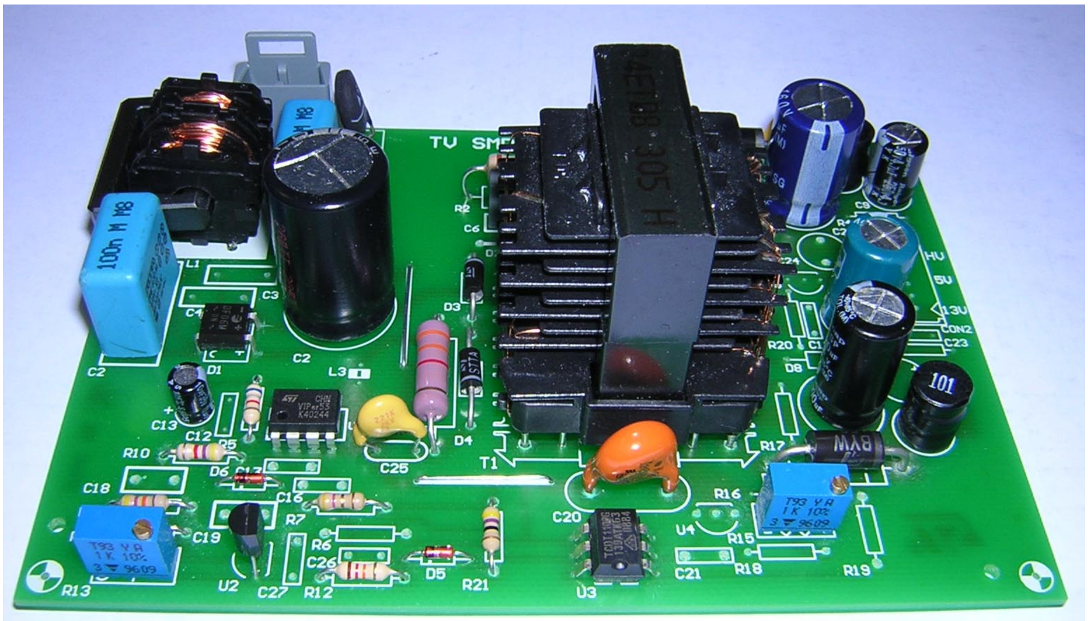
Table 3: Component list

Reference	Description	Note
F1	T2AL250V Fuse 5x20	
R1	NTC	
R2	10KΩ	
R3	3.3KΩ	
R4	330KΩ	
R5	6.8KΩ	
R6	22Ω	For secondary regulation
R7	4.7Ω	
R8	91Ω	Not connected
R9	68KΩ	
R10	4.7KΩ	
R11	47KΩ	
R12	12KΩ	
R13	1KΩ Trimmer	
R14	2.2KΩ	
R15	1KΩ Trimmer	
R16	2.2KΩ	
R17	120KΩ	
R18	10KΩ	
R19	220Ω	
R20	0Ω	
R21	150Ω	
R22	47Ω	
RS	3.3Ω 3W dv/dt Limiter Resistor	
C1	100nF - 250V X2 Capacitor	
C2	100nF - 250V X2 Capacitor	
C3	1nF - 250V	
C4	1nF - 250V	
C5	47µF - 400V	
C6	1nF - 600V	
C7	330nF - 25V	
C8	47µF - 200V	
C9	4.7µF - 200V	
C10	470µF - 25V	
C11	100nF - 25V	
C12	100nF - 25V	
C13	10µF - 25V	
C14	1000µF - 35V	
C15	100µF - 35V	
C16	4.7nF - 25V	
C17	10nF - 25V	
C18	100nF - 25V	
C19	330nF - 25V	
C20	2.2nF - 250V Y1 Capacitor	
C21	100nF - 25V	
C22	100 nF - 200V	
C23	100nF - 25V	

Table 3: Component list (continued)

Reference	Description	Note
C24	100µF - 16V	
C25	220pF	
C26	100nF - 25V	
CS	220pF - 600V dv/dt Limiter Capacitor	
D1	DF06M 1A - 600V	
D2	STTH106	
D3	**STMicroelectronics P6KE180A**	
D4	1N4148	
D5	**STMicroelectronics STTH106**	
D6	**STMicroelectronics 1N5819**	
D7	**STMicroelectronics STTH302**	
DS	**STMicroelectronics STTH106**	
D9	1N4148	
L1	330nH	
T1	TDK SRW34ETD8-E03V0121	Layer
	TDK SRW35EC-T89V017	Slot
T2	15mH S+M B82732	
U1	**STMicroelectronics VIPer53DIP**	
U2	**STMicroelectronics TL431**	
U3	TCDT102G	
U4	**STMicroelectronics TL431**	
U5	**STMicroelectronics LE50CZ**	

Figure 6: Board



2. LAYOUT RECOMMENDATION

Since EMI issues are strongly related to layout, a basic rule has to be considered in high current path routing, i.e. the current loop area has to be minimized. In particular, such a rule has to be applied to the input filter section, the clamper and the dv/dt limiter sections

One more consideration has to be done regarding the ground connection: in fact in order to avoid any noise interference on VIPer logic pins the control ground has to be separated from power the ground. This results in a dedicated track for ground connection of C12, C13, C16, C17, C18, U2 anode and U3 collector.

3. EXPERIMENTAL RESULTS

3.1 - PERFORMANCES AND TYPICAL WAVEFORMS

The performances of the power supply have been evaluated only using primary regulation, in terms of voltage regulation and power consumption. The board can also be configured for secondary regulation, even if this is not typical for such a TV set. Finally typical waveforms are shown.

In Table 4 and 5 the main experimental results on 14" and 21" chassis are listed. The converter features excellent voltage regulation as the input voltage changes, with low power consumption at no load and efficiency as high as 87% at full load. In Figure 7 the drain voltage V_{DS} at no-load and different input voltage V_{in} is shown; the automatic burst mode management is evident. In Figure 8 the drain voltage V_{DS} at full load is shown at 185VAC and 265VAC input voltage, respectively, in order to evaluate the maximum duty cycle and the maximum drain voltage under nominal operation. In Figure 9 V_{DS} and V_{DD} during start-up at 230VAC and typical load are shown, while in Figure 10 V_{DS} and V_{out3} during start-up 265VAC with stand-by load and full load are shown, respectively. Thanks to the internal current generator, which provides constant current, the start up time is independent of the input voltage and only depends on the V_{DD} capacitor value.

In Figure 11 the dynamic load regulation is shown as a step load variation is applied on the audio and both audio and video output, respectively.

Table 4: TV chassis typical consumptions

		14"				21"			
		V	mA	P_{out}	P_{in}	V	mA	P_{out}	P_{in}
V1	**H. Deflection**	100.3	274	34.4W	42W	105.6	380	49W	57W
V2	**μP and logic**	7.7	230			8.3	260		
V3	**Audio**	10.4	500			11.3	600		

These measurements have been performed applying an average video consumption (like an average real TV picture) and maximum audio output driven by a sinewave signal at 3KHz.

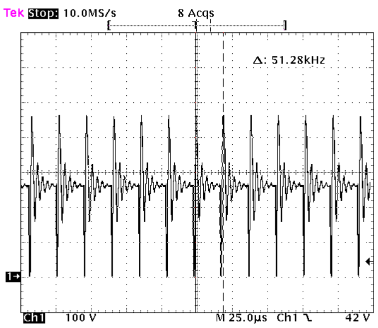
In order to allow the normal operation of the TV chassis a slight modification is required: as the output voltage V2 drops from 8.3V to 6V, the standard linear regulator on the chassis is changed with an LDO type.

The same set of test has been performed on boards with both kinds of transformers, i.e. slot and layer type. As shown in Table 5 the power supply performances are similar with both transformers, the picture stability (screen modulation) due to the audio load variation is good too. The two kinds of transformers can be used on the same board assuring the same performance: the only difference related to the transformer construction is the use of a small RC snubber across D7 using the slot transformer because of the minimum 20% margin required by the diode VRRM, since it damps the voltage ringing across the diode. Such an adjustment has led to lower dv/dt value of the drain voltage, as shown in Figure 12, and consequently to lower radiated noise level which has its importance in the case of low antenna signal (typical for portable TV set).

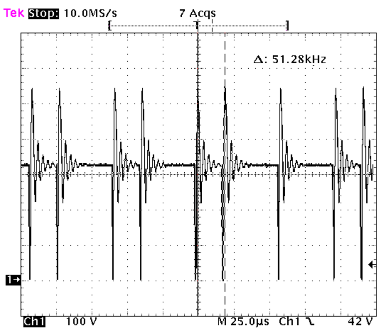
Table 5: Power measurements with 21” TV chassis in normal operation at 230V_{ac}

Normal operation at 230V_{AC}						
		V	mA	P_{in}	P_{out}	Efficiency
SLOT	V1	105.4	380	56.47	49.3	87.3%
	V2	6.24	262			
	V3	12.5	610			
LAYER	V1	103.9	378	55.34	48.47	87.6%
	V2	6.16	265			
	V3	12.62	600			

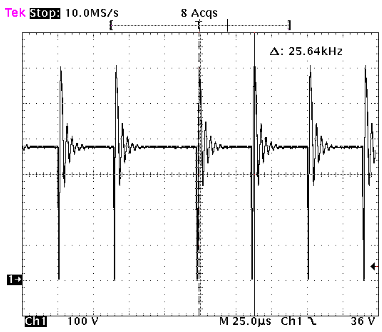
Figure 7: V_{DS} at no load



V_{in}=185VAC

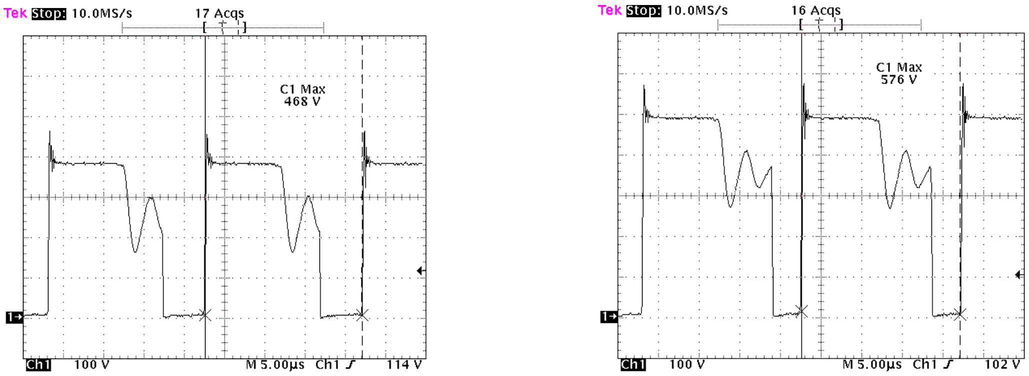


V_{in}=230VAC



V_{in}=265VAC

Figure 8: V_{DS} at full load



V_{in}=185VAC

V_{in}=265VAC

Figure 9: V_{DS} and V_{DD} during start-up at 230VAC and typical load

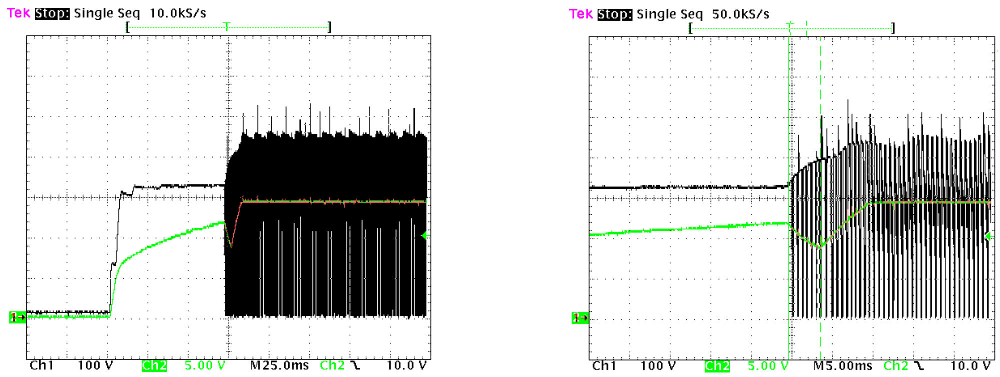


Figure 10: V_{DS} during start-up at 230VAC: stand-by and full load

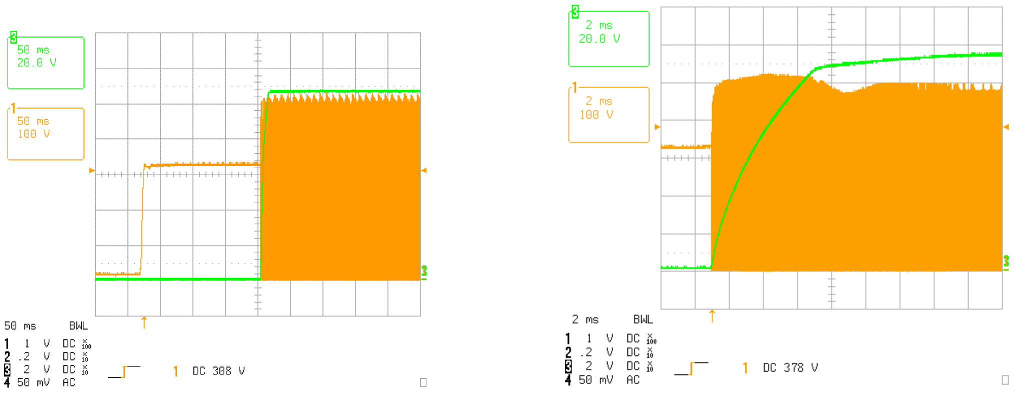
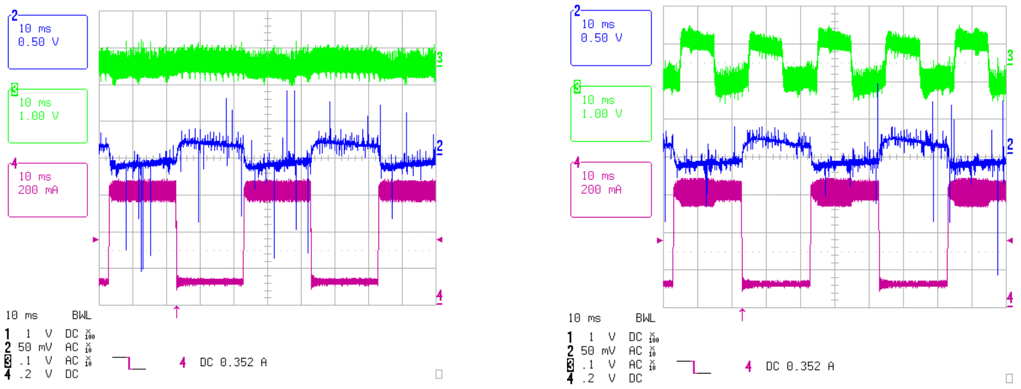


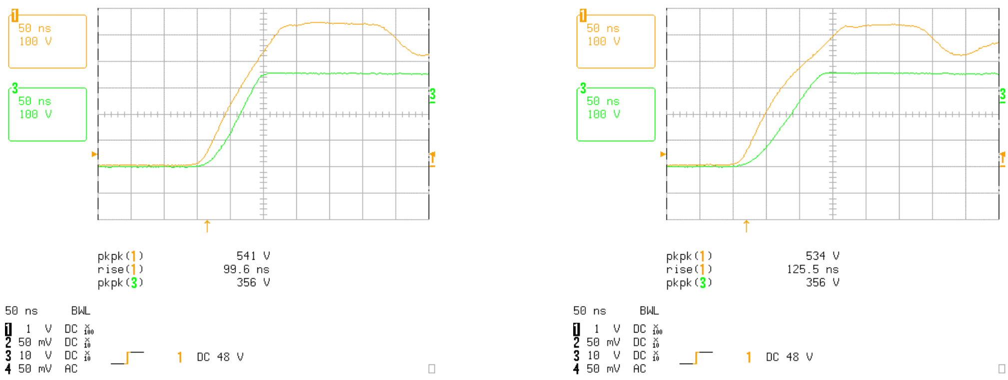
Figure 11: Dynamic load regulation at V_{in}=230VAC



CH2=V_{13V}, CH3=V_{115V}, CH4=I_{13V}=100/600mA, I_{115V}=380mA, I_{5V}=260mA

CH2=V_{13V}, CH3=V_{115V}, CH4=I_{13V}=100/600mA, I_{115V}=200/380mA, I_{5V}=260mA

Figure 12: Drain voltage dv/dt at V_{in}=325VDC and full load, using slot and layer transformers



3.2 STAND-BY PERFORMANCE

Typical waveforms of the circuit with nominal stand-by load have been shown in figure 7. During such a load condition, the power supply operates in burst mode thanks to the internal control circuit of the VIPer53, which allows power consumption saving due to lower switching losses. Inside the burst the maximum switching frequency is the nominal, fixed by the RC connected to OSC pin of the VIPer.

VIPer53 features improve stand-by performance thanks to variable blanking time, which is made longer, i.e 400ns, than the normal mode value, i.e. 150ns, during burst mode. This change is triggered according to COMP pin voltage: if V_{COMP}>1V the blanking time is set to 150ns typical, while it is set to 400ns typical if 0.5V<V_{COMP}<1V. Finally if 0<V_{COMP}<0.5V the device stops switching.

Power consumption measurements have been performed supplying the board by means of a DC source, slightly overestimating the real application consumption since the DC measurements are typically higher than in AC. As a final test on stand-by performance, the transition from stand-by to full load and viceversa have been tested, in order to check the control circuit stability. As shown in figure 13, in spite of a fast change in the current on the high voltage output, both the low voltage output and the auxiliary voltage do not present any unstable behavior, insuring proper operation of the power supply.

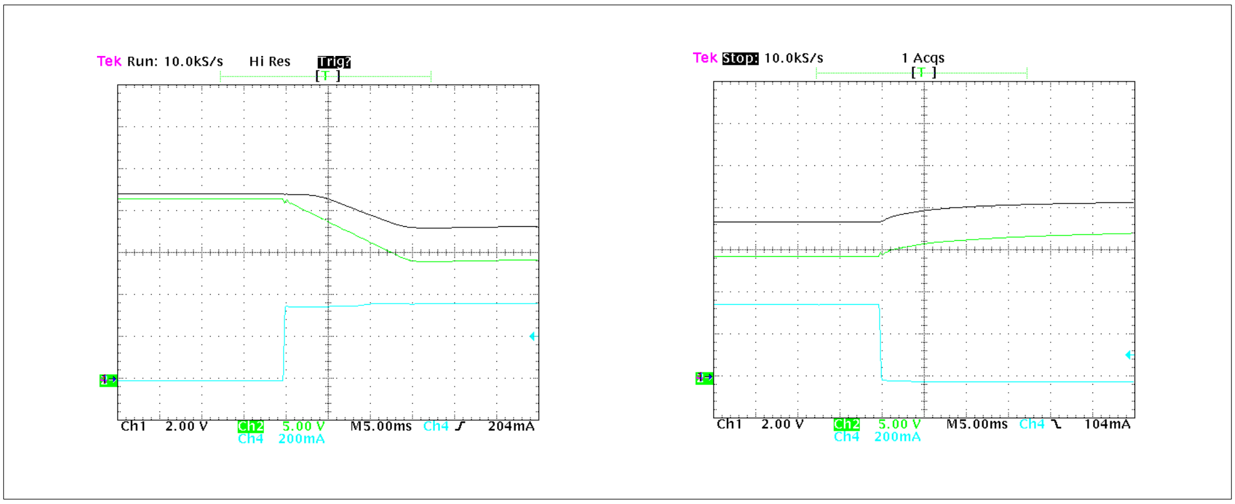
The power consumption during the TV stand-by operation has been measured with both transformers: the measured values are similar using both slot and layer type, as listed in Table 6.

Of course, using secondary regulation the input power consumption would be considerably reduced, since the output voltages will be regulated at lower values.

Table 6: Stand-by measurements

STAND-BY at 230Vac					
		V	mA	Pin [W]	Pout [W]
SLOT	V1	153.8	0	2.4	0.42
	V2	8.4	50		
	V3	18.54	0		
LAYER	V1	153.3	0	2.35	0.41
	V2	8.2	50		
	V3	18.59	0		

Figure 13: Waveforms during stand-by to full load and viceversa transitions at V_{in}=230VAC



3.3 SHORT CIRCUIT BEHAVIOUR

The short circuit behavior has been considered for the three outputs shorting them one by one. Figure 14 shows the VIPer53 typical waveforms behavior during the short circuit. When a short occurs the controller enters hiccup mode, working only for a short period as shown in the figure. This behavior limits the average power dissipation of all the devices, preventing dangerous overheating and catastrophic failures of the SMPS.

VIPer53 features a new integrated overload control circuit, which is implemented on the T_{OVL} pin and does not lie on the transformer coupling quality between output and auxiliary for hiccup mode. In fact, the device monitors the COMP pin voltage and as soon as its value is higher than 4.35V, an internal current source is activated to charge up the T_{OVL} capacitor, until the voltage across this latter pin reaches 4.0V. This is the threshold voltage to stop switching cycle and V_{DD} voltage will decrease below V_{DDoff} value, thus entering hiccup mode with a controlled duty cycle. In any case, if V_{COMP} goes below the OVL threshold, normal operation conditions are resumed. It is important to point out that the maximum value of the peak drain current to consider for design purpose is the I_{DMAX}, called drain current capability, which is the maximum drain current that does not trigger the overload protection and defines the maximum output power that the power supply can deliver.

Some constraints have to be considered for T_{OVL} capacitor design, since the start-up of the power supply do not have to be influenced. The following condition has to be checked regarding T_{OVL} and V_{DD} capacitors:

$$C_{OVL} > 12.5 \cdot 10^{-6} \cdot t_{SS}$$

$$C_{VDD} > 8 \cdot 10^{-4} \cdot \left(\frac{1}{D_{RST}} - 1 \right) \cdot \frac{C_{OVL} \cdot I_{DDch2}}{V_{DDhyst}}$$

$$C_{VDD} > \frac{I_{DD1} \cdot t_{SS}}{V_{DDhyst}}$$

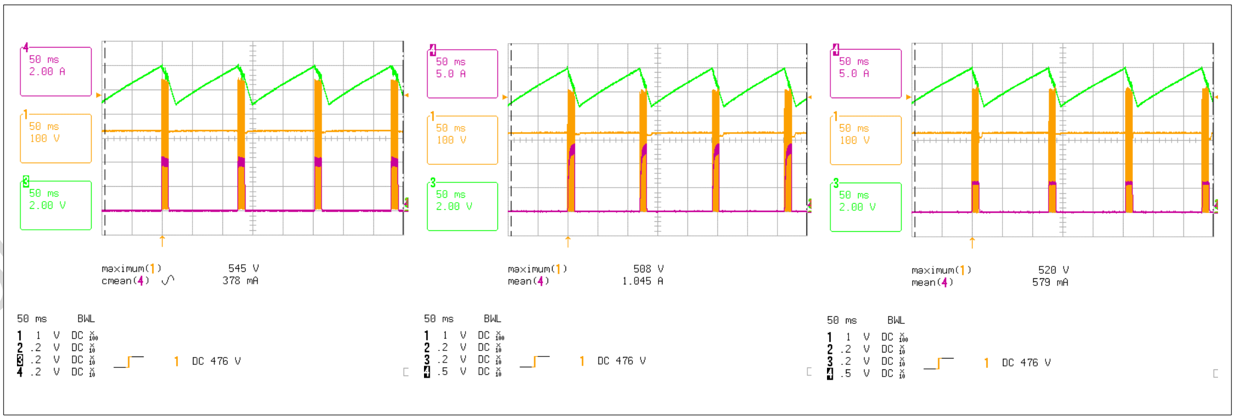
where t_{SS} is the rise time of the output voltage, D_{RST} is the re-start duty cycle under short circuit or overload conditions, I_{DD1} is the operating supply current during switching, I_{DDch2} is the start up charging current for V_{DD} higher than 5V and V_{DDhyst} is the V_{DD} start up threshold. The last 4 parameters are defined in the datasheet.

With such a selection of the two capacitors a proper start up of the power supply is guaranteed and a typical 10% of restart duty cycle is achieved, avoiding overheating of both the transformer and the output diodes and consequently catastrophic failure.

3.4 OPEN LOOP FAILURE

Open loop failure has also been considered as a faulty operation. Under such a condition the device will control the output voltage thanks to the presence of a fast internal error amplifier, which starts working as soon as the V_{DD} voltage reaches 15V. This loop regulates the auxiliary voltage at 15V thus maintaining the deflection voltage below the regulation value and avoiding the X-ray emission by an abnormal EHT voltage applied to the CRT anode.

Figure 14: Typical waveforms during short circuit at V_{in}=230VAC



3.5 EMI MEASUREMENTS

Conducted EMI measurements have been performed according to EN55022 Class B standard, using a 50W LISN and a spectrum analyzer. The quasi peak conducted noise measurements with the power supply connected to the 14" chassis has been performed at full load condition and nominal 230Vac input voltage; the results are shown in figures 15 and 16. The measurements have been taken both on the line (L1) and neutral (L2) conductors. In both conditions the power supply has passed the pre-compliance test on conducted emissions.

Figure 15: L1 and L2 quasi peak measurements V_{IN}=230VAC - 50Hz, with slot transformer

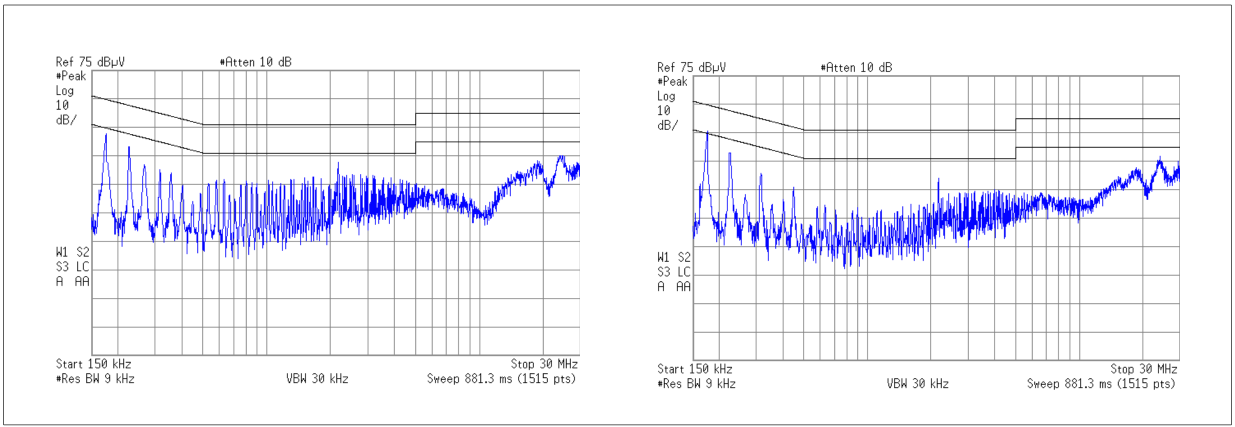
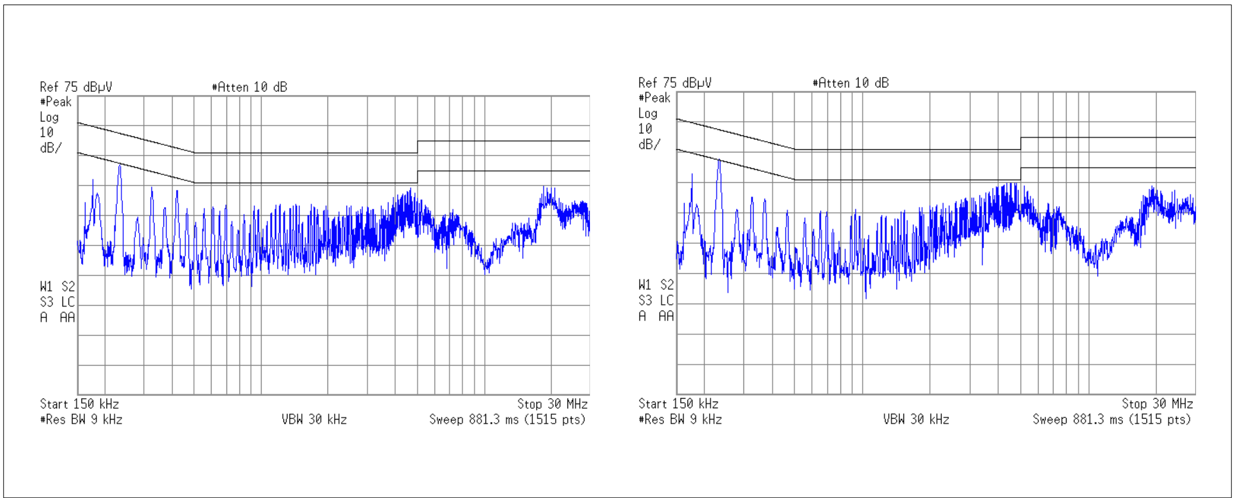


Figure 16: L1 and L2 quasi peak measurements V_{IN}=230VAC - 50Hz, with layer transformer



3.6 THERMAL MEASUREMENTS

Temperature measurements have been performed in order to provide reliable operation condition for all the circuit components. In Table 7the measured values with T_{amb}=23°C are listed. The VIPer53 in DIP-8 package takes advantage of the small copper area connected to the drain pin to act as a heat sink.

Table 7: Main component temperature at full load

Device	T at 230V_{AC}
VIPer53	68
R snubber	65
C snubber	42

D7 (105/115V)	59
D8 (5V)	35
D9 (13V)	43
Transformer	34
Bridge	58

4. CONCLUSIONS

In this paper an SMPS for 90º TV has been introduced and analyzed. Thanks to VIPer53 features the design of the power supply is really straightforward, yielding to a cost effective solution.

The built-in functions and protections of the VIPer53 reduce the external component count, simplifying the overall circuit. Recently introduced features improve both stand-by and overload operations.

Moreover, EMI behavior and thermal performance allow the use of standard components and materials for the PCB, keeping the cost of the whole system low.

The voltage regulation performance confirms the VIPer53 as the device of choice for low cost high performance power supplies as required by the low end TV set market.

For further information please visit STMicroelectronics VIPower web site: *www.st.com/vipower*.