AN2691
Application note

ST10 RPD pin: functionality during reset and Power Down mode

Introduction

RPD is a dedicated timing pin for the return-from-power-down circuit. Additionally, when this pin is recognized low, a reset event is taken as asynchronous. This application note gives advice on configuring the external circuitry connected to the RPD pin in order to make it work properly.

The information contained in this document is valid for ST10F27x and ST10R27x.

1 RPD functionality

RPD is a dual-purpose dedicated pin. This section covers its functionality.

1.1 System reset and startup

Several ST10 reset events that may occur are summarized in the following table:

Table 1. Reset event definition

Reset Source	Flag(1)	RPD Status	Conditions
Power-on reset	PONR	Low	Power-on
Asynchronous hardware reset	LHWR	Low	$t_{\overline{RSTIN}}$ > 500 ns
Synchronous long hardware reset		High	$t_{\overline{RSTIN}}$ > (1032 + 12) TCL + max (4 TCL, 500 ns)
Synchronous short hardware reset	SHWR	High	$t_{\overline{RSTIN}}$ > max (4 TCL, 500 ns) $t_{\overline{RSTIN}}$ ≤(1032 + 12) TCL + max (4 TCL, 500 ns)
Watchdog timer reset	WDTR	(2)	WDT overflow
Software reset	SWR	(2)	SRST instruction execution

1. Flags can be read in the WDTCON register
2. The RPD status has no influence unless bidirectional reset is activated (bit BDRSTEN in SYSCON): RPD low inhibits the bidirectional reset on SW and WDT reset events, that is RSTIN is not activated.

Therefore, roughly, the RPD pin level distinguishes between an asynchronous (low level) and a synchronous reset (high level). The main difference between these two kinds of reset is that the first immediately cancels pending internal hold states and if any, it aborts all internal/external bus cycles whereas in the synchronous reset, after $\overline{RSTIN}$ level is detected, a short duration of a maximum of 12 TCL (six periods of CPU clock) elapses, during which pending internal hold states are cancelled and the current internal access cycle, if any, is completed. For this reason, if an asynchronous reset occurs during a read or write phase in internal memories, the content of the memory itself could be corrupted. To avoid this, synchronous reset usage is strongly recommended.

However, asynchronous reset must be used during the power-on of the device. Depending on crystal or resonator frequency, the on-chip oscillator needs about 1 ms to 10 ms to stabilize with an already stable V_{DD}. The logic of the ST10 does not need a stabilized clock signal to detect an asynchronous reset and is therefore suitable for power-on conditions.

On the contrary, the reset state machine needs a stabilized clock to operate correctly. According to the length of pulse on $\overline{RSTIN}$, the synchronous reset may be recognized as long or short. Long and Short synchronous resets differ by the start-up configuration bits latched:

- Long synchronous reset latches the entire Port0 configuration, including clock frequency selection (P0[15:13])
- Short synchronous reset ignores the bits P0[15:13] and the same clock frequency is applied.

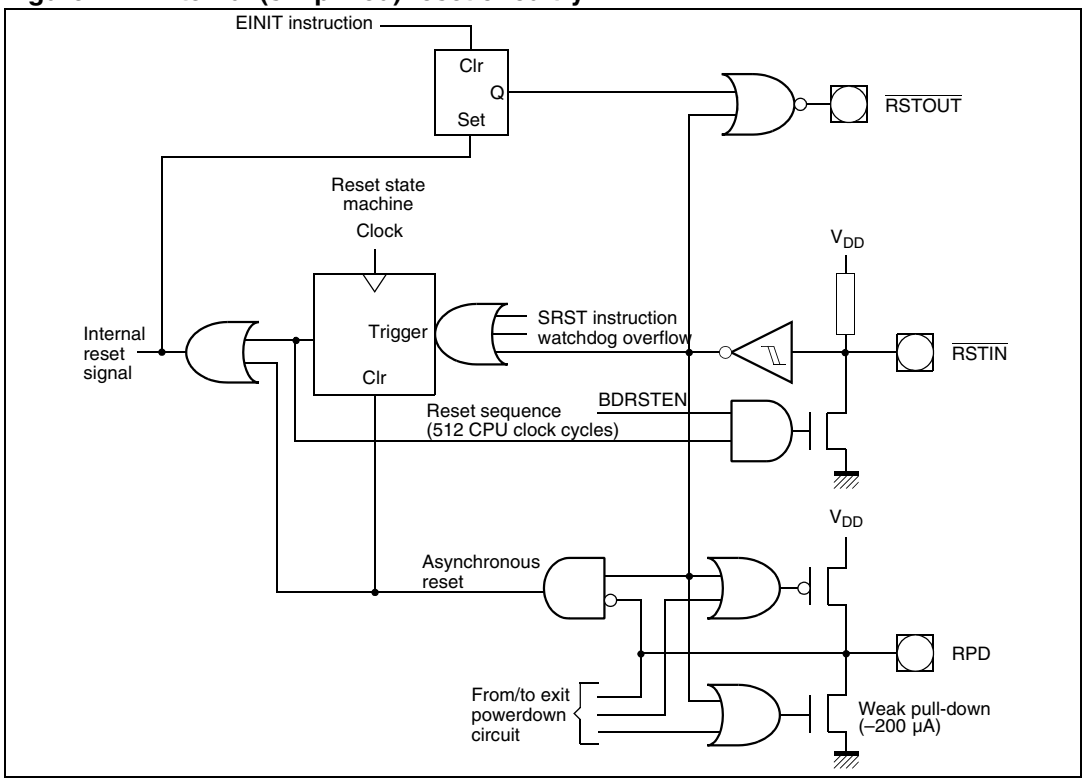
Refer to the product documentation for a full description of the reset mechanism.

The $\overline{\text{RSTIN}}$ pin is an input of the device that can be configured as an output that shows a low level during the internal reset condition. This is called bidirectional reset and is enabled by setting the BDRSTEN bit in the SYSCON register.

When enabled, the open drain of the $\overline{\text{RSTIN}}$ pin is activated, pulling down the reset signal for the duration of the internal reset sequence (synchronous/asynchronous hardware, synchronous software and synchronous watchdog timer resets). At the end of the internal reset sequence (1024 TCL) the pull-down is released.

The figure below shows a simplified reset circuitry scheme. Please refer to the product user manual for more details and timings related to system reset.

Figure 1. Internal (simplified) reset circuitry



1.2 Power down

To reduce power consumption, the microcontroller can be switched to Power Down mode. Clocking of all internal blocks is stopped, the contents of the internal RAM, however, are preserved through the voltage supplied via the V_{DD} pins (and on-chip voltage regulator).

The ST10 provides two different operating Power Down modes:

- Protected Power Down mode
- Interruptible Power Down mode

The Power Down operating mode is selected by the bit PWDCFG in the SYSCON register.

In the first case, the Power Down mode can only be entered if the $\overline{NMI}$ (Non Maskable Interrupt) pin is externally pulled low while the PWRDN instruction is executed and the only way to exit the Power Down mode is with an external hardware reset.

In the second case, the Power Down mode can be entered if enabled Fast External Interrupt pins (EXxIN pins, alternate functions of Port 2 pins, with x = 7...0) are at their inactive level. This inactive level is configured with the EXIxES bit field in the EXICON register, as follows:

EXICON (F1C0H / E0H) ESFR Reset value: 0000H

15 14	13 12	11 10	9 8	7 6	5 4	3 2	1 0
EXI7ES	EXI6ES	EXI5ES	EXI4ES	EXI3ES	EXI2ES	EXI1ES	EXI0ES
RW	RW	RW	RW	RW	RW	RW	RW

EXIxES (x=7...0) External Interrupt x Edge Selection Field (x=7...0)

'00': Fast external interrupts disabled: Standard mode.
EXxIN pin not taken into account for entering/exiting Power Down mode.

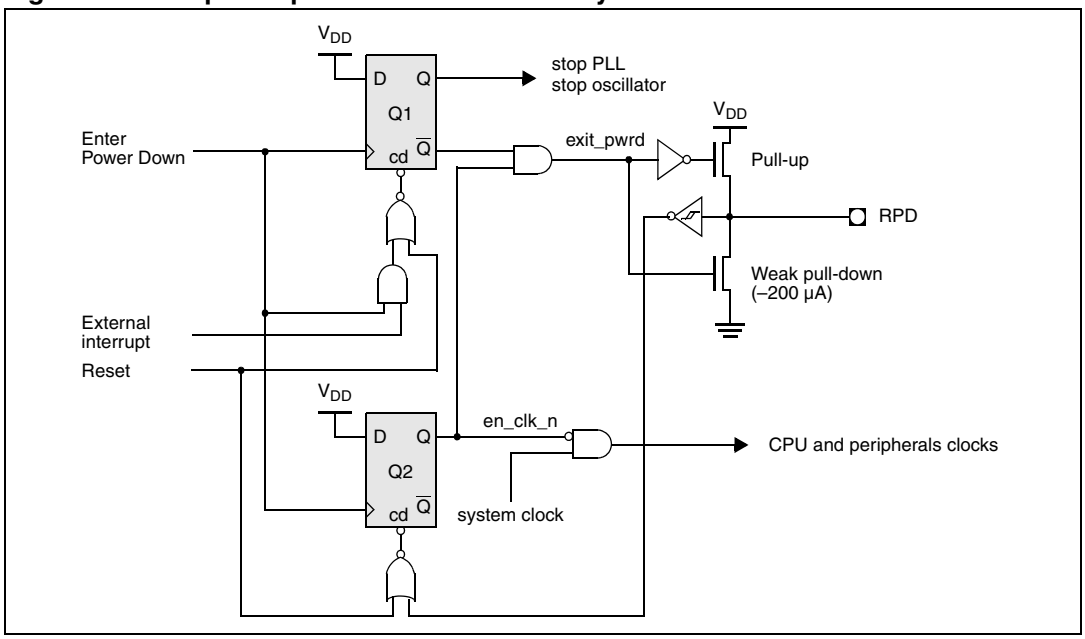
'01': Interrupt on positive edge (rising).
Enter Power Down mode if EX*i*IN = '0', exit if EXxIN = '1' (referred to as 'high' active level)

'10': Interrupt on negative edge (falling).
Enter Power Down mode if EX*i*IN = '1', exit if EXxIN = '0' (referred to as 'low' active level)

'11': Interrupt on any edge (rising or falling).
Always enter Power Down mode, exit if EXxIN level changed.

Interruptible Power Down mode can be exited by asserting either $\overline{RSTIN}$ or one of the enabled EXxIN pins (Fast External Interrupt).

Figure 2. Simplified power down exit circuitry



2 External RPD circuitry examples

To ensure that the two functions explained in the previous chapter work correctly, the external circuitry must be connected to the RPD pin.

2.1 RC network

A simple RC network can be connected to the RPD pin leading to correct behavior during both system reset and return from power down. The cases will be analyzed separately considering that the resistor R and the capacitor C are connected as in *Figure 3*.

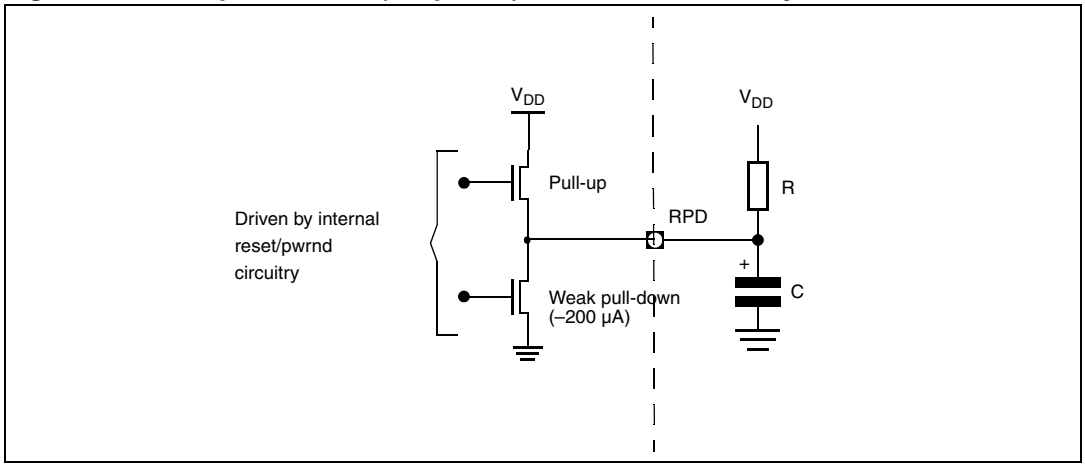
2.1.1 System reset

On power-up, the logical low level on the RPD pin forces an asynchronous hardware reset when $\overline{\text{RSTIN}}$ is asserted low (see *Figure 1*). The external pull-up R will then charge the capacitor C. Note that an internal pull-down device on the RPD pin is turned on when the $\overline{\text{RSTIN}}$ pin is low, and causes the external capacitor (C) to begin discharging at a typical rate of 100 to 200 µA. With this mechanism, after a power-up reset, short low pulses applied on $\overline{\text{RSTIN}}$ produce synchronous hardware reset. If $\overline{\text{RSTIN}}$ is asserted for longer than the time needed for C to be discharged by the internal pull-down device, then the device is forced into an asynchronous reset.

2.1.2 Return from power down

To exit Power Down mode with external interrupt, an EXxIN pin must be asserted for at least 40 ns (x = 7...0). This signal enables the internal main oscillator (if not already running) and PLL circuitry, and also turns on the internal weak pull-down on the RPD pin. The discharging of the external capacitor C provides a delay that allows the oscillator and PLL circuits to stabilize before the internal CPU and peripheral clocks are enabled. When the voltage on the RPD pin drops below the threshold voltage, the CPU and peripheral clocks are enabled and the device resumes code execution (see *Figure 2 on page 5*).

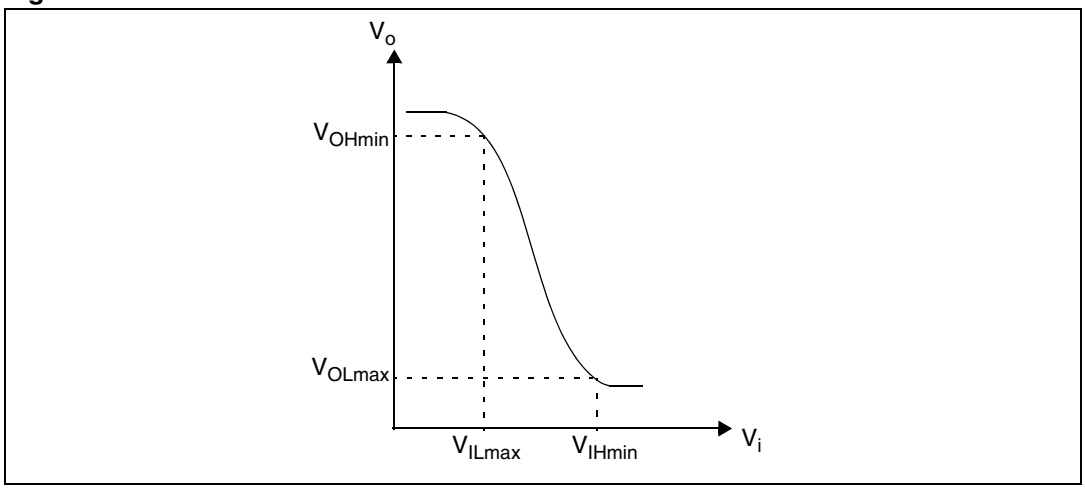
Figure 3. RPD pin: internal (simplified) and external circuitry



2.1.3 RC network sizing

To calculate the external C value, we will suppose that a time T is required to stabilize the oscillator and PLL circuit. Regarding a generic inverter I/O characteristic, the output level V_o of that inverter can be considered high as long as the input level V_i is higher than its V_{IHmin} (see *Figure 4: Generic inverter I/O characteristics*).

Figure 4. Generic inverter I/O characteristics



In the same way, as long as the RPD voltage is higher than V_{IH1}, CPU and peripherals are not fed with any clock (*Figure 2: Simplified power down exit circuitry*). Therefore, the capacitor value must be chosen to maintain the voltage above V_{IH1} for at least the time $T_{restart}$ required by the PLL and oscillator (also the input hysteresis on the RPD pin (V_{HYS4}) must be considered).

Using the simple formula that controls the discharge of capacitor C, we obtain:

$$C = \frac{I_{pulldown} \cdot T_{restart}}{VDD - (V_{IH1} - V_{HYS4})}$$

where $I_{pulldown}$ is the current that flows internally through the weak pull-down.

Supposing V_{DD} = 5 V, since (see product datasheet) V_{IH1} = 3.5 V, $V_{HYS4min}$ = 500 mV, $V_{HYS4max}$ = 1500 mV, $I_{pulldown}$ = 200 µA and $T_{restart}$ = 10.2 ms (crystal oscillator + PLL), it follows that:

$$C = \frac{I_{pulldown} \cdot T_{restart}}{VDD - (V_{IH1} - V_{HYS4min})} = \frac{200 \cdot 10^{-6} \cdot 10,2 \cdot 10^{-3}}{2} \sim 1\ \mu F$$

As during reset a pull-down is activated on the RPD pin, the capacitor C will be discharged. Subsequently the voltage will drop, causing the RPD pin to be seen at a low level. Therefore, an asynchronous reset will be detected.

Table 2. $\overline{\text{RSTIN}}$ pulse length and reset events in the presence of an RC network

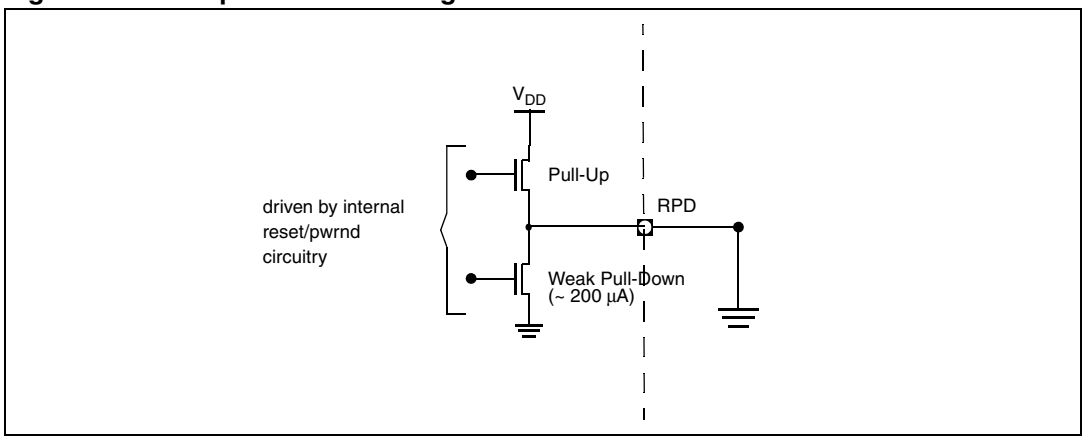
Pulse length	Event
$t_{\overline{RSTIN}}$ <= 500 ns	No effect (filtered)
500 ns < $t_{\overline{RSTIN}}$ < 512 CPU clock cycles	Short synchronous reset
512 CPU clock cycles < $t_{\overline{RSTIN}}$ < 10 ms	Long synchronous reset
$t_{\overline{RSTIN}}$ > 10 ms	Asynchronous reset

The value of the resistor R, instead, is linked to the time needed to charge the capacitor C. Normally 220 kΩ < R < 1 MΩ

2.2 Alternate configuration

If both synchronous reset and interruptible power down modes are not required, it is possible to connect the RPD pin to ground, directly or through a resistance.

Figure 5. RPD pin connected to ground



The internal pull-up is sized to allow a direct connection to ground without any problem to the internal circuitry.

As already explained, with this kind of connection, any pulse longer than 500 ns on the $\overline{\text{RSTIN}}$ pin leads to an asynchronous reset. Moreover, it is not advised to use an interruptible power-down.

3 Revision history

Table 3. Document revision history

Date	Revision	Changes
06-Mar-2008	1	Initial release.