# AN5080
# Application note

## IIS2MDC:
## high-accuracy, ultra-low-power, 3-axis digital output magnetometer

## Introduction

This document is intended to provide usage information and application hints related to ST's IIS2MDC magnetic sensor.

The IIS2MDC is a 3D digital magnetometer system-in-package with a digital I²C and 3-wire SPI serial interface standard output, delivering superior sensing accuracy at ultra-low power.

The device has a magnetic field dynamic range up to ±50 gauss.

The IIS2MDC can be configured to generate an interrupt signal for magnetic field detection and to automatically compensate for hard-iron offsets provided from the higher application layer.

ST software support available for the IIS2MDC includes drivers, a tilt-compensated electronic compass, dynamic magnetometer calibration, and 6-axis or 9-axis sensor fusion.

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# 1 Pin description

**Figure 1. Pin connections**

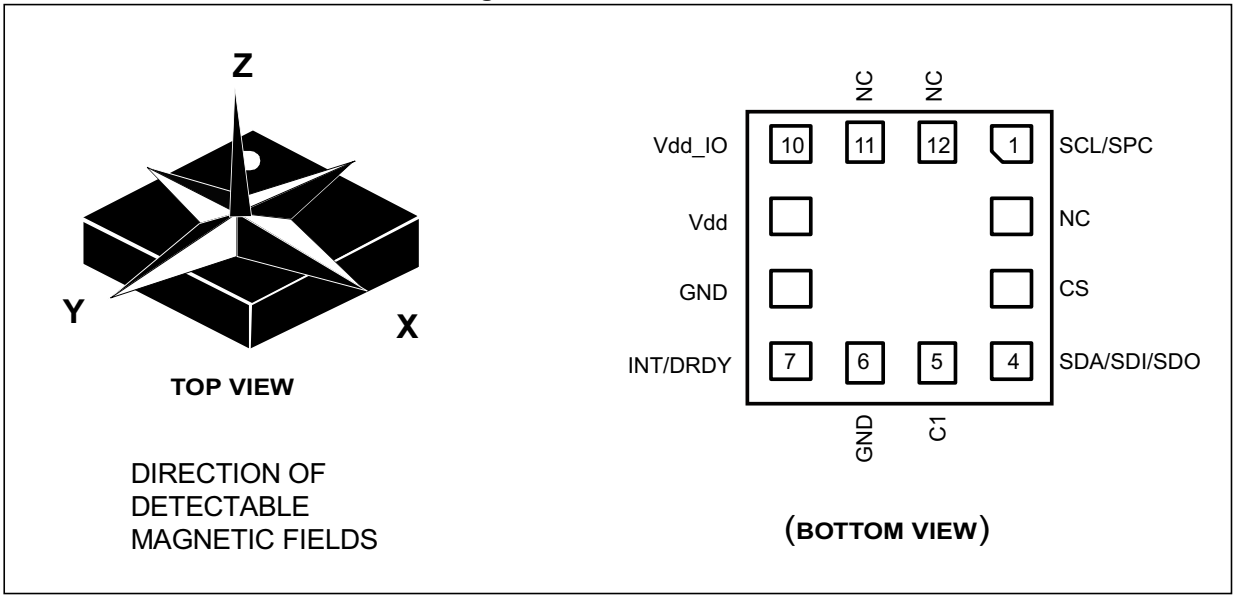



**Table 1. Pin description**

| Pin# | Name | Function | Pin status |
|---|---|---|---|
| 1 | SCL<br>SPC | $I^2C$ serial clock (SCL)<br>SPI serial port clock (SPC) | Default: input without pull-up |
| 2 | NC(1) | | Internally not connected |
| 3 | CS | SPI enable<br>$I^2C$/SPI mode selection<br>1: SPI idle mode / $I^2C$ communication enabled;<br>0: SPI communication mode / $I^2C$ disabled | Default: input without pull-up |
| 4 | SDA<br>SDI<br>SDO | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) | Default: (SDA) input without pull-up |
| 5 | C1 | Capacitor connection (C1 = 220 nF) | External capacitor, voltage forced by the device |
| 6 | GND | 0 V | |
| 7 | INT/DRDY | Interrupt/data-ready signal | Default: output high impedance |
| 8 | GND | 0 V | |
| 9 | Vdd | Power supply | |
| 10 | Vdd_IO | Power supply for I/O pins | |
| 11 | NC(1) | | Internally not connected |
| 12 | NC(1) | | Internally not connected |

1. This pin can be tied to Vdd, Vdd_IO or GND.

## 1.1 INT/DRDY pin configuration

The INT/DRDY pin can be configured to have one HW signal to determine when a new set of measurement data is available for reading or when an interrupt event occurs.

The Zyxda data-ready signal in the STATUS_REG register can be driven to the INT/DRDY pin by setting the DRDY_on_PIN bit in the CFG_REG_C register to 1 (see *Section 6.3: Using the data-ready signal* for further details).

The INT signal in the INT_SOURCE_REG register can be driven to the INT/DRDY pin by setting the INT_on_PIN bit in CFG_REG_C to 1 (see *Section 10: Interrupt generation* for further details).

*Note: Both the* DRDY_on_PIN *and* INT_on_PIN *bits in CFG_REG_C configure the INT/DRDY pin as a digital output, but only one signal (INT or DRDY) can be routed on the INT/DRDY pin. If both bits are asserted, only the INT signal is routed as shown in following table.*

The table below summarizes the INT/DRDY pin status and functionality in different configurations of the DRDY_on_PIN and INT_on_PIN bits of the CFG_REG_C register.

**Table 2. INT/DRDY pin configuration**

| DRDY_on_PIN | INT_on_PIN | INT/DRDY pin status | INT/DRDY pin function |
|---|---|---|---|
| 0 | 0 | High impedance output | None |
| 1 | 0 | Push-pull output | DRDY (Zyxda) signal routed |
| 0 | 1 | Push-pull output | INT signal routed |
| 1 | 1 | Push-pull output | INT signal routed |

# 2 Registers

**Table 3. Registers**

| Register name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| OFFSET_X_REG_L | 45h | Offset_X_7 | Offset_X_6 | Offset_X_5 | Offset_X_4 | Offset_X_3 | Offset_X_2 | Offset_X_1 | Offset_X_0 |
| OFFSET_X_REG_H | 46h | Offset_X_15 | Offset_X_14 | Offset_X_13 | Offset_X_12 | Offset_X_11 | Offset_X_10 | Offset_X_9 | Offset_X_8 |
| OFFSET_Y_REG_L | 47h | Offset_Y_7 | Offset_Y_6 | Offset_Y_5 | Offset_Y_4 | Offset_Y_3 | Offset_Y_2 | Offset_Y_1 | Offset_Y_0 |
| OFFSET_Y_REG_H | 48h | Offset_Y_15 | Offset_Y_14 | Offset_Y_13 | Offset_Y_12 | Offset_Y_11 | Offset_Y_10 | Offset_Y_9 | Offset_Y_8 |
| OFFSET_Z_REG_L | 49h | Offset_Z_7 | Offset_Z_6 | Offset_Z_5 | Offset_Z_4 | Offset_Z_3 | Offset_Z_2 | Offset_Z_1 | Offset_Z_0 |
| OFFSET_Z_REG_H | 4Ah | Offset_Z_15 | Offset_Z_14 | Offset_Z_13 | Offset_Z_12 | Offset_Z_11 | Offset_Z_10 | Offset_Z_9 | Offset_Z_8 |
| WHO_AM_I | 4Fh | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| CFG_REG_A | 60h | COMP_ TEMP_EN | REBOOT | SOFT_RST | LP | ODR1 | ODR0 | MD1 | MD0 |
| CFG_REG_B | 61h | 0 | 0 | 0 | OFF_CANC_ ONE_SHOT | INT_on_ DataOFF | Set_FREQ | OFF_CANC | LPF |
| CFG_REG_C | 62h | 0 | INT_on_PIN | I2C_DIS | BDU | BLE | 0 | Self_test | DRDY_on _PIN |
| INT_CTRL_REG | 63h | XIEN | YIEN | ZIEN | 0 | 0 | IEA | IEL | IEN |
| INT_SOURCE_REG | 64h | P_TH_S_X | P_TH_S_Y | P_TH_S_Z | N_TH_S_X | N_TH_S_Y | N_TH_S_Z | MROI | INT |
| INT_THS_L_REG | 65h | TH7 | TH6 | TH5 | TH4 | TH3 | TH2 | TH1 | TH0 |
| INT_THS_H_REG | 66h | TH15 | TH14 | TH13 | TH12 | TH11 | TH10 | TH9 | TH8 |
| STATUS_REG | 67h | Zyxor | zor | yor | xor | Zyxda | zda | yda | xda |
| OUTX_L_REG | 68h | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OUTX_H_REG | 69h | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| OUTY_L_REG | 6Ah | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OUTY_H_REG | 6Bh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| OUTZ_L_REG | 6Ch | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

Table 3. Registers (continued)

| Register name | Address | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|
| OUTZ_H_REG | 6Dh | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
| TEMP_OUT_L_REG | 6Eh | Temp7 | Temp6 | Temp5 | Temp4 | Temp3 | Temp2 | Temp1 | Temp0 |
| TEMP_OUT_H_REG | 6Fh | Temp15 | Temp14 | Temp13 | Temp12 | Temp11 | Temp10 | Temp9 | Temp8 |

# 3 Operating modes

The IIS2MDC provides three operating modes:

- Idle mode;
- Continuous mode;
- Single mode.

After the power supply is applied, the IIS2MDC performs a 20 ms boot procedure to load the trimming parameters. After the boot is completed, the magnetometer is automatically configured in Idle mode.

The device offers a wide Vdd and Vdd_IO voltage range from 1.71 V to 3.6 V.

In order to avoid potential conflicts, during the power-on sequence it is recommended to set the lines connected to the device IO pins to high-impedance state on the host side. Furthermore, to guarantee proper power-off of the device it is recommended to maintain the duration of the Vdd line to GND for at least 100 µs.

The operating modes of the device can be set through the MD[1:0] bits of CFG_REG_A as shown in table below.

**Table 4. Operative modes**

| MD1 | MD0 | Mode |
|---|---|---|
| 0 | 0 | Continuous mode |
| 0 | 1 | Single mode |
| 1 | 0 | Idle mode |
| 1 | 1 | Idle mode |

In all three operating modes, the typical value of the magnetic dynamic range is 50 gauss which applies when the magnetic field is fully aligned to one of the sensitive axes. In presence of a stray field in the cross-axis direction, the magnetic dynamic range can decrease down to 25 gauss (in the worst case).

## 3.1 Idle mode

When the magnetometer is in Idle mode, almost all internal blocks of the device are switched off to minimize power consumption. Digital interfaces ($I^2C$ and SPI) are still active to allow communication with the device. The content of the configuration registers is preserved and the output data registers are not updated, keeping the last data sampled in memory before going into idle mode.

## 3.2 Continuous mode

Continuous mode can be enabled by writing the MD[1:0] bits to 00 in CFG_REG_A register.

In Continuous mode the device continuously performs measurements and places the result in the output data registers. Either High-Resolution or Low-Power mode can be selected by configuring the LP bit in CFG_REG_A (please refer to *Section 4: Power modes*).

In Continuous mode the output data rate can be selected using the ODR[1:0] bits of CFG_REG_A register as shown in table below.

**Table 5. Output data rate configuration**

| ODR1 | ODR0 | ODR (Hz) |
|---|---|---|
| 0 | 0 | 10 (default) |
| 0 | 1 | 20 |
| 1 | 0 | 50 |
| 1 | 1 | 100 |

## 3.3 Single mode

The IIS2MDC offers Single mode in both High-Resolution and Low-Power modes (please refer to *Section 4: Power modes*).

Single mode configuration allows performing a single acquisition upon request; the acquisition is triggered by writing the MD[1:0] bits to 01 in the CFG_REG_A register. Once the measurement has been performed, the Zyxda, zda, yda, xda bits of the STATUS_REG register are asserted, data are available in the output registers and the IIS2MDC is automatically configured in Idle mode by setting the MD[1:0] bits to 11.

Single mode is independent of the programmed ODR: it depends on the frequency at which the MD[1:0] bits are written by the microcontroller/application processor. Maximum ODR frequency achievable in Single mode is given in the following table and strictly depends on the power mode selected (please refer to *Section 4: Power modes*).

**Table 6. Maximum ODR in single mode**

| Power mode (LP bit of CFG_REG_A register) | Maximum ODR [Hz] |
|---|---|
| High-Resolution (LP = 0) | 100 |
| Low-Power (LP = 1) | 150 |

In Single mode, the typical time needed for the generation of the new data corresponds to the turn-on time indicated in *Table 8: Operating mode and turn-on time*.

# 4 Power modes

The IIS2MDC provides two power modes, operating with the device configured either in Continuous or Single mode:

- High-Resolution mode;
- Low-Power mode.

The device power mode can be selected by configuring the LP bit of CFG_REG_A register: if the LP bit is asserted, the device operates in Low-Power mode, otherwise it operates in High-Resolution mode (default configuration).

In both Low-Power mode and High-Resolution mode, the magnetometer circuitry is periodically turned on/off with a duty cycle that is a function of the selected ODR and data interrupt generation is active.

The difference distinguishing the two modes is in the number of samples used to generate each output sample, which is four times less in Low-Power mode than the number used in High-Resolution mode, thus ensuring a lower power consumption.

The table below summarizes the current consumption of the two power modes with offset cancellation disabled/enabled (the sensor offset cancellation feature can be configured using the OFF_CANC bit of CFG_REG_B register - please refer to *Section 8: Magnetometer offset cancellation*).

**Table 7. Current consumption**

| ODR [Hz] | Current consumption (LP = 0 and OFF_CANC = 0) [uA] | Current consumption (LP = 1 and OFF_CANC = 0) [uA] | Current consumption (LP = 0 and OFF_CANC = 1) [uA] | Current consumption (LP = 1 and OFF_CANC = 1) [uA] |
|---|---|---|---|---|
| 10 | 100 | 25 | 120 | 50 |
| 20 | 200 | 50 | 235 | 100 |
| 50 | 475 | 125 | 575 | 235 |
| 100 | 950 | 250 | 1130 | 460 |

The following table summarizes the turn-on time of the device in the two different power modes with the offset cancellation function enabled or disabled (see *Section 8: Magnetometer offset cancellation*).

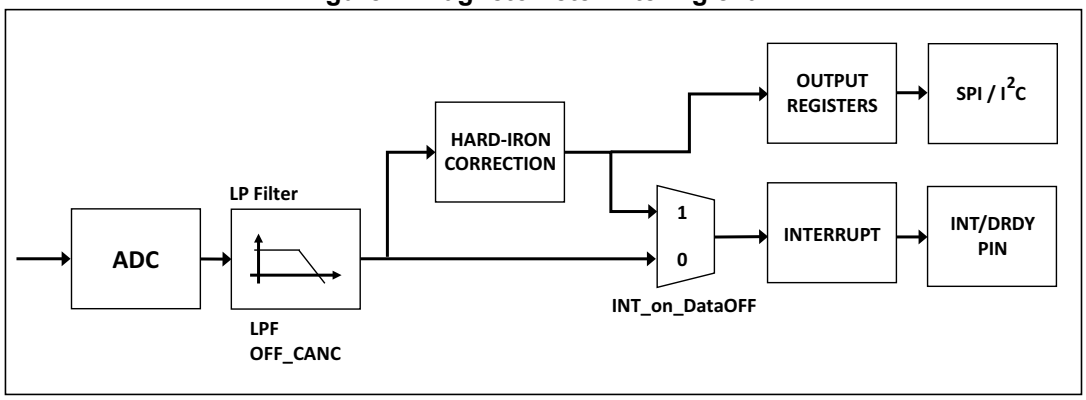
**Table 8. Operating mode and turn-on time**

| Operating mode | Turn-on time | |
|---|---|---|
| CFG_REG_A[LP] | CFG_REG_A[OFF_CANC = 0] | CFG_REG_A[OFF_CANC = 1] |
| 0 (High-Resolution) | 9.4 ms | 9.4 ms + 1/ODR |
| 1 (Low-Power) | 6.4 ms | 6.4 ms + 1/ODR |

# 5 Magnetometer low-pass filter

The IIS2MDC device embeds a digital low-pass filter in order to reduce noise. The filter can be enabled by setting the LPF bit in CFG_REG_B.

**Figure 2. Magnetometer filtering chain**




The table below summarizes the bandwidth and RMS noise values in different device configurations.

When the low-pass filter is enabled, the bandwidth is reduced while noise performance is improved without any increase in power consumption.

*Note: The offset cancellation feature (please refer to Section 8: Magnetometer offset cancellation) works as a two-level moving average filter, thus giving the same bandwidth and noise performance as with the LPF filter enabled.*

**Table 9. RMS noise of operating modes**

| LPF or OFF_CANC | LP = 0 | | LP = 1 | |
|---|---|---|---|---|
| | BW [Hz] | Noise RMS [mg] | BW [Hz] | Noise RMS [mg] |
| 0 (disable) | ODR/2 | 4.5 | ODR/2 | 9 |
| 1 (enable) | ODR/4 | 3 | ODR/4 | 6 |

# 6 Reading output data

## 6.1 Startup sequence

Once the device is powered up, it automatically downloads the calibration coefficients from the embedded flash to the internal registers. When the boot procedure is completed (it takes 20 ms), the magnetometer automatically enters Idle mode.

To turn on the magnetometer and gather magnetic data, it is necessary to select one of the operating modes through the CFG_REG_A register.

The following general-purpose sequence can be used to configure the magnetometer:

1. Write CFG_REG_A = 80h // Temperature compensation enabled // ODR = 10 Hz // Continuous and High-Resolution modes
2. Write CFG_REG_C = 01h // Configure INT/DRDY pin as digital output and route data-ready signal

Writing 81h in CFG_REG_A instead of 80h will set the device to operate in Single mode instead of Continuous mode.

## 6.2 Using the status register

The device is provided with a STATUS_REG register which should be polled to check when a new set of data is available (Zyxda = 1).

The reads should be performed as follows:

1. Read STATUS_REG
2. If Zyxda = 0, then go to 1
3. Read OUTX_L_REG
4. Read OUTX_H_REG
5. Read OUTY_L_REG
6. Read OUTY_H_REG
7. Read OUTZ_L_REG
8. Read OUTZ_H_REG
9. Data processing
10. Go to 1

If the device is configured in Single mode instead of Continuous mode, the routine will be stuck at step 1 after one execution, since the device performs a single measurement, sets the Zyxda bit high and returns to idle mode. Please note that the MD bits return to Idle mode values. It is possible to trigger another single read by setting the MD bits to 01.

## 6.3 Using the data-ready signal

The device can be configured to have one HW signal to determine when a new set of measurement data is available for reading.

The data-ready signal (DRDY) is represented by the Zyxda bit of the STATUS_REG register. This signal can be driven to the INT/DRDY pin by setting the DRDY_on_PIN bit of the CFG_REG_C register to 1.

The data-ready signal rises to 1 when a new set of data has been generated and it is available for reading. The signal gets reset when the higher part of one of the channels has been read (OUTX_H_REG, OUTY_H_REG and OUTZ_H_REG registers).

## 6.4 Using the block data update (BDU) feature

If reading the magnetometer data is particularly slow and cannot be synchronized (or it is not required) with either the Zyxda event bit in the STATUS_REG register or with the data-ready signal driven to the INT/DRDY pin, it is strongly recommended to set the BDU (block data update) bit to 1 in the CFG_REG_C register.

This feature avoids reading values (most significant and least significant parts of output data) related to different samples. In particular, when the BDU is activated, the data registers related to each channel always contain the most recent output data produced by the device, but, in case the read of a given pair (i.e. OUTX_H_REG and OUTX_L_REG, OUTY_H_REG and OUTY_L_REG, OUTZ_H_REG and OUTZ_L_REG) is initiated, the refresh for that pair is blocked until both MSB and LSB parts of the data are read.

*Note: BDU only guarantees that the LSB part and MSB part have been sampled at the same moment. For example, if the reading speed is too slow, X and Y can be read at T1 and Z sampled at T2.*

## 6.5 Understanding output data

The measured magnetic data are sent to the OUTX_H_REG, OUTX_L_REG, OUTY_H_REG, OUTY_L_REG, OUTZ_H_REG, and OUTZ_L_REG registers. These registers contain, respectively, the most significant part and the least significant part of the magnetic signals acting on the X, Y, and Z axes.

The complete output data for the X, Y, Z channels is given by the concatenation OUTX_H_REG & OUTX_L_REG, OUTY_H_REG & OUTY_L_REG, OUTZ_H_REG & OUTZ_L_REG and it is expressed as a two's complement number.

Magnetic data is represented as 16-bit numbers, called LSB. It must be multiplied by the proper sensitivity parameter, M_So = 1.5 mG / LSB, in order to obtain the corresponding value in mG.

### 6.5.1 Example of output data

Hereafter is a simple example of how to use the LSB data and transform it into mG.

Get raw data from the sensor:

```
OUTX_L_REG: 21h
OUTX_H_REG: 00h
OUTY_L_REG: 1Dh
OUTY_H_REG: FFh
OUTZ_L_REG: CBh
OUTZ_H_REG: FEh
```

Do registers concatenation:

```
OUTX_H_REG & OUTX_L_REG: 0021h
OUTY_H_REG & OUTY_L_REG: FF1Dh
OUTZ_H_REG & OUTZ_L_REG: FECBh
```

Calculate signed decimal value (two's complement format):

```
X: +33
Y: -227
Z: -309
```

Apply sensitivity:

```
X: +33 * 1.5 = +49.5 mG
Y: -227 * 1.5 = -340.5 mG
Z: -309 * 1.5 = -463.5 mG
```

### 6.5.2 Big-little endian selection

The IIS2MDC allows swapping the content of the lower and the upper part of the output data registers (i.e. OUTX_H_REG with OUTX_L_REG, and TEMP_OUT_H_REG with TEMP_OUT_L_REG) in order to be compliant with both little-endian and big-endian data representations.

“Little Endian” means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. This mode corresponds to the BLE bit of the CFG_REG_C register set to 0 (default configuration).

On the contrary, “Big Endian” means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address. This mode corresponds to the BLE bit of the CFG_REG_C register set to 1.

# 7 Reboot and software reset

After the device is powered up, the IIS2MDC performs a 20 ms boot procedure to load the trimming parameters. After the boot is completed, the magnetometer is automatically configured in Idle mode.

During the boot time the registers are not accessible.

After power-up, the trimming parameters can be re-loaded by setting the REBOOT bit of the CFG_REG_A register to 1.

No toggle of the device power lines is required; after the reboot is completed, the device enters in Idle mode (regardless of the selected operating mode) after performing one measurement.

If the reset to the default value of the control registers is required, it can be performed by setting the SOFT_RST bit of the CFG_REG_A register to 1. The software reset procedure can take 5 µs; the status of the reset is signaled by the status of the SOFT_RST bit of the CFG_REG_A register: once the reset is completed, this bit is automatically set low.

In order to avoid conflicts, the reboot and the software reset must not be executed at the same time (do not set to 1 at the same time both the REBOOT bit and SOFT_RST bit of the CFG_REG_A register).

The flow must be performed serially as shown in the example below:

1. Set the SOFT_RST bit of the CFG_REG_A register to 1;
2. Wait 5 µs (or wait until the SOFT_RST bit of the CFG_REG_A register returns to 0);
3. Set the REBOOT bit of the CFG_REG_A register to 1;
4. Wait 20 ms.

# 8 Magnetometer offset cancellation

The IIS2MDC is based on AMR technology: a set pulse is needed to set an initial operating condition.

Offset cancellation is the result of performing a set and reset pulse in the magnetic sensor and it can be enabled to remove the intrinsic sensor offset.

The offset cancellation technique is defined as follows:

$$H_{out} = \frac{H_n + H_{n-1}}{2}$$

where $H_n$ and $H_{n-1}$ are two consecutive magnetic field measurements, one after a set pulse, the other after a reset pulse.

Considering a magnetic offset ($H_{off}$), the two magnetic field measurements are:

- Set: $H_n = H + H_{off}$
- Reset: $H_{n-1} = H - H_{off}$

The offset is cancelled according to the offset cancellation technique:

$$H_{out} = \frac{H_n + H_{n-1}}{2} = \frac{2H + H_{off} - H_{off}}{2} = H$$

If the device is operating in Continuous mode, the offset cancellation is enabled by setting the OFF_CANC bit to 1 in CFG_REG_B. In this case, set/reset pulses are continuously performed; a set pulse is applied to one measurement, a reset pulse is applied to the next measurement. If the offset cancellation is disabled (OFF_CANC = 0) and Continuous mode is selected, the set pulse frequency can be configured by setting the Set_FREQ bit in CFG_REG_B. If Set_FREQ is set to 0, the set pulse is released every 63 ODR, otherwise if Set_FREQ is set to 1, the set pulse is released only at power-on from Idle mode (a set of the magnetic sensor is performed anyway, even if the offset cancellation is disabled).

If the device is operating in Single mode, in order to enable the offset cancellation, both OFF_CANC and OFF_CANC_ONE_SHOT bits must be set to 1 in CFG_REG_B. Enabling these bits, the impulse polarity is inverted between a single read and the next one. While offset cancellation is automatically managed by the device in Continuous mode, if this feature is enabled in Single mode, the user has to remove the offset manually using the formula below:

$$H_{out} = \frac{H_n + H_{n-1}}{2}$$

Offset cancellation using single reads is effective only if the reads are close in time, thus ensuring the offset does not drift between two consecutive reads.

# 9 Magnetometer hard-iron compensation

Hard-iron distortion occurs when a magnetic object is placed near the magnetometer and appears as a permanent bias in the sensor's outputs. The hard-iron correction consists of compensating magnetic data from hard-iron distortion.

The operation is defined as follows:

$$H_{out} = H_{read} - H_{HI}$$

where:

- $H_{read}$ is the generic uncompensated magnetic field data, as read by the sensor;
- $H_{HI}$ is the hard-iron distortion field;
- $H_{out}$ is the compensated magnetic data.

The computation of the hard-iron distortion field should be performed by an external processor. After the computation of the hard iron-distortion field has been performed, the measured magnetic data can be compensated.

The device offers the possibility of storing hard-iron data inside six dedicated registers from address 45h to 4Ah.

Each register contains eight bits so that the hard-iron data can be expressed as a 16-bit two's complement number. The OFFSET_X_REG_H, OFFSET_Y_REG_H and OFFSET_Z_REG_H registers should contain the MSBs of the hard-iron distortion field estimated along the X, Y and Z axes respectively. The OFFSET_X_REG_L, OFFSET_Y_REG_L and OFFSET_Z_REG_L registers should contain the LSBs of the hard-iron distortion field estimated along the X, Y and Z axes respectively. Hard-iron data have the same format and sensitivity of the magnetic output data. The hard-iron values stored in dedicated registers are automatically subtracted from the output data.

# 10 Interrupt generation

In the IIS2MDC, the magnetometer interrupt signal generation is based on the comparison between the magnetometer output data and the programmable threshold.

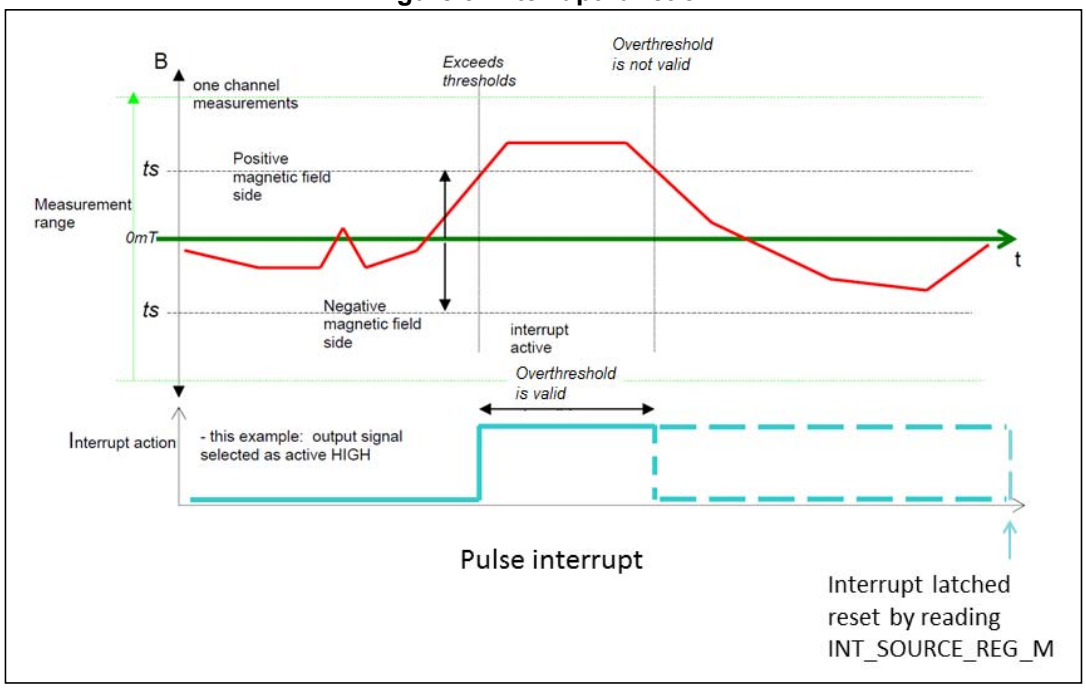
To enable the interrupt function, the IEN bit in INT_CTRL_REG must be set to 1. In the IIS2MDC the interrupt function can be selectively enabled on each axis. In order to do this, the XIEN, YIEN, and ZIEN bits in INT_CTRL_REG need be set properly.

The threshold value can be programmed by setting the INT_THS_L_REG and INT_THS_H_REG registers.

The threshold is expressed in absolute value as a 15-bit unsigned number. The threshold has the same sensitivity as the magnetic data.

When magnetic data exceeds the positive or the negative threshold, an interrupt signal is generated and the INT bit in the INT_SOURCE_REG register goes high. Information about which axis has triggered the wake-up event is also available in the INT_SOURCE_REG register; in particular, when magnetic data exceeds the positive threshold the P_TH_S_[X, Y, Z] bit is set to 1, while if data exceeds the negative threshold the N_TH_S_[X, Y, Z] bit is set to 1. If magnetic data lay between the positive and the negative thresholds, no interrupt signal is generated.

**Figure 3. Interrupt function**




Two different approaches for the interrupt function are available:

- Typical: comparison is between magnetic data read by the sensor and the programmable threshold;
- Advanced: comparison is made between magnetic data after hard-iron correction and the programmable threshold.

These approaches are configurable by setting the INT_on_DataOFF bit in CFG_REG_B.

If INT_on_DataOFF is set to 0, the typical approach is selected, otherwise, if it is set to 1, the advanced approach is selected.

The hardware interrupt signal can be either pulsed or latched:

- Pulsed interrupt signal: it goes to active level when the magnetic data exceeds one of the two thresholds and goes low when the magnetic data are between the two thresholds (positive or negative). This kind of interrupt is selected by setting the IEL bit in INT_CTRL_REG register to 0.
- Latched interrupt signal: it goes to active level when the data exceed one of the two thresholds but is reset only once the source register is read and not when the magnetic data returns between the two thresholds. This kind of interrupt is selected by setting the IEL bit in INT_CTRL_REG register to 1.

The interrupt signal polarity can be set using the IEA bit in INT_CTRL_REG.

If IEA is set to 1, then the interrupt signal is active high, while if it is set to 0, the interrupt signal is active low.

## 10.1 Interrupt configuration example

A basic SW routine for threshold event recognition is given below.

| | |
|---|---|
| 1. Write 80h in CFG_REG_A | // Temperature compensation enabled<br>// ODR = 10 Hz<br>// Continuous mode and High-Resolution |
| 2. Write 40h in CFG_REG_C | // Configure INT/DRDY pin as digital output and route interrupt signal |
| 3. Write 80h in INT_THS_L_REG | // Set a threshold equal to 128 (expressed in LSB) |
| 4. Write E7h in INT_CTRL_REG | // Enable a latched active-high interrupt on the three axes |

The sample code exploits a threshold set to 192 mG (128 LSB * 1.5 mG / LSB) and the event is notified by hardware through the INT/DRDY pin.

## 10.2 Overflow interrupt

The MROI bit in INT_SOURCE_REG alerts the user if a measurement range overflow has occurred at internal ADC level. This function is enabled only if the interrupt generator is active (IEN bit = 1). MROI behavior is always latched: once the internal measurement range overflow has occurred, the MROI bit is reset by reading INT_SOURCE_REG.

# 11 Temperature sensor

The IIS2MDC is provided with an internal temperature sensor.

The temperature sensor has to be enabled by setting the COMP_TEMP_EN bit in CFG_REG_A register to 1.

*Note: For proper operation of the magnetometer sensor, the COMP_TEMP_EN bit must be set to 1 by the user.*

If the device is configured in Continuous mode, the temperature sensor ODR is the same as the ODR of the magnetometer sensor, selected through the ODR[1:0] bits in CFG_REG_A register. Otherwise, if the device is configured in Single mode, the temperature sensor output data is generated upon user request together with the magnetometer sensor output data.

The temperature data is given by the concatenation of the TEMP_OUT_H_REG and TEMP_OUT_L_REG registers and it is represented as a number of 16 bits in two's complement format with a sensitivity of 8 LSB/°C. Typically, the output zero level corresponds to 25 °C.

The IIS2MDC allows swapping, by setting the BLE bit of the CFG_REG_B register to 1, the content of the lower and the upper part of the temperature output data registers.

# 12 Magnetometer self-test

The embedded self-test function allows checking device functionality without moving it. When the magnetometer self-test is enabled, a current is forced into a coil inside the device. This current will generate a magnetic field that will produce a variation of the magnetometer output signals. If the output signals change within the amplitude limits, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

The magnetometer self-test function is off when the Self_test bit of the CFG_REG_C register is disabled; setting the Self_test bit to 1 enables the self-test.

When the magnetometer self-test is activated, the sensor output level is given by the algebraic sum of the signals produced by the magnetic field acting on the sensor and by the current forced.

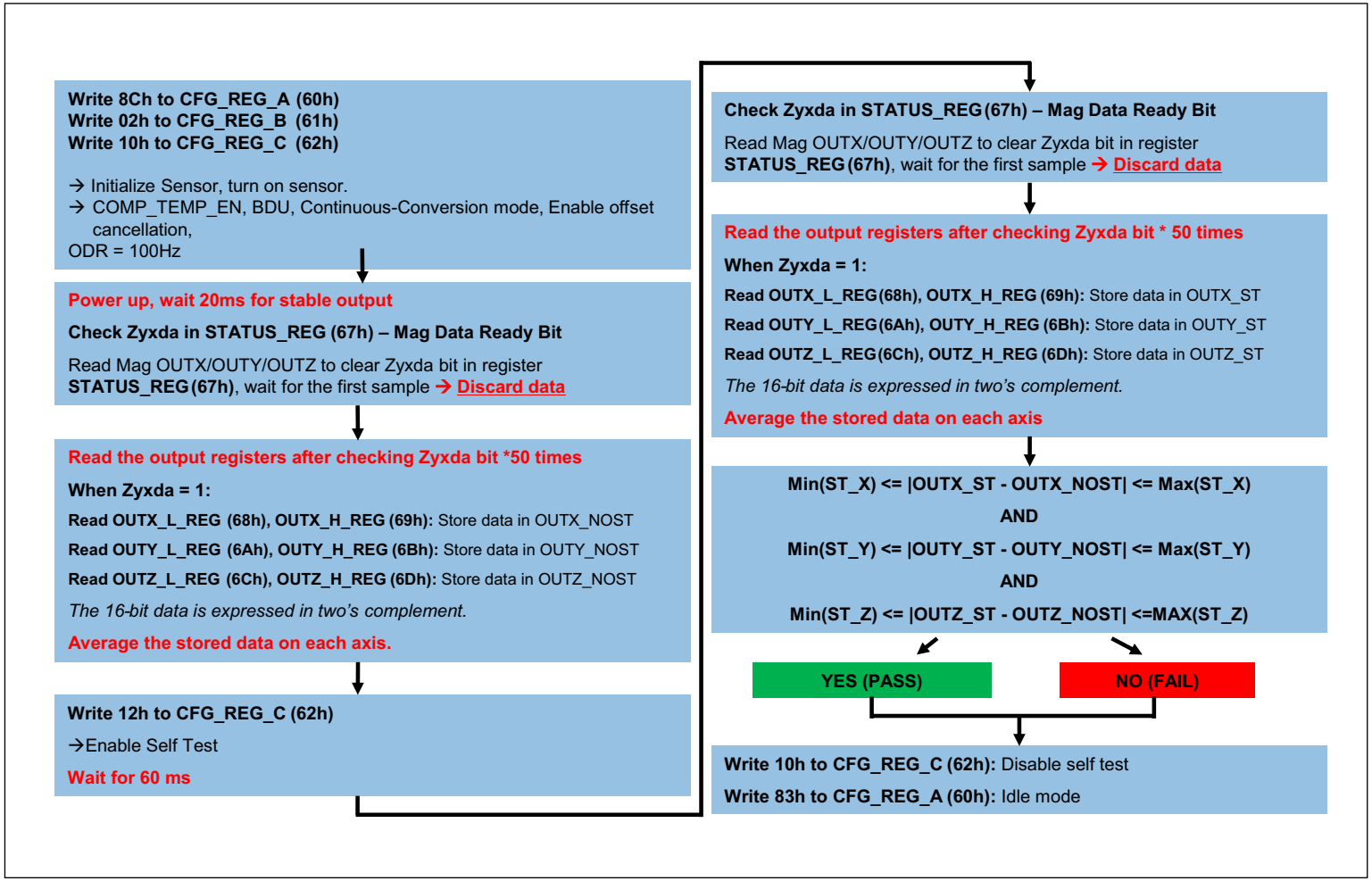
The procedure consists of:

1. enabling the magnetometer;
2. averaging fifty samples before enabling the self-test;
3. averaging fifty samples after enabling the self-test;
4. computing the difference in the module for each axis and verifying that it falls in the given range: the min and max value are provided in the datasheet.

The complete magnetometer self-test procedure is indicated in *Figure 4*.

*Note: Keep the device still during the self-test procedure.*

**Figure 4. Magnetometer self-test procedure**



# 13 Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 26-Sep-2017 | 1 | Initial release |
| 08-Jan-2018 | 2 | Updated *Section 8: Magnetometer offset cancellation* |