AN5113
Application note

MEMS motion sensor: L20G20IS ultra-compact two-axis gyroscope for optical image stabilization

Introduction

The L20G20IS is a two-axis MEMS gyroscope for image stabilization applications. It includes a sensing element and an IC interface capable of providing the measured angular rate to the application through an SPI digital interface.

The unique sensing element is manufactured using a dedicated micromachining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

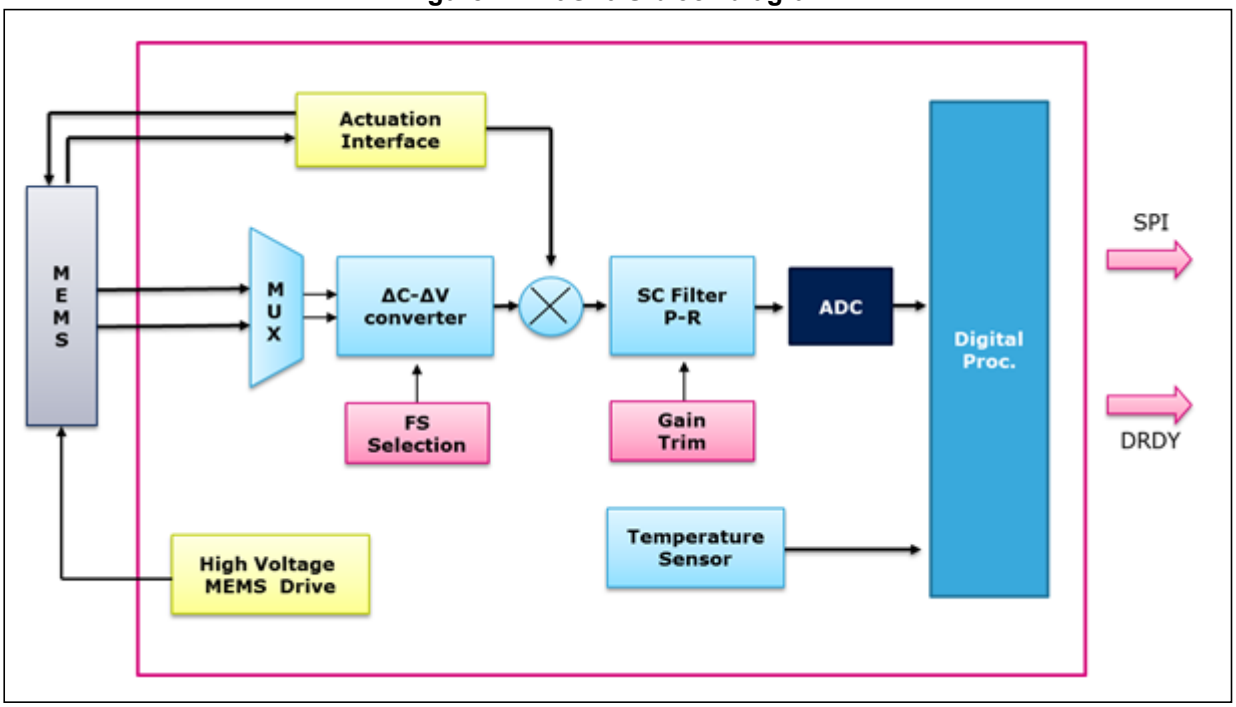
The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The L20G20IS is available in a plastic land grid array (LGA) package and can operate over a temperature range of -40 °C to +85 °C.

Contents

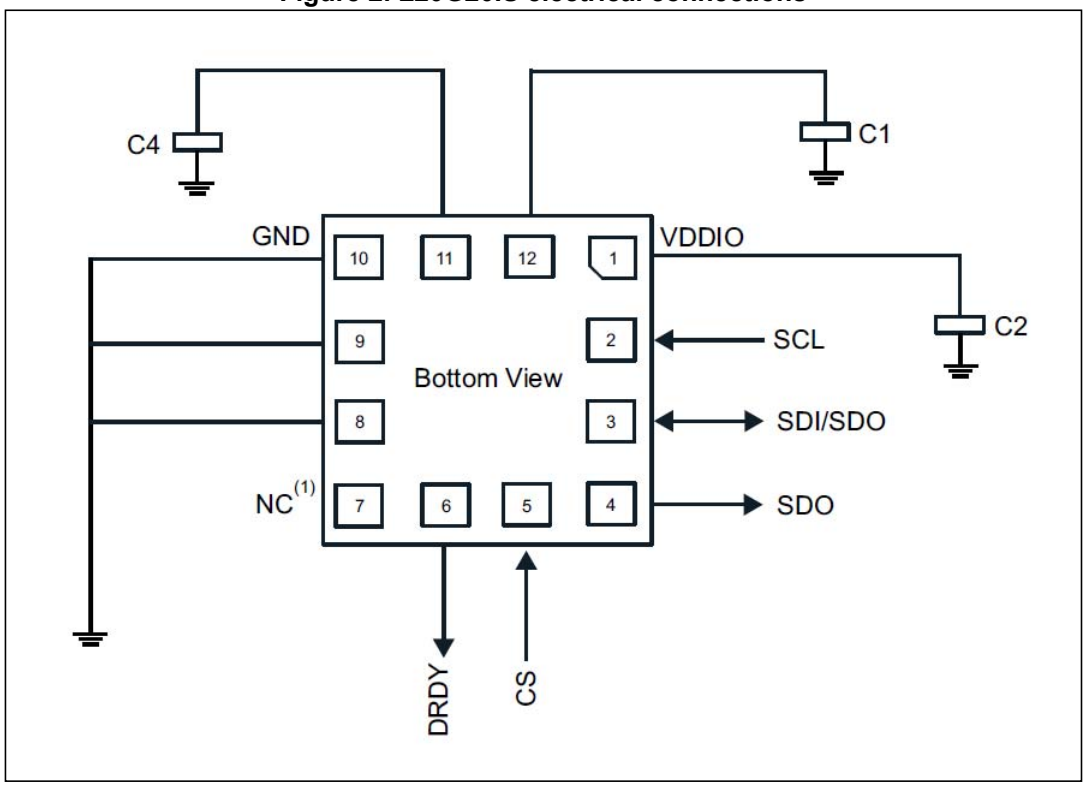
1 Readout chain

Figure 1. L20G20IS block diagram



2 Electrical connections and values for external components

Figure 2. L20G20IS electrical connections



1. Leave pin electrically unconnected and soldered to PCB.

Table 1. External components

External component	Value	Purpose
C1	100 nF	Decoupling
C2	100 nF	Decoupling
C4	100 nF (5 V class)	Internal regulator

Note: Power supply decoupling capacitors (C1, C2) should be placed as near as possible to the supply pins on the device (common design practice).

2.1 Internal pin status

Table 2. Internal pin status

Pin #	Pin name	Function	Status
1	VDDIO	Power supply for I/O pins	
2	SCL	Clock line for SPI interface	Default: input without pull-up
3	SDI/SDO	Serial data input (SDI) 3-wire interface serial data output (SDO)	Default: input without pull-up
4	SDO	Serial data output (SDO)	Default: input without pull-up
5	CS	Chip-select line	Default: input without pull-up
6	DRDY	Data ready signal	Default: push-pull to gnd
7	RES	Leave unconnected	Default: push-pull to gnd
8	RES	Connect to GND	Internally unconnected
9	RES	Connect to GND	Internally unconnected
10	GND	0 V power supply	
11	REG	Capacitance connection pin for internal regulator	
12	VDD	Power supply	

3 Registers

Table 3. Register address map

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WHO_AM_I	00h	1	1	0	1	1	0	1	0
TEMP_OUT_L	01h	Temp3	Temp2	Temp1	Temp0	0	0	0	0
TEMP_OUT_H	02h	Temp11	Temp10	Temp9	Temp8	Temp7	Temp6	Temp5	Temp4
OUT_X_L	03h	XD_7	XD_6	XD_5	XD_4	XD_3	XD_2	XD_1	XD_0
OUT_X_H	04h	XD_15	XD_14	XD_13	XD_12	XD_11	XD_10	XD_9	XD_8
OUT_Y_L	05h	YD_7	YD_6	YD_5	YD_4	YD_3	YD_2	YD_1	YD_0
OUT_Y_H	06h	YD_15	YD_14	YD_13	YD_12	YD_11	YD_10	YD_9	YD_8
DATA_STATUS_OIS	0Ah	XYOR_OIS	XOR_OIS	YOR_OIS	0	XYDA_OIS	XDA_OIS	YDA_OIS	0
CTRL1_OIS	0Bh	BOOT	DR_ PULSED	BLE	SIM	ODU	ORIENT	PW1	PW0
CTRL2_OIS	0Ch	SignX	SignY	LPF_BW1	LPF_BW0	0	HP_RST	SW_RST	HPF
CTRL3_OIS	0Dh	0	0	0	ST_SIGN	ST_EN	0	H_L_ ACTIVE	LP_BW2
CTRL4_OIS	0Eh	0	0	0	DRDY_EN	0	TEMP_ DATA_ON_ DRDY	DRDY_OD	0
OFF_X	0Fh	0	OFFX6	OFFX5	OFFX4	OFFX3	OFFX2	OFFX1	OFFX0
OFF_Y	10h	0	OFFY6	OFFY5	OFFY4	OFFY3	OFFY2	OFFY1	OFFY0
OIS_CFG_REG	1Fh	0	0	0	0	FS_SEL	0	HPF_BW[1]	HPF_BW[0]

4 Operating modes

The L20G20IS features three operating modes, normal mode, sleep mode and power-down, which are described in the following paragraphs.

To select the operating mode, the PW[1:0] bits in CTRL1_OIS (0Bh) are used.

Table 4. Operating selection

PW1	PW0	Operating mode selection
0	0	Power-down
0	1	Power-down
1	0	Sleep mode
1	1	Normal mode

4.1 Power-down mode

When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption.The SPI interface is still active to allow communication with the device. The content of the configuration registers is preserved and output data registers are not updated, therefore keeping the last data sampled in memory before going into power-down mode.

4.2 Sleep mode

When the device is set in sleep mode, the reading chain is completely turned off, while the mass is kept in oscillation, resulting in a lower power consumption than in normal mode. In this condition the device turn-on time is significantly reduced, allowing simple external power cycling.

4.3 Normal mode

When in normal mode, the angular rate data are generated at 9.33 kHz data rate (ODR); the full scale can be selected through the bit FS_SEL in OIS_CFG_REG (1Fh). Temperature data are generated at 70 Hz.

Table 5. Full-scale selection

FS_SEL	Full-scale selected
0	±100 dps
1	±200 dps

5 Startup sequence

Once the device is powered up, it automatically downloads the calibration coefficients from the embedded Flash to the internal registers. When the boot procedure is completed, i.e. after approximately 10 milliseconds, the device automatically enters power-down mode. To turn on the device and gather angular rate data, the device must be set in normal mode using the PW[1:0] bits in CTRL1_OIS (0Bh).

The following general-purpose sequence can be used to configure the device:

1. Write OIS_CFG_REG -- FS selection and HPF configuration (only if HPF is used)
2. Write CTRL2_OIS and CTRL3_OIS -- Digital LPF configuration and HPF enable (only if HPF is used)
3. Write OFF_X and OFF_Y -- User offset correction (not mandatory)
4. Write CTRL1_OIS -- Set the gyro in normal mode
5. Write CTRL2_OIS -- HPF enable reset (only if HPF is used)

The calibration steps for the OFF_X (0Fh) and OFF_Y (10h) registers are respectively -0.98 dps/LSB and 0.98 dps/LSB.

After power-up, the calibration coefficients can be re-loaded by setting the BOOT bit in the CTRL1_OIS (0Bh) register to 1. The boot request is executed as soon as the internal oscillator is turned on. It is possible to set this bit while in power-down mode: in this case, it will be served at the next normal or sleep mode selected. The procedure requires 10 milliseconds. During the boot time the registers are not accessible.

If a reset to the default value of the control registers is required, it can be performed by setting the SW_RST bit in the CTRL2_OIS (0Ch) register to 1. The procedure requires 1 millisecond.

5.1 Understanding angular rate data

The measured angular rates are sent to the OUT_X_H (04h), OUT_X_L (03h), OUT_Y_H (06h) and OUT_Y_L (05h) registers. These registers contain, respectively, the most significant part and the least significant part of the angular rate signals acting on the X and Y axes.

The complete angular rate data for the X and Y channels are given by the concatenation OUT_X_H & OUT_X_L (OUT_Y_H & OUT_Y_L) and are expressed as a 2's complement number.

Angular rate data are represented as 16-bit numbers.

5.2 Reading angular rate data

5.2.1 Using the status register

The device is provided with a status register, DATA_STATUS_OIS (0Ah), which should be polled to check when a new set of data is available. The procedure is as follows:

1. Read DATA_STATUS_OIS
2. If DATA_STATUS_OIS(3) = 0, then go to 1
3. If DATA_STATUS_OIS(7) = 1, then some data have been overwritten
4. Read OUTX_L
5. Read OUTX_H
6. Read OUTY_L
7. Read OUTY_H
8. Go to 1

The check performed at step 3 allows understanding whether the reading rate is adequate compared to the data production rate. If one or more angular rate samples have been overwritten by new data, because of a reading rate that is too slow, the XYOR_OIS bit of DATA_STATUS_OIS (0Ah) is set to 1.

The overrun bits are automatically cleared when all the data present inside the device have been read and new data have not been produced in the meantime.

5.2.2 Using the data-ready (DRDY) signal

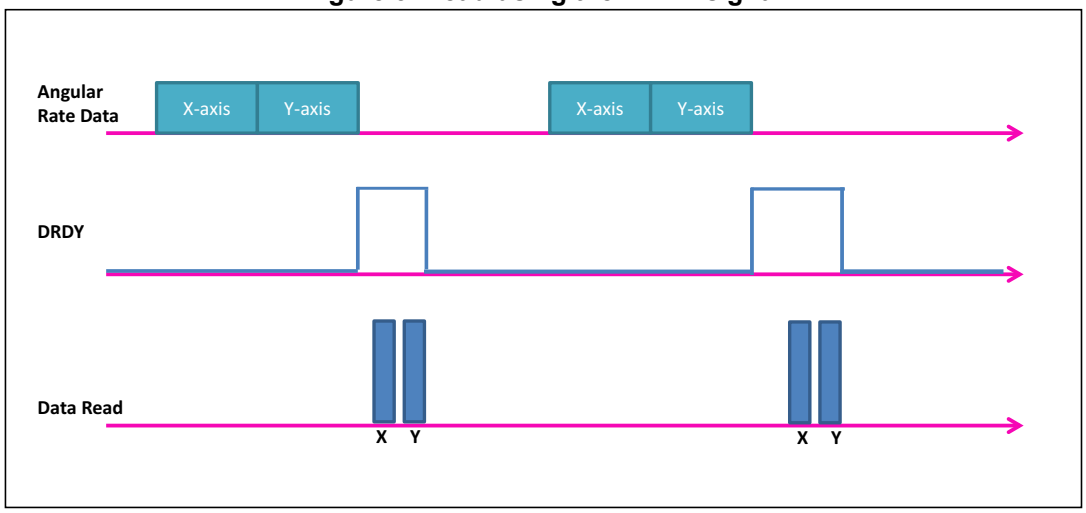
The device may be configured to have one HW signal to determine when a new set of measurement data is available to be read. This signal is equivalent to the XYDA_OIS bit in DATA_STATUS_OIS (0Ah). The DRDY_EN bit in CTRL4_OIS (0Eh) has to be set to '1' to enable the data-ready interrupt on the DRDY pin.

To properly perform a synchronous read, the angular rate data have to be read every time the DRDY pin goes high.

The DRDY signal can be latched (default condition) or pulsed if the DR_PULSED bit in CTRL1_OIS (0Bh) is set to '1'. The DRDY pin is set by default as a push-pull output, but it can be configured as an open-drain output by setting the DRDY_OD bit in CTRL4_OIS (0Eh) to '1'. The DRDY signal is configured as active high by default. It can be configured as active low by setting the H_L_ACTIVE bit in the CTRL3_OIS (0Dh) register to 1.

The interrupt is then reset when the output of all the channels has been read (OUT_X_L (03h), OUT_X_H (04h), OUT_Y_L (05h), and OUT_Y_H (06h)).

Figure 3. Read using the DRDY signal



5.3 Output data update (ODU)

By default the output data update (ODU) function is enabled in the L20G20IS, preventing the update of the output registers until MSB and LSB have been read.

This feature avoids reading values (most significant and least significant parts of the angular rate data) related to different samples. In particular, when the ODU bit is deasserted, the data registers related to each channel always contain the most recent angular rate data produced by the device, but, if a read of a given pair (i.e. OUT_X_H and OUT_X_L, OUT_Y_H and OUT_Y_L) is initiated, the refresh for that pair is blocked until both MSB and LSB parts of the data are read.

The ODU only guarantees that OUT_X(Y)_L and OUT_X(Y)_H have been sampled at the same moment. For example, if the reading speed is too slow, it may be possible to read the angular rate data of the x-axis sampled at T1 while the y-axis data sampled at T2.

The ODU function can be configured in CTRL1_OIS (0Bh). If the ODU bit is asserted, the output registers are updated continuously.

5.4 Big-little endian selection

In the L20G20IS it is possible to swap the content of the lower and the upper part of the angular rate registers (i.e. OUT_X_H with OUT_X_L), to be compliant with both little-endian and big-endian data representations.

"Little Endian" means that the low-order byte of the number is stored in memory at the lowest address, and the high-order byte at the highest address. (The little end comes first).

This mode corresponds to bit BLE in CTRL1_OIS (0Bh) set to 0 (default configuration).

On the contrary, "Big Endian" means that the high-order byte of the number is stored in memory at the lowest address, and the low-order byte at the highest address.

The following table provides a few basic examples of the gyroscope data that is read in the data registers when the device is subjected to a given angular rate.

Table 6. Output data registers content vs. angular rate (FS = 100 dps)

Angular rates values	BLE = 0		BLE = 1	
	Register address			
	OUT_X_H (04h)	OUT_X_L (03h)	OUT_X_H (04h)	OUT_X_L (03h)
0 dps	00h	00h	00h	00h
43 dps	2Ch	A4h	A4h	2Ch
87 dps	59h	49h	49h	59h
-43 dps	D3h	5Ch	5Ch	D3h
-87 dps	A6h	B7h	B7h	A6h

5.5 Orientation configuration

On the L20G20IS it is possible to change the sign and the orientation of the gyroscope axes through the SignX and SignY bits of the register CTRL2_OIS (0Ch) and the ORIENT bit of the CTRL1_OIS (0Bh) register. In particular the SignX and SignY bits can be used to invert the sign of the X and Y-axis respectively.

The ORIENT bit in the CTRL1_OIS (0Bh) register allows changing the orientation of the X and Y axes as given in the table below.

Table 7. Orientation configuration

ORIENT	OUT_X_L, OUT_X_H	OUT_Y_L, OUT_Y_H
0	X-axis	Y-axis
1	Y-axis	X-axis

6 Temperature sensor

The L20G20IS automatically measures the temperature and provides the data through the TEMP_OUT_L (01h) and TEMP_OUT_H (02h) registers, at a data rate of 70 Hz.

For the temperature sensor, the data-ready signal can be driven to the DRDY pad by setting the TEMP_DATA_ON_DRDY bit in the CTRL4_OIS (0Eh) register to 1.

The complete temperature data are given by the concatenation of TEMP_OUT_L (01h) and TEMP_OUT_H (02h), as two's complement data in 12-bit format, left-justified, with a sensitivity of 0.0625 °C/digit. The output of the temperature sensor is 0 at 25 °C.

The L20G20IS allows swapping, by setting the BLE bit of the CTRL1_OIS (0Bh) register, the content of the lower and the upper part of the temperature output data registers.

The following table provides a few basic examples of the temperature data that is read in the data registers when the device is subject to a given temperature.

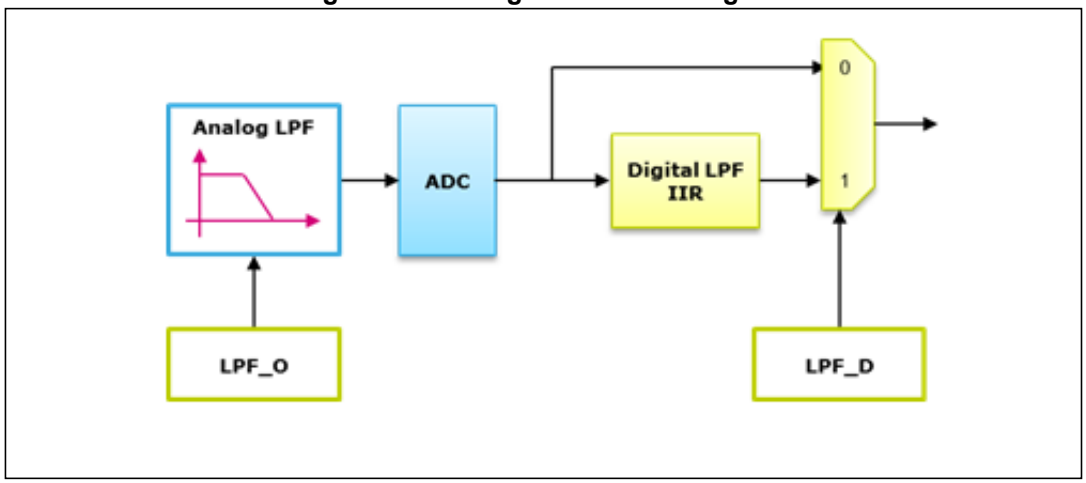
Table 8. Output data registers content vs. temperature

Temperature values	BLE = 0		BLE = 1	
	Register address			
	TEMP_OUT_H (02h)	TEMP_OUT_L (01h)	TEMP_OUT_H (02h)	TEMP_OUT_L (01h)
0 °C	E7h	00h	00h	E7
25 °C	00h	00h	00h	00h
50 °C	19h	00h	00h	19h

7 Filtering chain

The filtering chain for the L20G20IS appears in the figure below.

Figure 4. Filtering chain block diagram



7.1 High-pass filtering chain

The L20G20IS integrates a 1st order digital high-pass filter and it can be enabled by setting the HPF bit in CTRL2_OIS (0Ch) to '1'.

Using the HPF_BW[1:0] bits in OIS_CFG_REG (1Fh), it is possible to select the high-pass filter cutoff frequency as indicated in *Table 9*.

If the HPF bit is set to '0', then the content of the HPF_BW[1:0] bits is not considered.

Figure 5. HPF chain block diagram

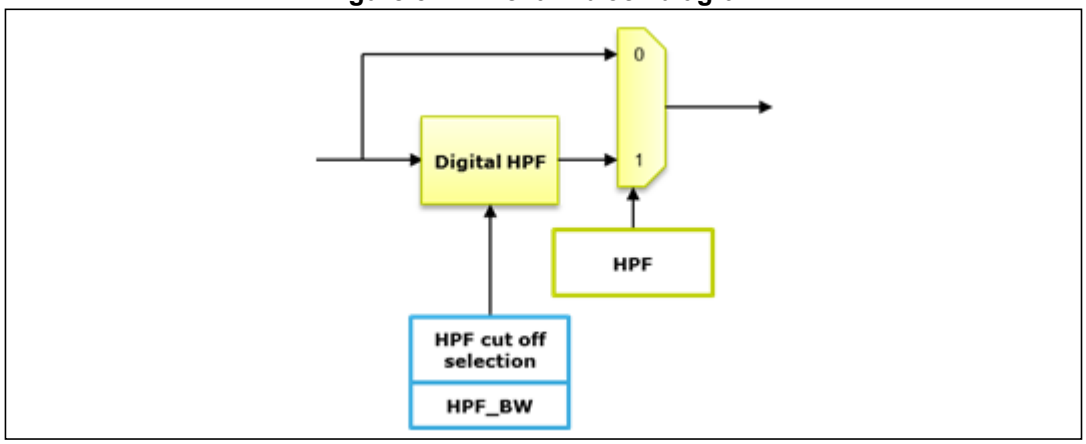
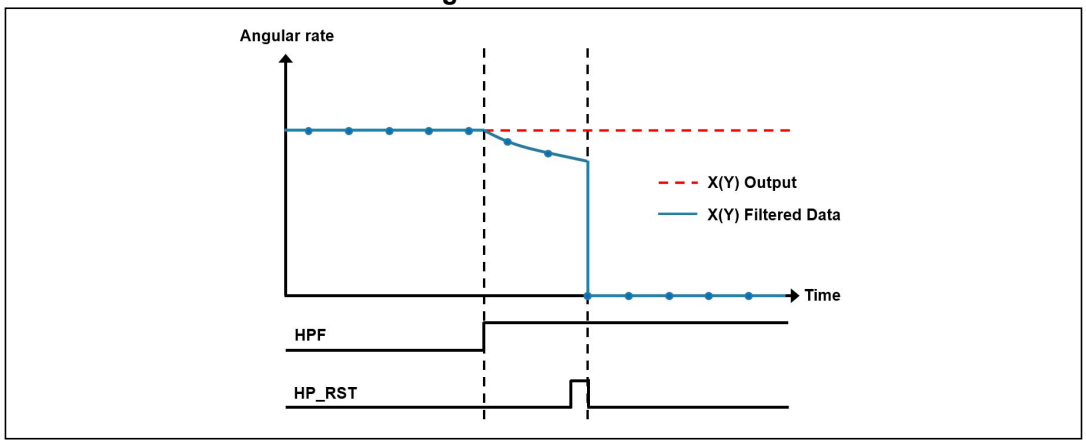


Table 9. High-pass filter cutoff frequency selection

HPF_BW[1]	HPF_BW[0]	HPF cutoff [Hz]
0	0	0.023
0	1	0.091
1	0	0.324
1	1	1.457

The high-pass filter can be reset instantly by deleting the DC component of the angular rate. This reset can be performed by setting the HP_RST bit in the CTRL2_OIS (0Ch) register to ‘1’. HP_RST automatically resets to 0.

Figure 6. HPF reset



7.2 Low-pass filtering chain

The L20G20IS integrates a programmable digital low-pass filter.

It can be configured through the LP_BW1 and LP_BW0 bits of the register CTRL2_OIS (0Ch) and the LP_BW2 bit of the register CTRL3_OIS (0Dh).

The following table shows the digital LPF bandwidth, based on the LP_BW2, LP_BW1 and LP_BW0 bits settings.

Table 10. Low-pass filter bandwidth selection

LPF_BW2	LP_BW1	LP_BW0	LPF Bandwidth [Hz]	Phase delay [°]
0	0	0	290	7 @ 20 Hz
0	0	1	210	9 @ 20 Hz
0	1	0	160	11 @ 20 Hz
0	1	1	450	5 @ 20 Hz
1	x	x	1150	1 @ 10 Hz

8 Self-test

The embedded self-test functions allows checking the device functionality without moving it.

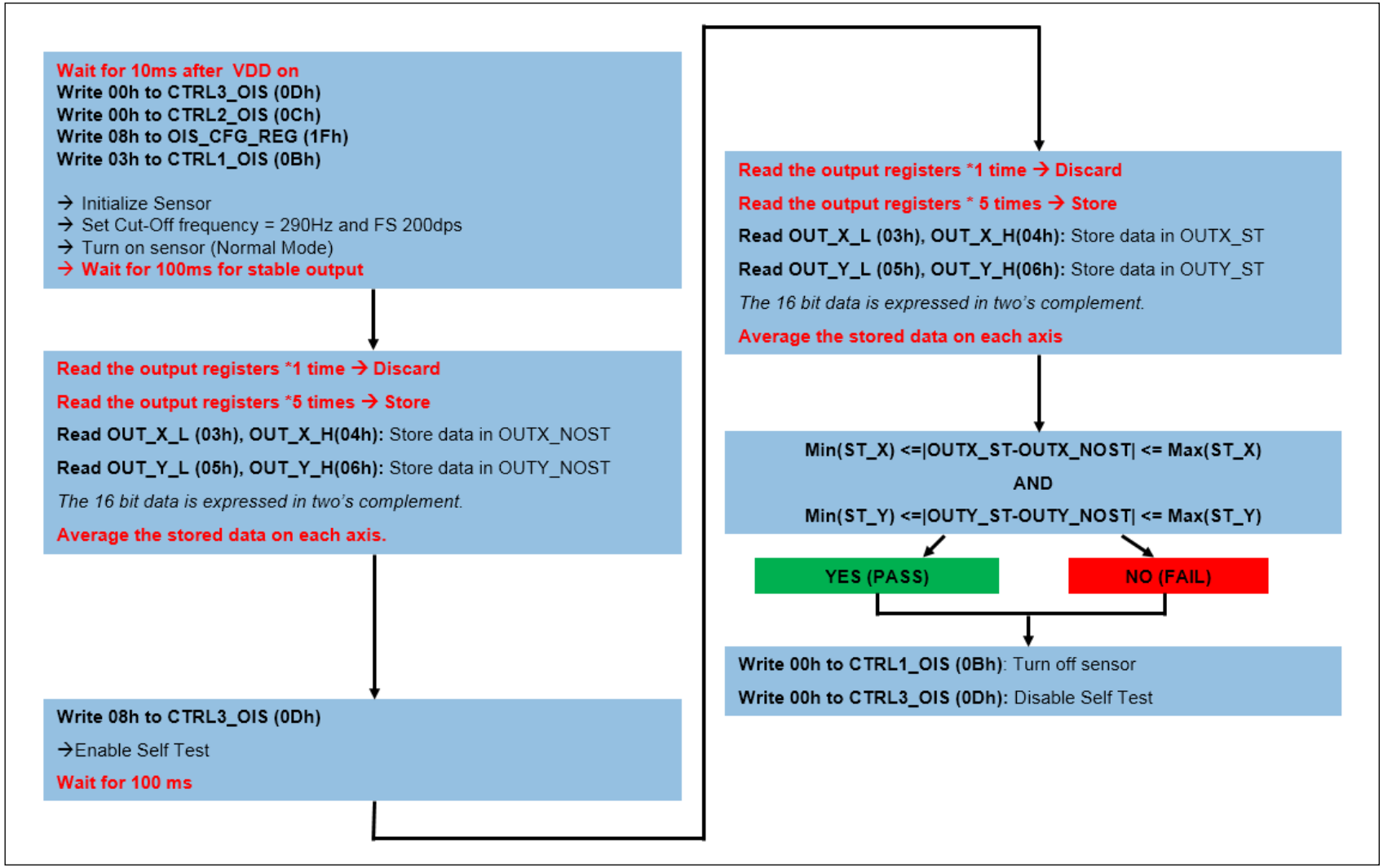
It allows testing the mechanical and electrical parts of the gyroscope sensor. When the self-test is activated, an actuation force is applied to the sensor, simulating a definite Coriolis force, and the seismic mass is moved by means of this electrostatic test-force. In this case the sensor output exhibits an output change.

The self-test function can be enabled through the ST_EN bit of the CTRL3_OIS (0Dh) register. The self-test sign can be selected through the ST_SIGN bit of the CTRL3_OIS (0Dh) register: if it is enabled, the self-test sign is inverted.

When the gyroscope self-test is active, the sensor output level is given by the algebraic sum of the signals produced by the velocity acting on the sensor and by the electrostatic test force.

The complete gyroscope self-test procedure is indicated in the following figure.

Figure 7. Self-test



9 Revision history

Table 11. Document revision history

Date	Revision	Changes
23-Feb-2018	1	Initial release