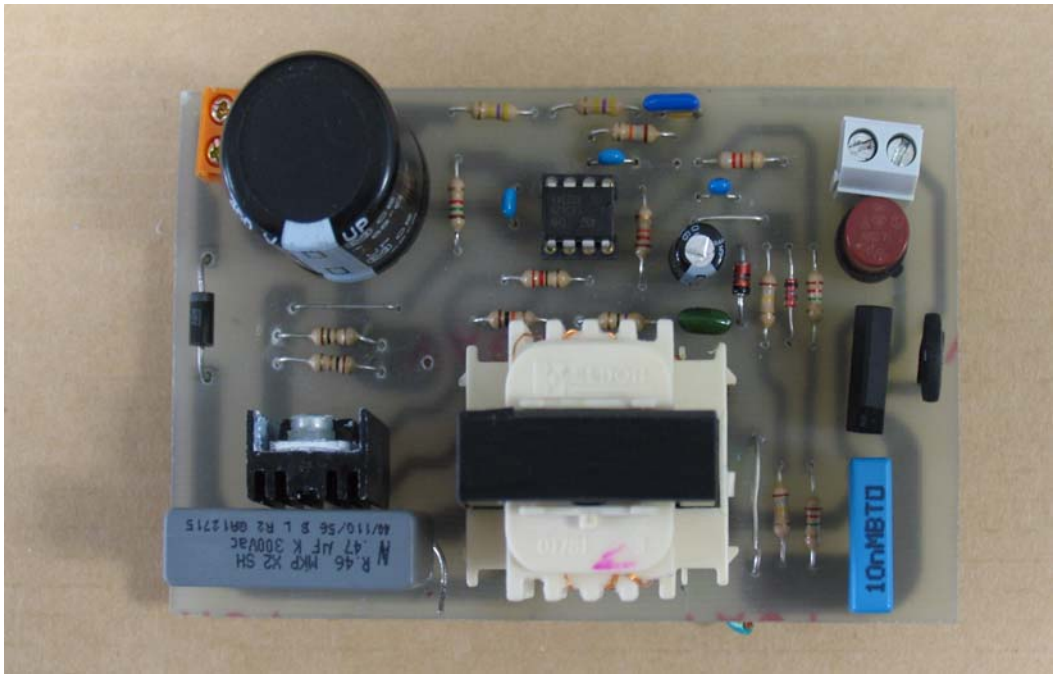
AN2435
Application note

TM sepic converter in PFC pre-regulator

Introduction

For the PFC (power factor correction) converter, sepic topology can be used when an output voltage lower than the maximum input voltage is required. This is instead of boost topology, which is unsuitable beacuse it must have an output voltage higher than the maximum input voltage. Sepic topology is advantageous because it allows the use of the ripple steering technique in order to reduce the switching frequency components of the input current without additional costs. This application note presents the basic equation of the sepic converter, in addition to design guidelines for a sepic PFC operating in transition mode and using the ripple steering technique. An application example with some tests results and waveforms is also provided in the document.

Sepic converter



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1 Sepic topology for PFC converter

The most widely used topology in PFC applications is boost topology. It has two main advantages:

1. The power switch is a low sided one, unlike buck and buck-boost topology where it is an hide side one and needs a floating driving circuit.
2. The inductor is on the input side of the converter, limiting the slope of the input current.

The main disadvantage is that output voltage must always be higher then maximum input voltage, which may limit some applications and may be a problem when a lower output voltage is required.

Sepic topology has the above advantages and does not have the output voltage constraint. As in buck-boost topology, output voltage can be higher or lower than the input voltage. An additional advantage of sepic topology is that there are two inductors instead of one which can be wounded in the same magnetic core. Using the proper turn ratio the input current ripple can be reduced theoretically to zero and the input filter for the conducted electro-magnetic interference strongly reduced (theoretically eliminated).

However, sepic topology, compared to boost topology, has the following disadvantages:

1. The MOSFET and the output diode break-down voltages are higher as they are the maximum reverse voltage when input and output voltages are summed (only output voltage for boost converter).
2. The current through the MOSFET is generally higher for the same output power.

1.1 Operation of the sepic converter

The basic schematic of the sepic converter is given in *Figure 1*.

Assuming that the average voltage across each inductor during one switching cycle, in steady state operation, is zero, it can also be assumed than the average voltage over one switching cycle across capacitor C1 equals the input voltage of the converter.

If capacitor C1 is not too small, the voltage ripple across C_1 (V_{C1}) is negligible, and it can be assumed that over one switching cycle, this voltage stays constant and equals the input voltage (V_{IN}). This hypothesis (V_{C1}= V_{IN}) is the starting point for sepic converter analysis.

When the main switch (M_1) of the sepic converter is on, input voltage is applied to inductor L_2 (see *Figure 2*). In steady state condition, the same voltage is applied to inductor L1 which is in parallel with capacitor C1. The reverse voltage applied on diode D_1 is the sum of the input and output voltage (V_{IN} + V_{OUT}) and the current through M1 is the sum of the currents through inductor L1 and inductor L2 (I_{L1} + I_{L2}).

Across inductor L1 and inductor L2 we have the same voltages and the currents throug them rise linearly with slopes inversely proportional to their inductances values.

When M1 is switched off (*Figure 3*), diode D1 starts to conduct and the energy previously stored in inductor L1 and inductor L2 is released to restore the energy used up by capacitor C1 and capacitor C_2 when M1 was on. This energy also supplies the load. *The voltage across the MOSFET is the sum of the voltage across capacitor C1, which is equal to the sum of the input and the output voltage.*

The current through diode D1 is the sum of the currents running through inductor L1 and inductor L2. The voltage across both inductors is equal to V_{OUT}, and the current slope is negative and inversely proportional to inductor L1 and inductor L2 respectively.

Figure 4 shows the theoretical waveforms of the inductors' currents. *Equation 1* and *Equation 2* give the waveform expressions during turn-on (T_{ON}), whilst *Equation 3* and *Equation 4* give the waveform expressions during turn-off (T_{OFF}).

Equation 1

$$I_{L1}(t) = I_{L10} + \frac{V_{IN}}{L_1} \bullet t$$

Equation 2

$$I_{L2}(t) = I_{L20} + \frac{V_{IN}}{L_2} \bullet t$$

Equation 3

$$I_{L1}(t) = I_{L10} + \frac{V_{IN}}{L_1} \bullet T_{ON} - \frac{V_{out}}{L_1} \bullet t$$

Equation 4

$$I_{L2}(t) = I_{L20} + \frac{V_{IN}}{L_1} \bullet T_{ON} - \frac{V_{out}}{L_2} \bullet t$$

Figure 1. Basic circuit of the sepic converter

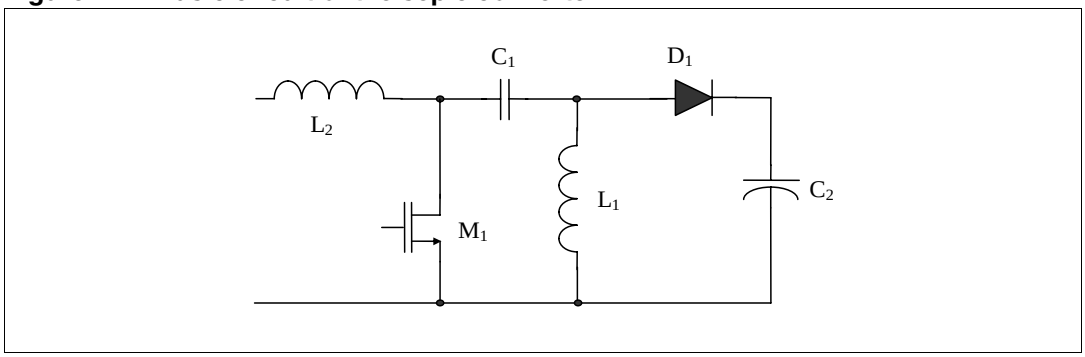


Figure 2. Sepic converter when the main switch is on

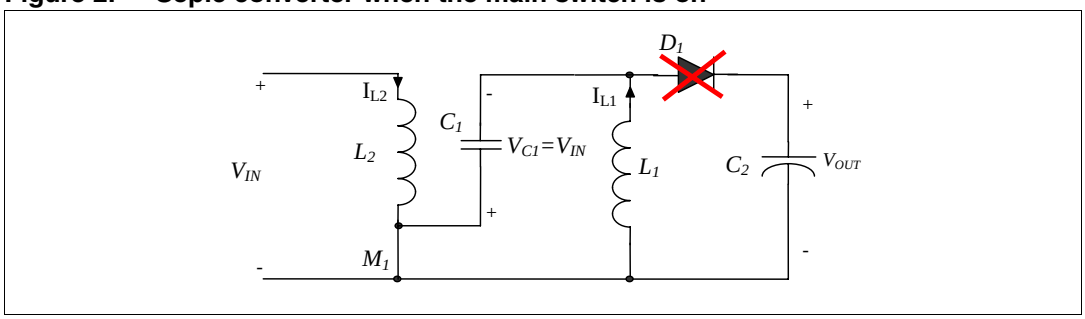


Figure 3. Sepic converter when the main switch is off

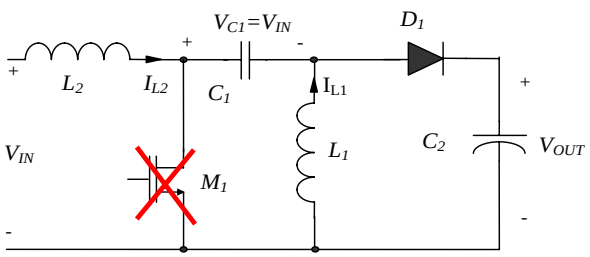
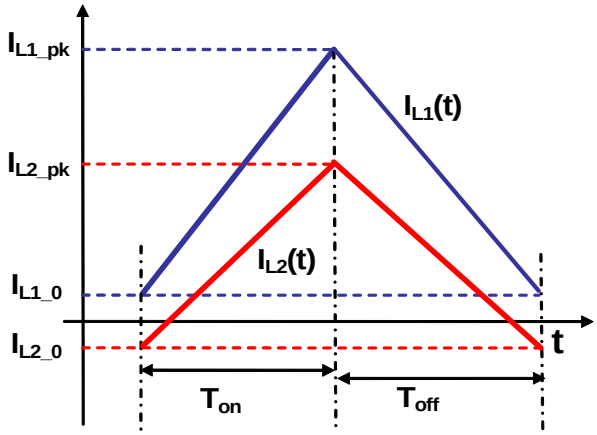


Figure 4. Inductor L1 and inductor L2 current waveform



1.2 Sepic converter as a PFC circuit operating in transition mode [1.]

In PFC applications, input voltage is the rectified main and it changes according to the equation:

Equation 5

$$V_{IN}(\vartheta) = \sqrt{2} \bullet V_{ac} \bullet |\sin(\vartheta)|$$

where ϑ is 2 πf_L, f_L is the line frequency, and V_{ac} is the rms value of the line voltage.

As switching frequency is in the range of some tenth of kHz, and thus much higher than the line frequency, we can assume ϑ is constant over each switching cycle.

The L6562 (see [2]) is a current mode controller dedicated to PFC applications. It is used in this instance. It senses the MOSFET current and the input voltage of the converter (rectified main), through a sense resistor and a resistor divider respectively. Cycle by cycle the MOSFET is switched-off as the sensed current reaches a limit set by the controller. This limit is proportional to the sensed input voltage so, the MOSFET peak current ($I_{PK}(t)$) follows a sinusoidal reference:

Equation 6

$$I_{PK}(t) = I_{PK} \bullet |\sin(\vartheta)|$$

Taking into account that input voltage is now the rectified main, *Equation 1* and *Equation 2* can be rewritten as follows:

Equation 7

$$I_{L1}(t,\ \vartheta) = I_{L10} + \frac{V_{IN}(\vartheta)}{L_1} \bullet t,\ I_{L2}(t,\ \vartheta) = I_{L20} + \frac{V_{IN}(\vartheta)}{L_2} \bullet t$$

Due to transition mode operation, the MOSFET is switched on as soon as the diode current falls to zero. This means that:

Equation 8

$$I_{L10} - I_{L20} = 0$$

From and *Equation 8*, the MOSFET peak current equation may be derived:

Equation 9

$$I_{PK}(\vartheta) = \left(\frac{1}{L_1} + \frac{1}{L_2}\right) \bullet t_{ON}(\vartheta) \bullet \sqrt{2} \bullet V_{ac} \bullet \sin(\vartheta)$$

Combining *Equation 9* and *Equation 6* an expression for T_{ON} may be obtained:

Equation 10

$$t_{ON}(\vartheta) = \frac{I_{PK} \bullet \sin(\vartheta)}{\left(\frac{1}{L_1} + \frac{1}{L_2}\right) \bullet \sqrt{2} \bullet V_{ac} \bullet \sin(\vartheta)} = \frac{L_e \bullet I_{PK}}{\sqrt{2} \bullet V_{ac}} = T_{ON}$$

where L_e is the parallel between inductor L1 and inductor L2. *Equation 10* indicates that, as in TM (Transition Mode) boost converter T_{ON} is independent from ϑ.

The expression for T_{OFF} is obtained in a similar way to above:

Equation 11

$$T_{OFF}(\vartheta) = \frac{T_{ON} \bullet \sqrt{2} \bullet V_{ac} \bullet \sin(\vartheta)}{V_O}$$

where V_O is the output voltage. The off time is dependent on θ, as in TM boost converter.

Once T_{ON} and T_{OFF} are known, switching frequency (f_{SW}) may be easily calculated as it is a function of ϑ:

Equation 12

$$f_{SW}(\vartheta) = \frac{1}{T_{ON} + T_{OFF}(\vartheta)} = \frac{1}{T_{ON} \bullet \left(1 + \frac{\sqrt{2} \bullet V_{ac} \bullet |\sin(\vartheta)|}{V_O}\right)}$$

Figure 5 shows the switching frequency versus θ for two different input voltages. To calculate input current averaged over one switching cycle, *Equation 13*, the charge balance on capacitor C1, is used:

Equation 13

$$\left(I_{L10}(\vartheta) + \frac{1}{2} \bullet \frac{V_{IN}(\vartheta)}{L_1} \bullet T_{ON}\right) \bullet T_{ON} = \left(I_{L20}(\vartheta) + \frac{1}{2} \bullet \frac{V_{IN}(\vartheta)}{L_2} \bullet T_{ON}\right) \bullet T_{OFF}(\vartheta) = Q(\vartheta)$$

where Q (ϑ) indicates the quantity of electrical charge that flows through capacitor C1, cycle by cycle.

Combining *Equation 8* and *Equation 13*, $I_{L2(0)}(\vartheta)$ may be calculated as follows:

Equation 14

$$I_{L20}(\vartheta) = \frac{f_{SW}(\vartheta) \bullet V_{IN}(\vartheta) \bullet T_{ON}}{2} \bullet \left[\frac{T_{ON}}{L_1} - \frac{T_{OFF}(\vartheta)}{L_2}\right]$$

Using equation 14, I_{L2avg} may then be calculated using *Equation 15*:

Equation 15

$$I_{L2avg}(\vartheta) = \frac{1}{2} \bullet \frac{V_{IN}(\vartheta)}{L_2} \bullet T_{ON} + I_{L20}(\vartheta) = \frac{1}{2} \bullet I_{PK} \bullet \frac{|\sin(\vartheta)|}{1 + \frac{\sqrt{2} \bullet V_{AC}}{V_O}|\sin(\vartheta)|}$$

Equation 15 shows that the input current is not exactly sinusoidal. A certain amount of distortion is related to the quantity K_v, which is defined as follows:

$$K_V = \frac{\sqrt{2} \times V_{AC}}{V_O}$$

Figure 6 shows the input currents (before the bridge diodes) for different values of V_{AC}. The first input current, $I_0(\theta)$, is calculated for K_v= 0. It is used only as a reference, because it is completely sinusoidal. In this instance, V_O is considered to be 200 V. The second input current, $I_1(\theta)$, is at V_{AC} = 265 V and the third, $I_2(\theta)$, is the input current at V_{AC} = 175 V. All currents are normalized in accordance with their respective RMS values. In figure 6, the distortion of the current with respect to a perfect sinusoid is obvious. Even though such distortion is present, quite high values for the power factor are obtained. The voltage across capacitor C1 averaged over one switching cycle is the same as the input voltage. There is an additional voltage ripple due to the currents of the inductors across capacitor C1. Its amplitude ($\Delta V_{C1}(\vartheta)$) is calculated below:

Equation 16

$$\Delta V_{C1}(\vartheta) = \frac{V_{IN}(\vartheta) \bullet T_{ON}^{2}}{C_1 \bullet L_e} \bullet \frac{T_{OFF}(\vartheta)}{T_{ON} + T_{OFF}(\vartheta)}$$

Substituting the values of T_{ON} (*Equation 10*), T_{OFF} (*Equation 11*), and $V_{IN}(\theta)$ (*Equation 5*), $\Delta VC1\ (\vartheta)$ may be expressed as follows:

Equation 17

$$\Delta V_{C1}(\vartheta) = \frac{L_e}{C1} \bullet \frac{I_{PK}^2}{2} \bullet \frac{|\sin(\vartheta)|^2}{(V_O + \sqrt{2} \bullet V_{ac} \bullet |\sin(\vartheta)|)}$$

It is useful to rewrite some quantities calculated earlier, in terms of converter output power, RMS input voltage (V_{AC}) , and expected efficiency (η), because these quantities are generally known at the beginning of a design. Input power may be expressed as follows:

Equation 18

$$P_{in} = f_L \bullet \int_0^{\frac{1}{f_L}} \left[\frac{I_{PK}}{2} \bullet \frac{\sin(2\pi f_L \bullet t)}{1 + K_v \bullet |\sin(2\pi f_L \bullet t)|} \bullet \sqrt{2} \bullet V_{ac} \bullet \sin(2\pi f_L \bullet t) \right] \bullet dt$$

(F(Kv)) may be calculated as follows:

Equation 19

$$F(k_v) = f_L \bullet \int_0^{\frac{1}{f_L}} \left[\frac{\sin^2(2\pi f_L \bullet t)}{1 + k_v \bullet |\sin(2\pi f_L \bullet t)|} \right] \bullet dt$$

I_{PK} may be expressed as follows:

Equation 20

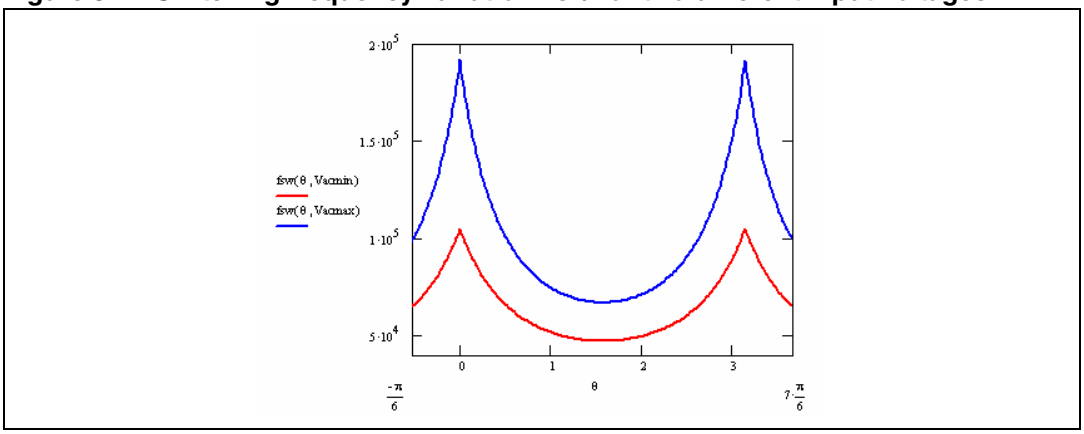
$$I_{PK} = \frac{2 \bullet P_O}{\eta \bullet \sqrt{2} \bullet V_{ac} \bullet F(k_v)}$$

The switching frequency can be expressed as:

Equation 21

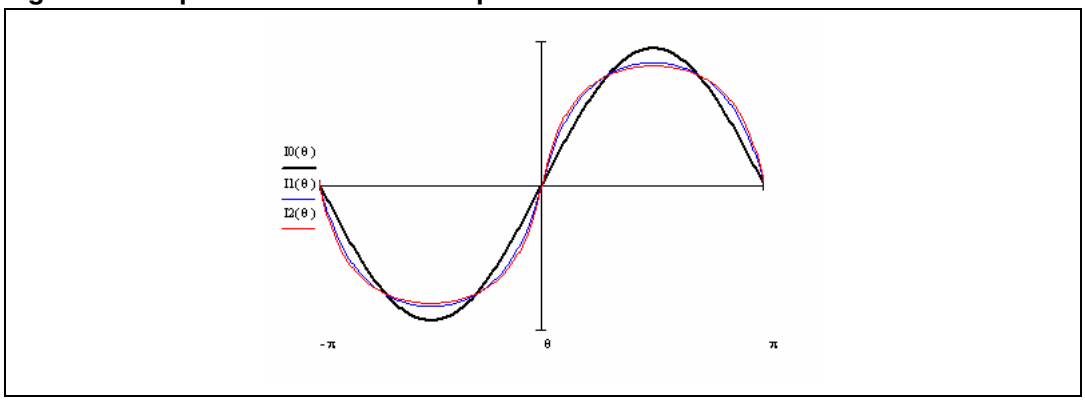
$$f_{sw}(\vartheta) = \frac{\eta \bullet V_{ac}^2 \bullet F(k_v)}{P_O \bullet L_e \bullet (1 + k_v \bullet |\sin(\vartheta)|)}$$

Figure 5. Switching frequency variation vs θ for two different input voltages



1. Where V_{acmin} = 175 V, V_{acmax} = 265 V, L_e = 1 mH, h = 0.9, and P_O = 65W.

Figure 6. Input current in TM for sepic PFC



1.3 Coupled inductor sepic converter and ripple steering

If the two inductors are wounded in the same magnetic core, it is possible to reuse the equations used in *Section 1.2*. Moreover, the current ripple in the input inductor L_2 can theoretically be reduced to zero, simply by selecting the correct turn ratio. A model of two coupled inductors is shown in *Figure 8*. L_{lk1} and L_{lk2} are the leakage inductances, L_M is the magnetizing inductance and n is the turn ratio.

The equations that describe the coupled inductor model of *Figure 8* are given below.

Equation 22

$$\begin{cases} v_1(t) = L_{L1} \bullet \frac{dI_1(t)}{dt} + L_M \bullet \frac{dI_M(t)}{dt} \\ v_2(t) = L_{L2} \bullet \frac{dI_2(t)}{dt} + n \bullet L_M \bullet \frac{dI_M(t)}{dt} \\ \frac{dI_M}{dt} = \frac{dI_1}{dt} + n \bullet \frac{dI_2(t)}{dt} \end{cases}$$

In the first two sub equations of *Equation 22*, the derivate of the magnetizing current (I_M) can be substituted with the value given in sub-equation 3.

Considering that the same voltage is applied to both inductors we have:

Equation 23

$$\begin{cases} v_1(t) = L_{EQ1} \bullet \frac{dI_1(t)}{dt} \\ v_2(t) = L_{EQ2} \bullet \frac{dI_2(t)}{dt} \end{cases}$$

Equation 24

$$\begin{cases} L_{EQ1} = \frac{L_{L1} \bullet L_{L2} + L_M \bullet L_{L2} + n^2 \bullet L_M \bullet L_{L1}}{L_{L2} + n \bullet (n-1) \bullet L_M} \\ L_{EQ2} = \frac{L_{L1} \bullet L_{L2} + L_M \bullet L_{L2} + n^2 \bullet L_M \bullet L_{L1}}{L_{L1} - (n-1) \bullet L_m} \end{cases}$$

The main conclusion of *Equation 23* and *Equation 24*, is that the same equations can be used for coupled and uncoupled inductors. If no current flows on the secondary side, voltage V_2 is the same as voltage V_2^1 (see *Figure 8*) and may be written as follows:

Equation 25

$$V_2 = V_2^1 = n \bullet V_1^1 = n \bullet \frac{L_M}{L_M + L_{LK1}} \bullet V_1$$

As the same voltage is applied, simultaneously, to both inductors in a sepic converter, *Equation 25* may be simplified below as:

Equation 26

$$n \bullet \frac{L_M}{L_M + L_{LK1}} = 1$$

When the above 'ripple steering' condition is verified theoretically, the voltage across L_{LK2} is zero and no current flows on the secondary side. In the actual circuit only the high frequency components of the inductor L2 current are attenuated. Once *Equation 26* is verified, *Equation 24* may be simplified as:

Equation 27

$$\begin{cases} L_{EQ1} = L_M + L_{LK1} \\ L_{EQ2} = \infty \end{cases}$$

Therefore, for a sepic converter with coupled inductors, infinite inductance at the input may be seen theoretically once *Equation 26* is satisfied. In the actual circuit, due to imperfect matching with *Equation 26* and due to the fact that the voltages applied to the two inductors are not exactly the same (because of the voltage ripple on capacitor C1), a large input inductance may be seen at the converter input. This input inductance helps the line filter in eliminating the switching frequency component of the input current.

Figure 7. Coupled inductor of a sepic converter

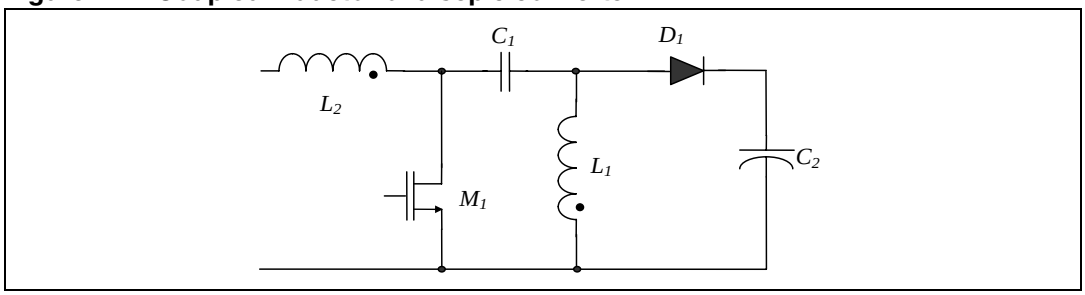
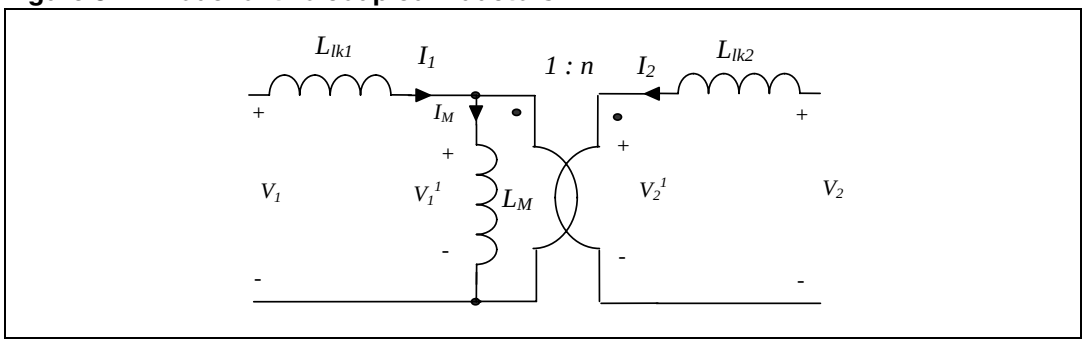


Figure 8. Model of two coupled inductors



1.4 Small signal model for a TM sepic converter

It is possible to model the output stage of the sepic converter as a current source. The sourced current is a function of the input voltage RMS value, the output voltage, and the MOSFET peak current. To obtain the necessary function, the output diode current may first by averaged over each switching cycle, to give the following equation:

Equation 28

$$I_{D1}(\vartheta) = \frac{k_{vmin}}{2} \bullet \frac{I_{PK} \bullet (\sin(\vartheta))^2}{1 + k_v \bullet |\sin(\vartheta)|}$$

Assuming that the control loop reaction must be very slow to remain constant over a single line cycle, then to ensure high PFC, *Equation 28* may be averaged with respect to θ as follows:

Equation 29

$$I_{Dlavg}(V_{ACRMS},\ V_O,\ I_{PK}) = \frac{1}{2} \bullet \frac{\sqrt{2} \bullet V_{ACRMS}}{V_O} \bullet I_{PK} \bullet F\left(\frac{\sqrt{2} \bullet V_{ACRMS}}{V_O}\right)$$

For small variations of its argument, the I_{D1AVG} function may be approximated with a linear function, and the output stage of the sepic converter may be represented by the circuit in *Figure 10*. Bearing in mind that $F(K_v)$ was defined in *Equation 19*, expressions for g_2 (see *Figure 10*), e_2 (see *Figure 10*) and r_2 (see *Figure 10*) are given below:

Equation 30

$$g_2 = \frac{\partial I_{D1AVG}}{\partial I_{ACRMS}}$$

$$e_2 = \frac{\partial I_{D1AVG}}{\partial I_{PK}} = \frac{1}{2} \bullet K_v \bullet F(K_v)$$

$$r_2 = -\left[\frac{\partial I_{D1AVG}}{\partial V_O}\right]^{-1} = \left[\frac{I_{PK}}{2 \bullet V_O} \bullet K_v \bullet \left(F(K_v) + K_v \bullet \frac{\partial F(K_v)}{\partial K_v}\right)\right]^{-1}$$

It should be remembered that K_v was defined as:

$$K_V = \frac{\sqrt{2} \times V_{AC}}{V_O}$$

Also, note that g_2 is not calculated here because is not used in the control Loop design. Then, using *Figure 10* and the sub-equations of *Equation 30*, it is possible to deduce the small signal transfer function (control to output) $G_{(S)} = V_{COMP}(s)/V_O(s)$.

Equation 31

$$G(s) = \frac{\partial \hat{V}_O}{\partial \hat{V}_{COMP}} = \frac{G_O}{1 + \frac{s}{\omega_P}}$$

where the gain (G_O) and the pole frequency (ω_P) are defined below:

Equation 32

$$G_O = K_P \bullet K_M \bullet e_2 \bullet \frac{\sqrt{2} \bullet V_{ACrms}}{R_{SENSE}} \bullet \frac{r_2 \bullet R_O}{r_2 + R_O},\ \omega_P = \frac{r_2 - R_O}{C_2 \bullet r_2 \bullet R_O}$$

where (R_O) is the assumed resistive load.

Figure 9. Equivalent current source of the sepic converter

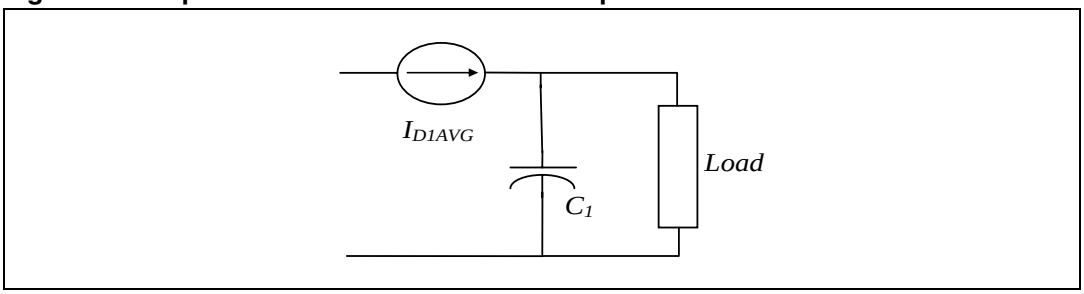
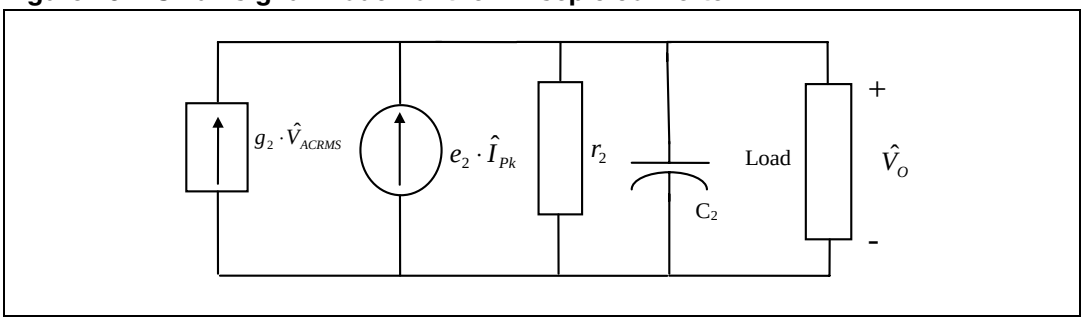


Figure 10. Small signal model for the TM sepic converter



2 Practical design example of a sepic converter

A practical example of a sepic converter is described below.

2.1 Design specifications

For the input data, the design specifications are needed.

Table 1. Design specification

Quantity	Value
Mains voltage range: $V_{INMIN\ (RMS)}$ – $VI_{NMAX\ (RMS)}$	175 V_{ACRMS} - 265 V_{ACRMS}
Regulated DC output voltage	200 V
Rated Output Power: P_O	65 W
Minimum switching frequency: f_{swmin}	45 kHz
Maximum over-voltage admitted: ΔV_{OVP}	40 V
Maximum output voltage ripple ΔV_O	20 V
Expected efficiency: η	90 %
Maximum mains RMS current	$I_{INRMSMAX} = \frac{P_O}{\eta \bullet V_{ACMIN}} = 420mA$

Table 1. Design specification (continued)

Quantity	Value
Rated output current: I_O	$I_O = \frac{P_O}{V_O} = 325mA$
Output equivalent resistor	$I_O = \frac{V_O^2}{P_O} = 615\Omega$

The complete schematic of the circuit is given in *Figure 13*.

2.2 MOSFET (M_1) selection

The MOSFET peak current value (I_{PK}) is calculated using *Equation 18*. Substituting the quantities given in the electrical specifications, the MOSFET peak current value is I_{PK} = 2.36 A. The RMS value of the current flowing through the MOSFET may be calculated using *Equation 33*:

Equation 33

$$I_{M1RMS} = I_{PK}\sqrt{\frac{F(K_{vmin})}{3}} = 0.678A$$

where:

Equation 34

$$K_{vmin} = \frac{\sqrt{2} \bullet V_{ACMIN(RMS)}}{V_O}$$

Under the worst case scenario, the MOSFET and the output diode have to sustain a voltage that is the sum of the maximum peak input voltage and the maximum output voltage. Considering the electrical specifications above and a safety margin of 10%, the minimum breakdown voltage ($B_{DVSSMin}$) for M1 is:

Equation 35

$$B_{DVSSMin} = (\sqrt{2} \bullet V_{ACmax} + V_O + \Delta V_{OVP}) \bullet 1.1 = (375V + 200V + 40V) \bullet 1.1 = 677V$$

To avoid large heat sink, the RMS value of the through current suggests using a MOSFET with an R_{DSON} not greater than 1.5 Ω The selected MOSFET, the STP9NK70, has a maximum R_{DSON} of 1.2 Ω at 25 °C and a breakdown voltage of 700 V.

2.3 Diode D1 selection

The average value of the diode D1 current is the output current . The RMS value of the current flowing through diode D1 can be calculated using the following formula:

Equation 36

$$I_{D1RMS} = I_{PK}\sqrt{\frac{1}{3} \bullet \frac{1}{\pi} \bullet \int_0^{\pi} \frac{K_{vmin} \bullet |\sin(\vartheta)|^3}{1 + K_{vmin} \bullet |\sin(\vartheta)|^3} \bullet d\vartheta} = 0.687A$$

The minimum breakdown voltage of diode D1 is the same as for the MOSFET. The selected diode D1, STTH208, has a breakdown voltage of 800 V. When it is forward biased, the voltage drop, (V_d) is 1.05 V and the dynamic resistance(r_d) is 100 mΩ The power dissipation on DI may easily be calculated as follows:

Equation 37

$$P_{D1Loss} = V_d \bullet I_O + r_d \bullet I^2_{D1RMS} = 0.388W$$

2.4 Capacitor C1 selection

The equivalent inductance L_e must be calculated, using *Equation 38* and knowing the minimum switching frequency, the output power, and the efficiency from previous electrical specifications:

Equation 38

$$L_e = \frac{\eta \bullet V^2_{ACMIN(RMS)} \bullet F(k_{vmin})}{P_O \bullet f_{swmin} \bullet (1 + k_{vmin})} = 1041mH \cong 1mH$$

The value of capacitor C1 may be selected by imposing the maximum voltage ripple across it. Considering a maximum voltage ripple of 15 V

$\Delta V_{C1MAX} = 15V$ and using *Equation 21*, the following formula may be calculated:

Equation 39

$$C_1 = \frac{L_e}{\Delta V_{C1MAX}} \bullet \frac{I_{PK}^2}{2} \bullet \frac{1}{(V_O + \sqrt{2} \bullet V_{acmin})} = 416nF$$

A 470 nF capacitor was selected.

It is important to note that the voltage ripple on capacitor C1 will affect the ripple steering effect.

The difference between the voltages across the two inductors, either when the MOSFET is on or off, is the difference between the voltage on capacitor C1 and the input voltage, which effectively is the switching frequency voltage ripple, across capacitor C1.

Because of this ripple, the two inductors do not have exactly the same voltage. Even when *Equation 26* is perfectly satisfied, the current ripple on the input inductor L2 is not zero.

2.5 Output capacitor C2 selection

The output diode current, averaged over each switching cycle, is given in *Equation 29*. The graph of this waveform is shown in *Figure 11* The quantity of electrical charge that goes into capacitor C2 is the same as the integral of the diode current:

Equation 40

$$C_2 \bullet V_O(\vartheta) = X(\vartheta) = \int_0^{\vartheta} I_{D1}(\alpha) \bullet d\alpha$$

Under steady state conditions, the output voltage is maximum and minimum at the two points where $I_{D1}(\theta)$ equals the output current I_O. Letting these angles be $\theta 1$ and $\theta 2$, the minimum output capacitor value that guarantees an output voltage ripple lower than the specified ΔV_O is:

Equation 41

$$C_2 = \frac{|X(\vartheta_1) - X(\vartheta_2)|}{2 \bullet \pi \bullet f_L \bullet \Delta V_O}$$

2.6 Transformer design

The selected magnetic core is an ETD29 made with N67 material. The effective area (A_e) of this core is 0.76 cm^2. Once the core is selected, the minimum turn number, which prevents the transformer from saturation or overheating, may be calculated using the formula:

Equation 42

$$N2_{min} = \frac{V_{in} \bullet T_{ON}}{A_e \bullet \Delta B}$$

The maximum magnetic swing (ΔB) selected is 0.25 T. In the current design the number of turns for the inductor L2 is 125.

If the ripple steering condition is satisfied, *Equation 43* (below) may be calculated using *Equation 24*:

Equation 43

$$L_e = \left(\frac{1}{L_{EQ1}} + \frac{1}{L_{EQ2}}\right)^{-1} = L_{LK1} + L_M = L_{OP1}$$

It may be used to select the proper air gap, where L_{OP1} is the inductance measured at the primary side with the secondary side open. Selecting the correct turn ratio to meet the ripple steering condition for an actual transformer (rather than a theoretical one) is not easy, as the internal parameters of the transformer (L_M and L_{LK1}) are unknown. *Equation 44* is equivalent to *Equation 26* but is based on measurable quantities. L_{SH1} and L_{OP1} are the primary inductances, measured when the secondary side is shorted and when the secondary side is open, respectively.

Equation 44

$$n = \sqrt{\frac{L_{OP1}}{L_{OP1} - L_{SH1}}}$$

Equation 44 is obtained using the hypothesis expressed in *Equation 45*:

Equation 45

$$L_{LK1} = \frac{1}{n^2} \bullet L_{LK2}$$

Equation 45 is generally true if the transformer has a ‘symmetrical structure’. *Figure 12* shows two examples of transformers with a symmetrical structure. A slotted transformer (*Figure 12* b) is used in the board for the current document. The selected turn ratio (n) is 1.28, which gives a value of 98 turns for the inductor L1.

2.7 Selection of other components

Selection of the other components of the circuit may be made using the guidelines for a boost converter which are given in [*2*]. Capacitor C1 must be considered in parallel with the input capacitor, which means that a small capacitor of 10 nF is adequate for the current design.

For the control loop design the procedure used for a boost converter in [*4*] may be followed. The small signal model developed in this document must be considered.

The charge pump which supplies the IC, while respecting the calculated steady state values, needs to be a little over-sized. During start-up, capacitor C2 is not pre-charged by the inrush current as in a boost converter, and therefore, the charge pump provides less current. In order not to have too big a charge pump, the capacitor on the V_{CC} pin of the L6562 has to be increased during start up phase to supply the IC, even if the charge pump is not able to provide enough current.

Figure 11. Output diode current averaged over the switching cycles

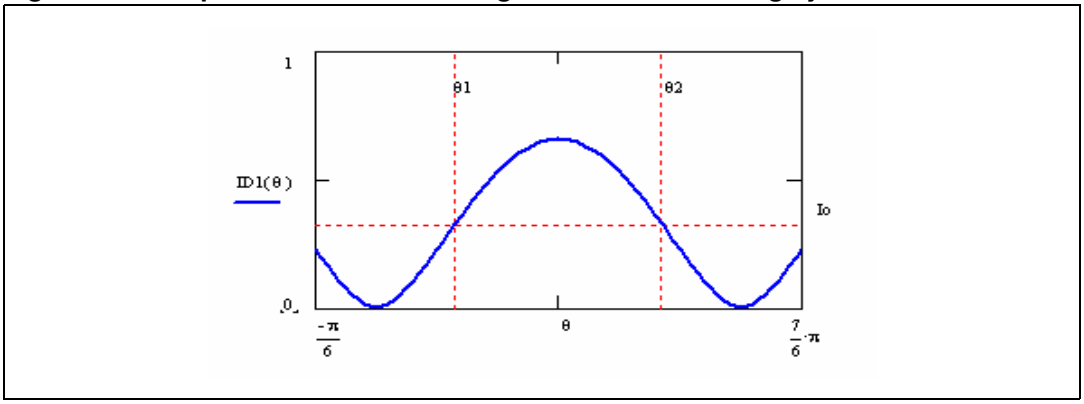
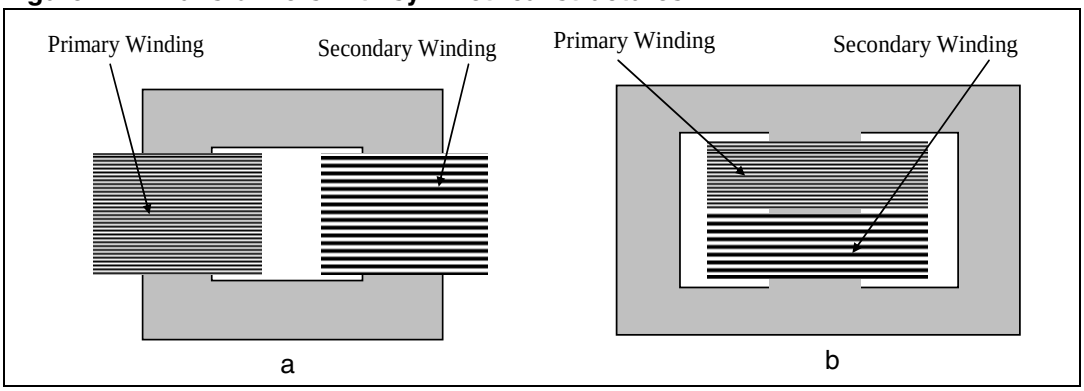


Figure 12. Transformers with symmetrical structures



3 Conclusion

This document presented the sepic converter operating in transition mode for power factor correction applications. The ripple steering technique was also presented. The basic theory behind the sepic converter and the ripple steering technique was discussed and design equations were outlined. An example of a design was proposed.

3.1 References

1. Analysis and design of SEPIC converter in boundary conduction mode for universal-line power factor correction applications. From Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual.
2. L6561, enhanced transition mode power factor corrector (AN966).
3. Minimize filtering with ripple steering. Published in Analog Zone.
4. Control loop modeling of L6561-based TM PFC (AN1089)
5. Transition-mode PFC controller (L6562 datasheet)

4 Board description and bench evaluation results

4.1 Board description

This section gives the bill of material and the schematic of the board according to the electrical specifications given in *Section 2*.

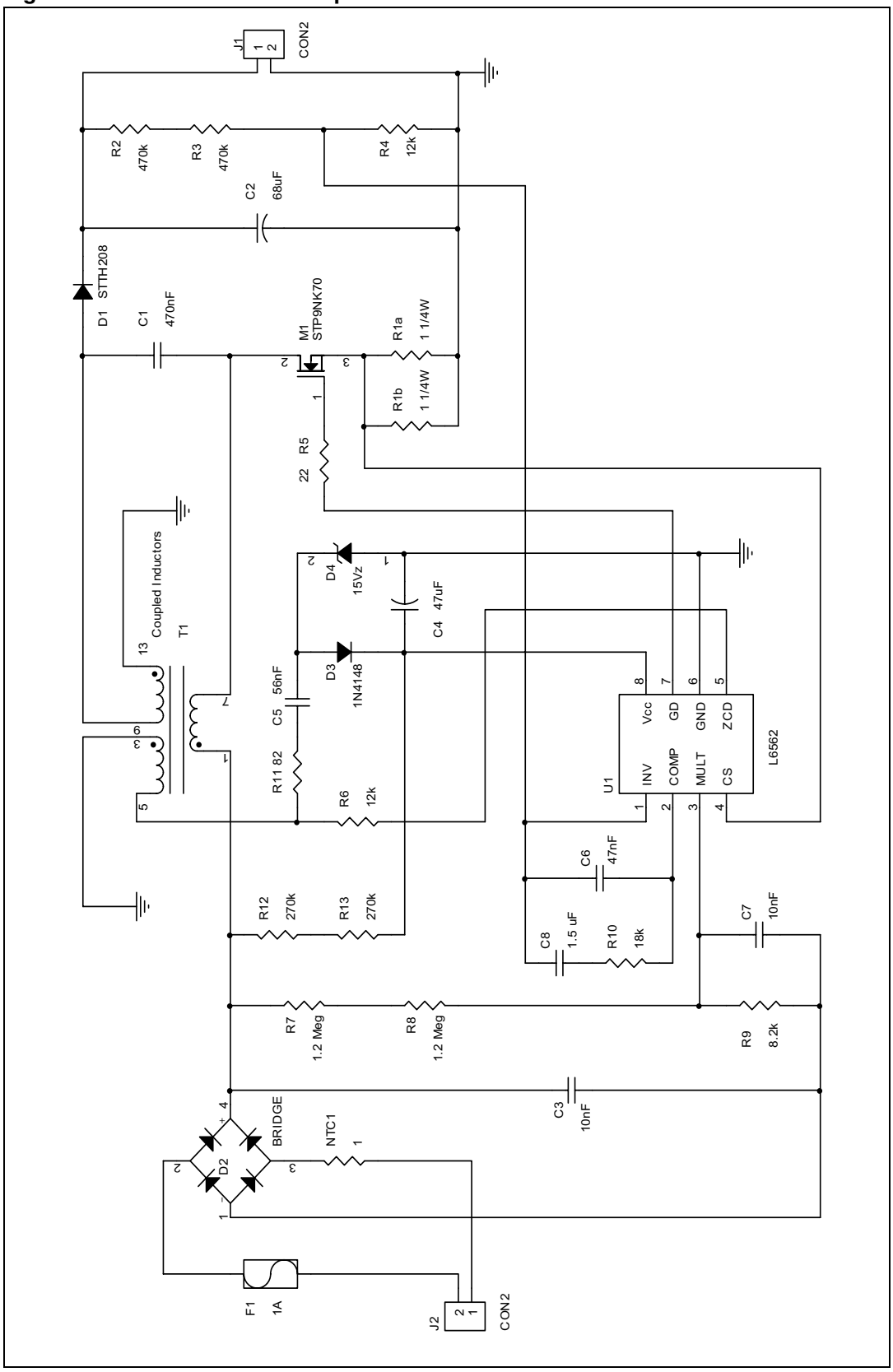
Table 2. Bill of material

Part	Value	Description
C1	470 nF	630 V capacitor
C2	68 µF	250 V electrolitic capacitor
C3	10 nF	X2 type capacitor
C4	47 µF	25V electrolitic capacitor
C5	56 nF	100 V capacitor
C6	47 nF	Samll signal capacitor
C7	10 nF	Small signal capacitor
C8	1.5 µF	Small signal capacitor
D1	STTH208	STMicroelectronics high voltage ultrafast rectifier
D2	BRIDGE	600 V, 1 A standard bridge diode
D3	1N4148	Standard diode
D4	15 Vz	15 V zener diode
F1	1 A	1 A fuse

Table 2. Bill of material (continued)

Part	Value	Description
NTC1	1	1 Ohm NTC
Q1	STP9NK70	STMicroelectronics N-Channel 700 V supermesh^{tm} power MOSFET
R1a, R1b	1 Ohm	1 % precision resistor
R2, R3	470 Kohm	1 % precision resistor
R4	12 Kohm	1 % precision resistor
R5	22 Ohm	Resistor
R6	12 Kohm	Resistor
R7, R8	1.2 Megaohm	Resistor
R9	8.2 Kohm	Resistor
R10	18 Kohm	Resistor
R11	82 Ohm	Resistor
R13,R12	270 Kohm	Resistor
T1	Coupled inductors	
U1	L6562	Transition mode PFC controller

Figure 13. Schematic of the sepic converter



4.2 Bench results

The diagrams in this section summarize the results of certain bench evaluations. They also show waveforms under different load and line conditions.

Figure 14 illustrates the measured efficiency for different loads (65 W, 38 W and 22 W of output power) versus the input ac voltage.

Figure 15 demonstrates the MOSFET drain voltage (Ch4), the output voltage (Ch3) and the input voltage.

The quantities that indicate the quality of the input current as power factor, THD (Total Harmonic Distortion) and crest factor, where measured at full load and for different input voltages. They are reported in *Table 3*.

Figure 16 to *Figure 19* show the currents flowing in the two inductors (Ch1: L1 current; Ch2: L2 current) for different load conditions. Letting the input voltage of the converter (the rectified main) be a perfect rectified sinusoid, it may be used as a reference and is shown as Ch4 in the above figures.

Figure 20 illustrates the input current (Ch1) measured before the input bridge diodes. The voltage at the input of the bridge diodes (Ch4) is also shown as a reference.

Figure 20 is input current at full load (65 W) with 230 V_{ac} as input voltage. *Figure 21* is input current at half load (32 W) with 230 V_{ac} as input voltage.

Table 3. Input current quality measurements

P_{out} = 65 W			
Input voltage (V_{RMS})	**PFC**	**THD %**	**Crest factor**
175	0.992	10.3	1.35
220	0.986	12.3	1.36
230	0.984	12.6	1.37
265	0.975	14.2	1.46

Figure 14. Efficiency chart

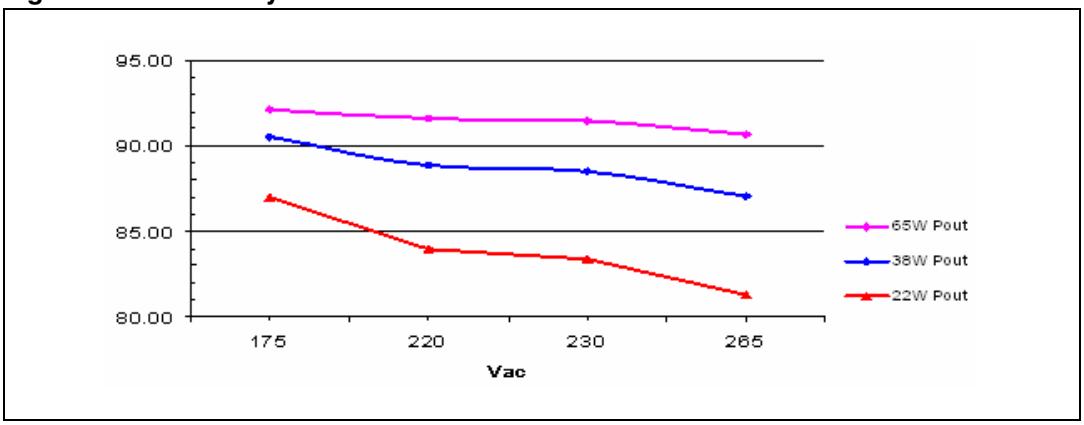
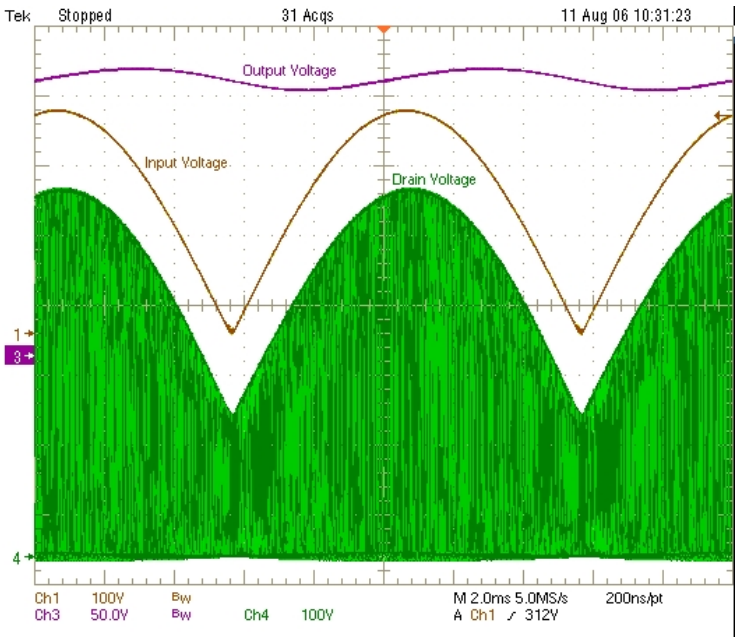


Figure 15. Main waveform of the circuit



1. Test conditions include P_{out} = 65 W and V_{in} = 230 V_{ACRMS}.

Figure 16. Current of the inductors over one line cycle: V_{in} = 230 V_{ACRMS}, P_{out} = 65 W

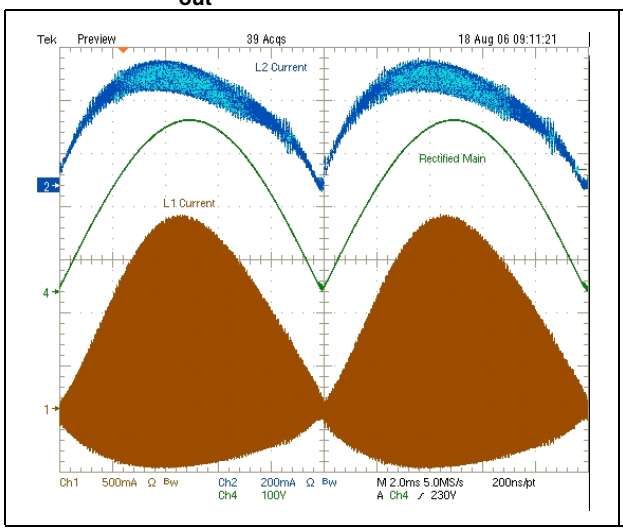


Figure 17. Current of the inductors over switching cycles: V_{in} = 230 V_{ACRMS}, P_{out} = 65 W

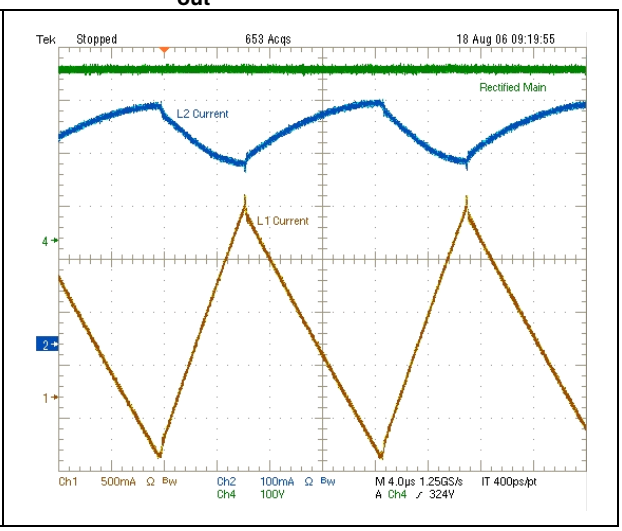


Figure 18. Current of the inductors over one line cycle: V_{in} = 230 V_{ACRMS}, P_{out} = 65 W

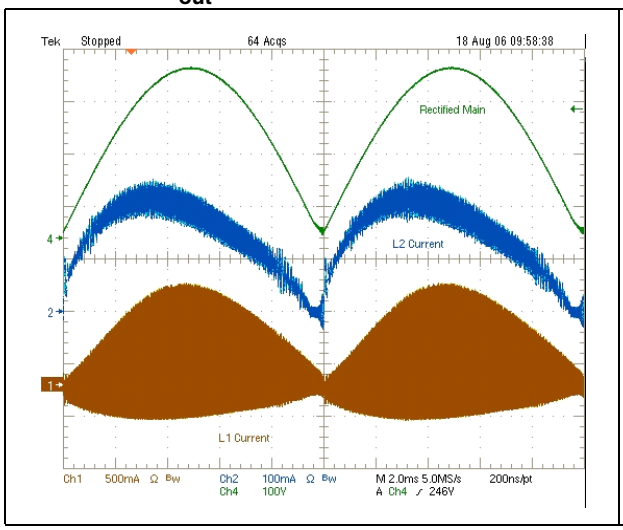


Figure 19. Currents of the inductors over switching cycles: V_{in} = 230 V_{ACRMS}, P_{out} = 65 W

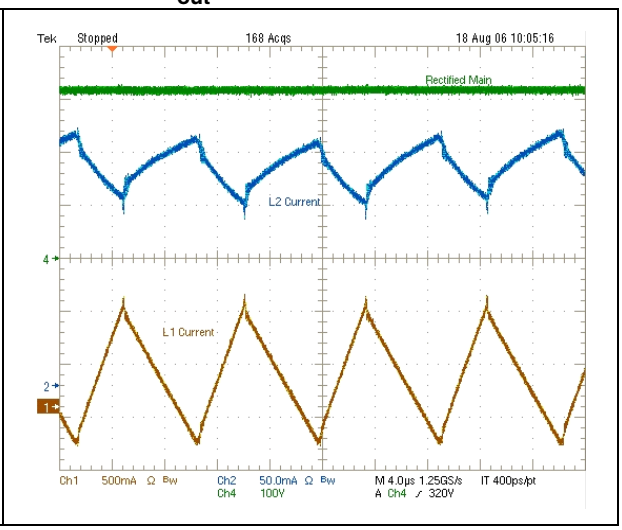


Figure 20. Input current: 230 V_{ac} input, 65 W output

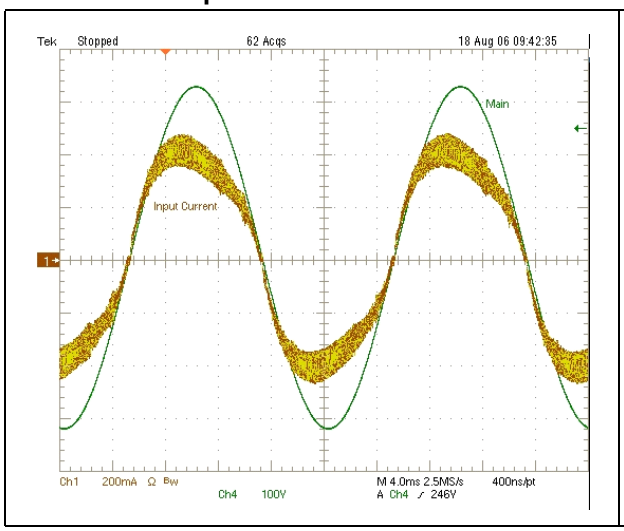
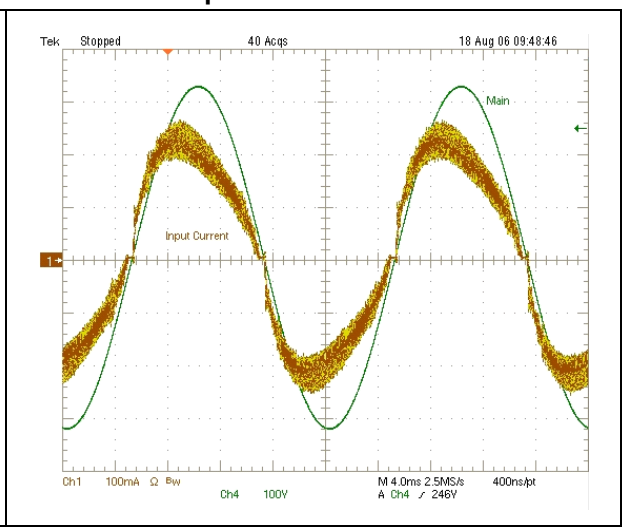


Figure 21. Input current: 230 V_{ac} input, 32 W output



5 Revision history

Table 4. Revision history

Date	Revision	Changes
05-Mar-2007	1	First issue