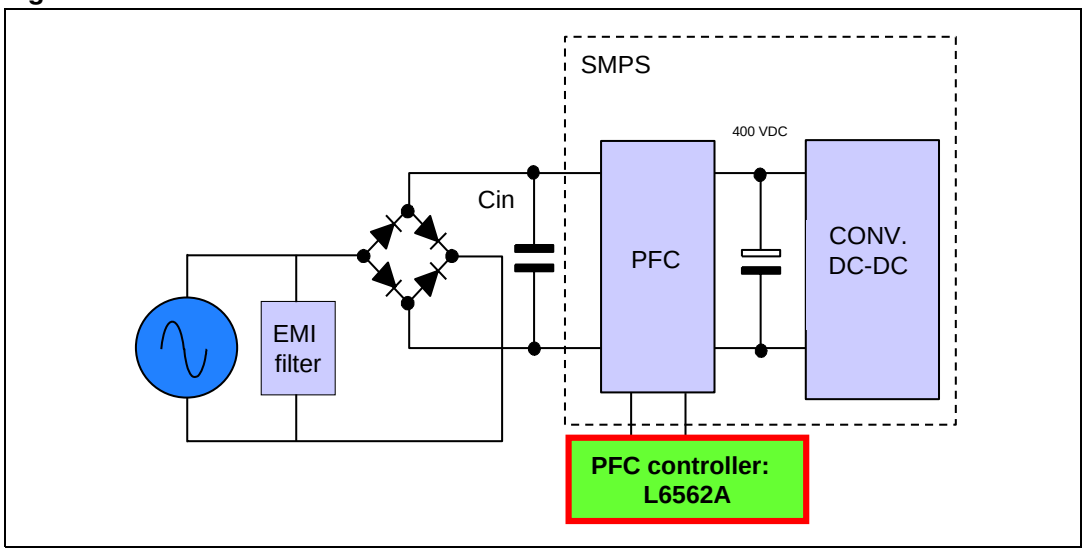
AN2761
Application note

Solution for designing a transition mode PFC preregulator with the L6562A

Introduction

The TM (transition mode) technique is widely used for power factor correction in low and middle power applications, such as lamp ballasts, high-end adapters, flat TVs and monitors, and PC power supplies. The L6562A is the latest proposal from STMicroelectronics for this market as well as emerging markets that may require a low-cost power factor correction. Based on a well-established architecture, the L6562A offers excellent performance that considerably enlarges its field of application.

Figure 1. L6562A PFC controller in an SMPS architecture



Contents

List of figures

1 Introduction to power factor correction

The front-end stage of conventional offline converters, typically consisting of a full-wave rectifier bridge with a capacitor filter, has an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level. This means that the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line half-cycle. The current drawn from the mains is then a series of narrow pulses whose amplitude is 5-10 times higher than the resulting DC value. Many drawbacks result such as a much higher peak and RMS current down from the line, distortion of the AC line voltage, overcurrents in the neutral line of the three-phase systems and, consequently, a poor utilization of the power system's energy capability. This can be measured in terms of either total harmonic distortion (THD), as norms provide for, or power factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage times RMS line current) drawn from the mains, which is more immediate. A traditional input stage with capacitive filter has a low PF (0.5-0.7) and a high THD (>100%). By using switching techniques, a power factor corrector (PFC) preregulator, located between the rectifier bridge and the filter capacitor, allows drawing a quasi-sinusoidal current from the mains, in phase with the line voltage. The PF becomes very close to 1 (more than 0.99 is possible) and the previously mentioned drawbacks are eliminated. Theoretically, any switching topology can be used to achieve a high PF but, in practice, the boost topology has become the most popular thanks to the advantages it offers:

- primarily because the circuit requires the fewest external parts (low-cost solution)
- the boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter
- the switch is source-grounded, therefore easy to drive

However, boost topology requires the DC output voltage to be higher than the maximum expected line peak voltage (400 VDC is a typical value for 230 V or wide-range mains applications). In addition, there is no isolation between the input and output, thus any line voltage surge is passed on to the output. Two methods of controlling a PFC preregulator are currently widely used: the fixed frequency average current mode PWM (FF PWM) and the transition mode (TM) PWM (fixed ON-time, variable frequency). The first method needs a complex control that requires a sophisticated controller IC (ST's L4981A, with the variant of the frequency modulation offered by the L4981B) and a considerable component count. The second one requires a simpler control (implemented by ST's L6562A), much fewer external parts and is therefore much less expensive. With the first method the boost inductor works in continuous conduction mode, while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given throughput power, TM operation involves higher peak currents. This, also consistently with cost considerations, suggests its use in a lower power range (typically below 200 W), while the former is recommended for higher power levels. For completion, FF PWM is not the only alternative when CCM operation is desired. FF PWM modulates both switch ON and OFF times (their sum is constant by definition), and a given converter operates in either CCM or DCM depending on the input voltage and the load conditions. Exactly the same result can be achieved if the ON-time only is modulated and the OFF-time is kept constant, in which case, however, the switching frequency is no longer fixed. This is referred to as "fixed-OFF-time" (FOT) control. Peak-current-mode control can still be used. In this application note transition mode is studied in depth.

2 TM PFC operation (boost topology)

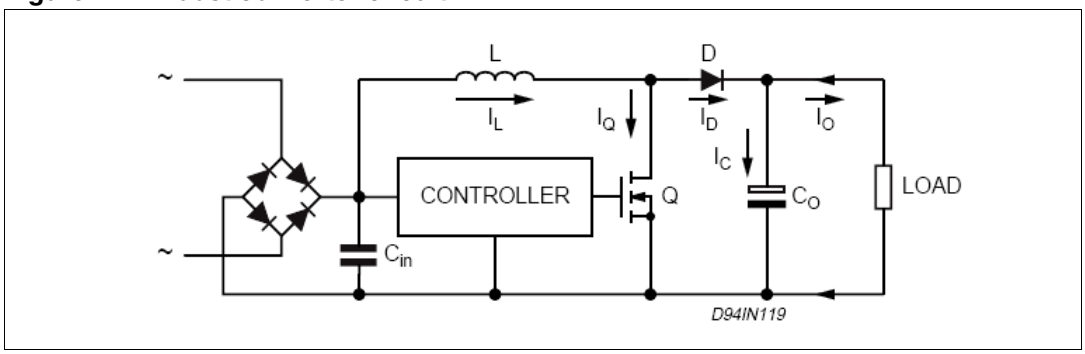
The operation of the PFC transition mode controlled boost converter, can be summarized in the following description.

The AC mains voltage is rectified by a bridge and the rectified voltage is delivered to the boost converter. This, using a switching technique, boosts the rectified input voltage to a regulated DC output voltage (Vo).

The boost converter consists of a boost inductor (L), a controlled power switch (Q), a catch diode (D), an output capacitor (Co) and, obviously, a control circuitry (see *Figure 2*).

The goal is to shape the input current in a sinusoidal fashion, in phase with the input sinusoidal voltage. To do this the L6562A uses the transition mode technique.

Figure 2. Boost converter circuit



The error amplifier compares a partition of the output voltage of the boost converter with an internal reference, generating an error signal proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (below 20 Hz), the error signal is a DC value over a given half-cycle.

The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result is a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal.

The output of the multiplier is in turn fed into the (+) input of the current comparator, thus it represents a sinusoidal reference for PWM. In fact, as the voltage on the current sense pin (instantaneous inductor current times the sense resistor) equals the value on the (+) of the current comparator, the conduction of the MOSFET is terminated. As a consequence, the peak inductor current is enveloped by a rectified sinusoid. As demonstrated in *Section 3.3.4*, TM control causes a constant ON-time operation over each line half-cycle.

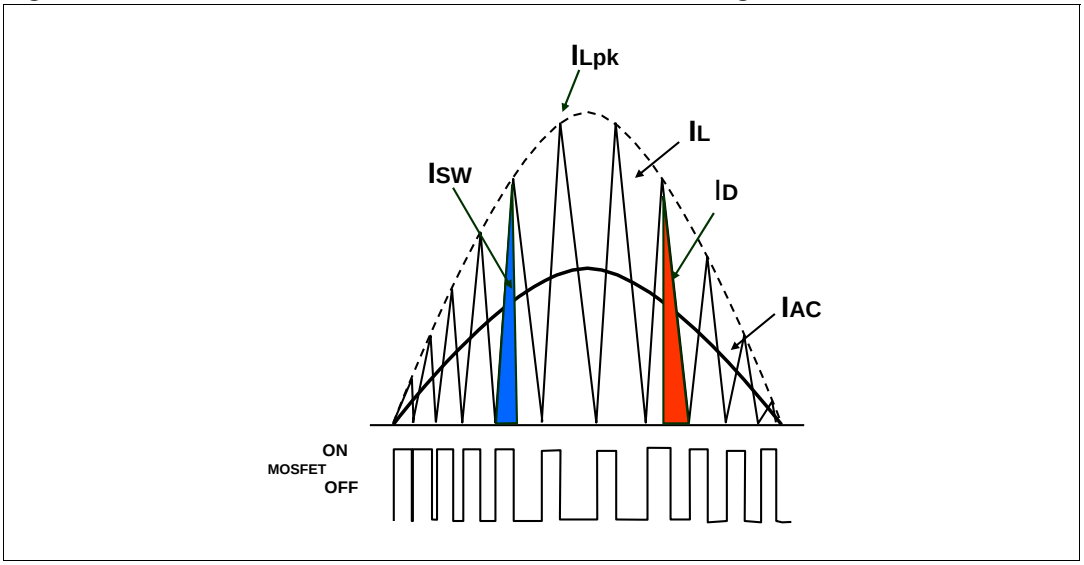
After the MOSFET has been turned off, the boost inductor discharges its energy into the load until its current goes to zero. The boost inductor has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain. The drain voltage drops rapidly below the instantaneous line voltage and the signal on ZCD drives the MOSFET on again and another conversion cycle starts.

This low voltage across the MOSFET at turn-on reduces both the switching losses and the total drain capacitance energy that is dissipated inside the MOSFET.

The resulting inductor current and the timing intervals of the MOSFET are shown in *Figure 3*, where it is also shown that, by geometric relationships, the average input current

(the one which is drawn from the mains) is just one-half of the peak inductor current waveform.

Figure 3. Inductor current waveform and MOSFET timing



The system operates not exactly on, but very close to, the boundary between continuous and discontinuous current mode and that is why this system is called a transition mode PFC.

Besides the simplicity and the few external parts required, this system minimizes the inductor size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified main bus, which needs a heavier EMI filter to be rejected. These drawbacks limit the use of the TM PFC to lower power range applications.

3 Designing a TM PFC

3.1 Input specification

The following is a possible design flowchart in reference to a transition mode PFC, using the L6562A. This first part is a detailed specification of the operating conditions of the circuit that is needed for the following calculation. In this example a 80 W, wide input range mains PFC circuit has been considered. Some design criteria are also given.

- Mains voltage range (Vac rms):

$$VAC_{min} = 85Vac \quad (1)$$

$$VAC_{max} = 265Vac$$

- Minimum mains frequency:

$$f_l = 47\,Hz \quad (2)$$

- Rated output power (W):

$$P_{out} = 80\,W \quad (3)$$

Because the PFC is a boost topology the regulated output voltage depends strongly on the maximum AC input voltage. In fact, for boost correct operation the output voltage must always be higher than the input and thus, because the Vin max is $VAC_{max} \cdot \sqrt{2} = 374\ V_{pk}$, the output has been set at 400 Vdc as the typical value. If the input voltage is higher, as typical in ballast applications, the output voltage must be set higher accordingly. As a rule of thumb the output voltage must be set 6/7% higher than the maximum input voltage peak.

- Regulated DC output voltage (Vdc):

$$V_{out} = 400\ V \quad (4)$$

The target efficiency and PF are set here at minimum input voltage and maximum load. They are used for the following operating condition calculations of the PFC. Of course at high input voltage the efficiency is higher.

- Expected efficiency (%):

$$\eta = \frac{P_{out}}{P_{in}} = 93\% \quad (5)$$

- Expected power factor:

$$PF = 0.99 \quad (6)$$

Because of the narrow loop voltage bandwidth, the PFC output can face overvoltages at startup or in case of load transients. To prevent from excessive output voltage that can overstress the output components and the load, the L6562A integrates an OVP. The overvoltage protection sets the extra voltage overimposed at Vout:

- Maximum output overvoltage (Vdc):

$$\Delta OVP = 55V \quad (7)$$

The mains frequency generates a $2f_L$ voltage ripple on the output voltage at full load. The ripple amplitude determines the current flowing into the output capacitor and the ESR.

Additionally, a certain holdup capability in case of mains dips can be requested of the PFC in which case the output capacitor must also be dimensioned, taking into account the required minimum voltage value ($V_{out\ min}$) after the elapsed holdup time (t_{Hold}),

- Maximum output low-frequency ripple:

$$\Delta V_{out} = 20\ V \quad (8)$$

- Minimum output voltage after line drop (Vdc):

$$V_{out\ min} = 300\ V \quad (9)$$

- Holdup capability (ms):

$$t_{Hold} = 10\ ms \quad (10)$$

The PFC minimum switching frequency is one of the main parameters used to dimension the boost inductor. Here we consider the switching frequency at low mains on the top of the sinusoid and at full load conditions. As a rule of thumb, the switching frequency must be higher than the audio bandwidth in order to avoid audible noise and additionally it must not interfere with the L6562A minimum internal starter period, as given in the datasheet. On the other hand, if the minimum frequency is set too high, the circuit shows excessive losses at a higher input voltage and probably operates skipping switching cycles not only at light load. The typical minimum frequency range is 20÷50 kHz for wide range operation.

- Minimum switching frequency (kHz):

$$f_{sw\ min} = 35\ kHz \quad (11)$$

In order to properly select the power components of the PFC and dimension the heat sinks in case they are needed, the maximum operating ambient temperature around the PFC circuitry must be known. Please note that this is not the maximum external operating temperature of the entire equipment, but it is the local temperature at which the PFC components are working.

- Maximum ambient temperature (°C):

$$T_{ambx} = 50\ °C \quad (12)$$

3.2 Operating condition

The first step is to define the main parameters of the circuit, using the specifications given in *Section 3.1*:

- Rated DC output current:

$$I_{out} = \frac{P_{out}}{V_{out}} \qquad I_{out} = \frac{80\ W}{400\ V} = 0.2\ A \qquad (13)$$

- Maximum input power:

$$P_{in} = \frac{P_{out}}{\eta} \qquad P_{in} = \frac{80\,W}{93} \cdot 100 = 86.02\,W \qquad (14)$$

- RMS input current:

$$I_{in} = \frac{P_{in}}{VAC_{min} \cdot PF} \qquad I_{in} = \frac{86\ W}{85Vac \cdot 0.99} = 1.02A \qquad (15)$$

- Peak inductor current:

$$IL_{pk} = 2 \cdot \sqrt{2} \cdot I_{in} \qquad IL_{pk} = 2 \cdot \sqrt{2} \cdot 1.02A = 2.89A \qquad (16)$$

As shown in *Figure 3*, the inductor current is a triangle shape at switching frequency, and the peak of triangle is twice its average value. The average value of the inductor current is exactly the peak of the input sine wave current, and therefore it can be easily calculated as its rms value is obtained from equation *(15)*. To write down a complete inductor specification for the inductor manufacturer we also provide the RMS and the AC current that can be calculated using equations *(17)* and *(18)*.

- RMS inductor current:

$$IL_{rms} = \frac{2}{\sqrt{3}} \cdot I_{in} \qquad IL_{rms} = \frac{2}{\sqrt{3}} \cdot 1.02A = 1.18A \qquad (17)$$

- AC inductor current:

$$IL_{ac} = \sqrt{IL_{rms}^2 - I_{in}^2} \qquad IL_{ac} = \sqrt{(1.18)^2 - (1.02A)^2} = 0.59A \qquad (18)$$

The current flowing in the inductor can be split in two parts, depending on the instant of conduction. During the on time, the current increases from zero up to the peak value and circulates into the switch, while during the following off-time the current decreases from peak down to zero and circulates into the diode. Therefore there is a current with a triangular wave, with the same peak value equal to the inductor current flowing into these two components. Thus, it is also possible to calculate the RMS current flowing into the switch and into the diode (*Figure 3*), needed to calculate the losses of these two elements.

- RMS switch current:

$$ISW_{rms} = IL_{pk} \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}}$$

$$ISW_{rms} = 2.89A \cdot \sqrt{\frac{1}{6} - \frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{85Vac}{400V}} = 1.01A \quad (19)$$

- RMS diode current:

$$ID_{rms} = IL_{pk} \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{VAC_{min}}{V_{out}}}$$

$$ID_{rms} = 2.89A \cdot \sqrt{\frac{4 \cdot \sqrt{2}}{9\pi} \cdot \frac{85Vac}{400V}} = 0.59A \quad (20)$$

3.3 Power section design

3.3.1 Bridge rectifier

The input rectifier bridge can use standard, slow-recovery, low-cost devices. Typically a 600 V device is selected in order to have good margin against mains surges. An NTC resistor limiting the current at plug-in is required to avoid overstress to the rectifier bridge and fuse.

The rectifier bridge power dissipation can be calculated using equations *(21)*, *(22)*, *(23)*. The threshold voltage and dynamic resistance of a single diode of the bridge can be found in the component datasheet.

$$\bar{I}_{inrms} = \frac{\sqrt{2} \cdot I_{in}}{2} = \frac{\sqrt{2} \cdot 1.02A}{2} = 0.72A \quad (21)$$

$$\bar{I}_{in\_avg} = \frac{\sqrt{2} \cdot I_{in}}{\pi} = \frac{\sqrt{2} \cdot 1.02A}{\pi} = 0.46A \quad (22)$$

The power dissipated on the bridge is:

$$P_{bridge} = 4 \cdot R_{diode} \cdot \bar{I}^2_{inrms} + 4 \cdot V_{th} \cdot \bar{I}_{in\_avg}$$

$$P_{bridge} = 4 \cdot 0.07\Omega \cdot (0.72A)^2 + 4 \cdot 1V \cdot 0.46A = 1.98W \quad (23)$$

3.3.2 Input capacitor

The input high-frequency filter capacitor (Cin) has to attenuate the switching noise due to the high-frequency inductor current ripple (twice the average line current, *Figure 3*).

The worst conditions occur at the peak of the minimum rated input voltage.

The maximum high-frequency voltage ripple across Cin is usually imposed between 5% and 20% of the minimum rated input voltage. This is expressed by a coefficient r (from 0.05 to 0.2) as an input design parameter:

- Ripple voltage coefficient (%):

$$r = 0.2 \quad (24)$$

$$C_{in} = \frac{I_{in}}{2\pi \cdot f_{sw\,min} \cdot r \cdot VAC_{min}} \qquad C_{in} = \frac{1.02A}{2\pi \cdot 35kHz \cdot 0.2 \cdot 85Vac} = 0.26\mu F \quad (25)$$

In real conditions the input capacitance is designed taking the EMI filter into account and a tolerance on the component of about 5% -10% (typical for polyester capacitors).

A commercial value of Cin = 0.22 µF has been selected. Of course a bigger capacitor provides a benefit from the EMI point of view but worsens the THD, especially at high mains. Therefore a compromise must be found between these two parameters. A good quality film capacitor for this component must be selected in order to provide good filtering effectiveness.

3.3.3 Output capacitor

The output bulk capacitor (Co) selection depends on the DC output voltage *(4)*, the allowed overvoltage *(7)* and the converter output power*(3)*.

The 100/120 Hz (twice the mains frequency) voltage ripple (∆Vout = peak-to-peak ripple value) is a function of the capacitor impedance and the peak capacitor current:

$$\Delta V_{out} = 2 \cdot I_{out} \cdot \sqrt{\frac{1}{(2\pi \cdot 2f_l \cdot C_O)^2} + ESR^2} \quad (26)$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

$$C_O \geq \frac{I_{out}}{2\pi \cdot f_l \cdot \Delta V_{out}} = \frac{P_{out}}{2\pi \cdot f_l \cdot V_{out} \cdot \Delta V_{out}} \qquad C_O \geq \frac{80\ W}{2\pi \cdot 47\ Hz \cdot 400\ V \cdot 20V} = 33.8\ \mu F \quad (27)$$

∆Vout is usually selected in the range of 1.5% of the output voltage.

Although ESR usually does not affect the output ripple, it should be taken into account for power loss calculations. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

$$I_{Crms} = \sqrt{ID^2_{rms} - I^2_{out}} \qquad I_{Crms} = \sqrt{(0.59A)^2 - (0.20A)^2} = 0.56A \quad (28)$$

If the PFC stage has to guarantee a specified holdup time, the selection criterion of the capacitance changes. C_O has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage (Vout min) which is the minimum output voltage value (which takes load regulation and output ripple into account). Vout min is the minimum output operating voltage before the 'power fail' detection and consequent stopping by the downstream system supplied by the PFC.

$$C_O = \frac{2 \cdot P_{out} \cdot t_{Hold}}{\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2} \qquad C_O = \frac{2 \cdot 80\,W \cdot 10\,ms}{(400\,V - 20\,V)^2 - (300\,V)^2} = 29.4\,\mu F \qquad (29)$$

A 20% tolerance on the electrolytic capacitors has to be taken into account for the right dimensioning.

Following the relationship *(27)* for this application, a capacitor Co = 47 µF (450 V) has been selected. The actual output voltage ripple with this capacitor is also calculated. In detail:

Holdup capability:

$$t_{hold} = \frac{C_O \cdot \left[\left(V_{out} - \Delta V_{out}\right)^2 - V_{out\,min}^2\right]}{2 \cdot P_{out}} \qquad (30)$$

$$t_{hold} = \frac{47\mu F \cdot \left[(400\,V - 20\,V)^2 - (300\,V)^2\right]}{2 \cdot 80\,W} = 17.43\,ms$$

As expected the ripple variation on the output is:

$$\Delta V_{out} = \frac{I_{out}}{2 \cdot \pi \cdot f_l \cdot C_O} \qquad \Delta V_{out} = \frac{0.20A}{2 \cdot \pi \cdot 47Hz \cdot 47\mu F} = 14.41V \qquad (31)$$

3.3.4 Boost inductor

The boost inductor determines the working frequency of the converter. It is usually calculated so that the minimum switching frequency is greater than the maximum frequency of the L6562A internal starter (190 µs), to ensure a correct TM operation. Assuming unity PF, it is possible to write:

$$t_{on}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{\sqrt{2} \cdot VAC \cdot \sin(\vartheta)} = \frac{L \cdot IL_{pk}}{\sqrt{2} \cdot VAC} \qquad (32)$$

In equation *(32)* it is demonstrated that the ON-time doesn't depend on the mains phase angle but it is constant over the entire mains cycle.

$$t_{off}(VAC, \vartheta) = \frac{L \cdot IL_{pk} \cdot \sin(\vartheta)}{V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\vartheta)} \qquad (33)$$

T_{on} and T_{off} are respectively the ON-time and the OFF-time of the power MOSFET, IL_{pk} is the maximum peak inductor current in a line cycle, and θ is the instantaneous line phase in the interval [0,Π]. Note that the ON-time is constant over a line cycle.

As previously stated, IL_{pk} is twice the line-frequency peak current *(16)*, which is related to the input power and the input mains voltage. Substituting this relationship in the expressions of T_{on} and T_{off}, after some algebra it is possible to find the instantaneous switching frequency along a line cycle:

$$f_{sw}(VAC,\theta) = \frac{1}{T_{on} + T_{off}} = \frac{1}{2 \cdot L \cdot P_{in}} \cdot \frac{VAC^2 \cdot \left(V_{out} - \sqrt{2} \cdot VAC \cdot \sin(\theta)\right)}{V_{out}} \quad (34)$$

The switching frequency is the minimum at the top of the sinusoid ($\theta = \Pi /2$ rad => $\sin \theta = 1$), maximum at the zero-crossings of the line voltage ($\theta = 0$ rad or Π rad=> $\sin \theta = 0$), where T_{off} =0 µs.

The absolute minimum frequency f_{swmin} can occur at either the maximum VAC_{max} or the minimum mains voltage VAC_{min}, thus the inductor value is defined by the formula:

$$L(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot f_{sw\,min} \cdot P_{in} \cdot V_{out}} \quad (35)$$

After calculating the values of the inductor at low mains and at high mains $L(VAC_{max})$, $L(VAC_{min})$ *(35)*, the minimum value has to be taken into account. It becomes the maximum inductance value for the PFC dimensioning.

$$L(VAC_{min}) = \frac{(85Vac)^2 \cdot (400V - \sqrt{2} \cdot 85Vac)}{2 \cdot 35kHz \cdot 86.02W \cdot 400V} = 0.73mH \quad (36)$$

$$L(VAC_{max}) = \frac{(265Vac)^2 \cdot (400V - \sqrt{2} \cdot 265Vac)}{2 \cdot 35kHz \cdot 86.02W \cdot 400V} = 0.83mH \quad (37)$$

For this application a 0.7 mH boost inductance has been selected.

Figure 4. Switching frequency fixing the line voltage

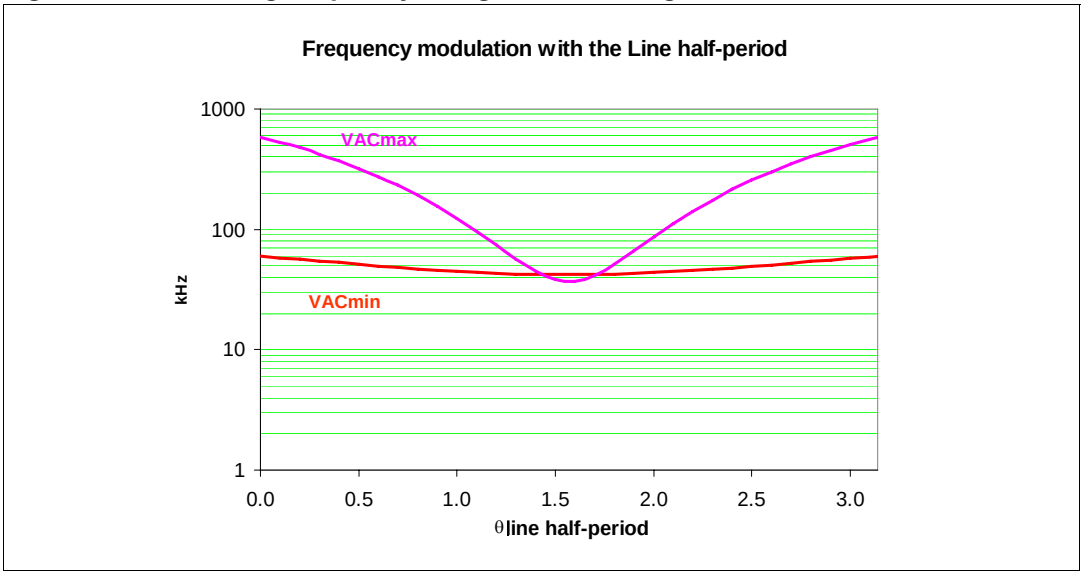


Figure 4 shows the switching frequency versus the θ angle calculated with the *(35)*, a 0.7 mH boost inductance and fixing the line voltage at minimum and maximum values.

The minimum switching frequency can be recalculated for the selected inductance value inverting equation *(35)* as follows:

$$f_{sw\,min}(VAC) = \frac{VAC^2 \cdot (V_{out} - \sqrt{2} \cdot VAC)}{2 \cdot L \cdot P_{in} \cdot V_{out}} \quad (38)$$

From the comparison of the f_{swmin} (VAC_{min}), f_{swmin}(VAC_{max}) with L = 0.7 mH the actual, calculated minimum switching frequency is 37 kHz, as expected.

The core size is determined assuming a peak flux density Bx ≅ 0.25T (depending on ferrite grade selected and relevant specific losses) and calculating the maximum current according to *(58)*, as a function of the maximum current sense pin clamping voltage and sense resistor value.

DC and AC copper losses and ferrite losses must also be calculated to determine the maximum temperature rise of the inductor.

3.3.5 Power MOSFET selection and dissipation

The selection of the MOSFET concerns mainly its $R_{DS(on)}$, which depends on the output power *(3)*, since the breakdown voltage is fixed just by the output voltage *(4)*, plus the over-voltage admitted *(7)* and a safety margin (20%). Thus, a voltage rating of 500 V (1.2 · Vout = 480 V) is selected. Using its current rating as a rule of thumb, we can select a device having ~ 3 times the RMS switch current (19) but the power dissipation calculation gives the final confirmation that the selected device is the right one for the circuit also taking into account the heat sink dimensions. In this 80W TM PFC application an STP8NM50 MOSFET has been selected.

The MOSFET' s power dissipation depends on conduction, switching and capacitive losses.

The conduction losses at maximum load and minimum input voltage are calculated by:

$$P_{cond}(VAC) = RDS_{on} \cdot (ISW_{rms}(VAC))^2 \quad (39)$$

Because normally in the datasheets $R_{DS(on)}$ is given at ambient temperature (25°C) to calculate correctly the conduction losses at 100 °C (typical MOSFET junction operating temperature) a factor of 1.75 to 2 should be taken into account. The exact factor can be found in the device datasheet.

Now, the conduction losses normalized to 1Ω $R_{DS(on)}$ at ambient temperature as a function of P_{in} and VAC can be calculated, combining equations *(39)* and *(19)*:

$$P'_{cond}(VAC) = 2 \cdot (ISW_{rms}(VAC))^2 = 2 \cdot \left(\frac{P_{in}}{\sqrt{2} \cdot VAC \cdot PF} \cdot \sqrt{2 - \frac{16}{3\pi} \cdot \frac{\sqrt{2} \cdot VAC}{V_{out}}} \right)^2 \quad (40)$$

The switching losses in the MOSFET occur only at turnoff because of the TM operation and can be basically expressed by:

$$P_{switch}(VAC) = V_{MOS} \cdot I_{MOS} \cdot t_{fall} \cdot f_{sw}(VAC) \quad (41)$$

(41) represents the crossing between the MOSFET current that decreases linearly during the fall time and the voltage on the MOSFET drain that increases. In fact during the fall time the current of the boost inductor flows into the parasitic capacitance of the MOSFET charging it. For this reason switching losses depend also on the total drain capacitance. Because switching frequency depends on the input line voltage and the phase angle on the sinusoidal waveform, it can be demonstrated that from *(41)* the switching losses per 1 µs of current fall time and 1 nF of total drain capacitance can be written as:

$$P'_{switch}(VAC) = IL_{pk} \cdot V_{out} \cdot \frac{1}{\pi} \int_0^{\pi} (\sin \vartheta)^2 \cdot f_{sw}(VAC, \theta) \cdot d\vartheta \quad (42)$$

The value t_{fall} at turn-off can be found in the MOSFET datasheet.

At turn-on the losses are due to the discharge of the total drain capacitance inside the MOSFET itself.

In general, the capacitive losses are given by:

$$P_{cap}(VAC) = \frac{1}{2} \cdot C_d \cdot V^2_{MOS} \cdot f_{sw}(VAC) \quad (43)$$

where C_d is the total drain capacitance including the MOSFET and the other parasitic capacitances such as the inductor at the drain node, and V_{MOS} is the drain voltage at MOSFET turn-on.

Taking into account the frequency variation with the input line voltage and the phase angle similar to *(43)*, a detailed description of the capacitive losses per 1 nF of total drain capacitance can be calculated as:

$$P'_{cap}(VAC) = \frac{1}{2} \cdot \frac{1}{\pi} \int_{\vartheta_1}^{\vartheta 2} \left(2\sqrt{2}VAC - V_{out}\right)^2 f_{sw}(VAC, \vartheta) \cdot d\vartheta \quad (44)$$

$\theta 1$ and $\theta 2$ depend on input voltage and they are defined as follows:

$$\vartheta_1 = \arcsin\left(\frac{V_{out}}{2\sqrt{2}VAC}\right) \quad (45)$$

$$\vartheta_2 = \pi - \vartheta_1 \quad (46)$$

Figure 5. Transition angle versus input voltage

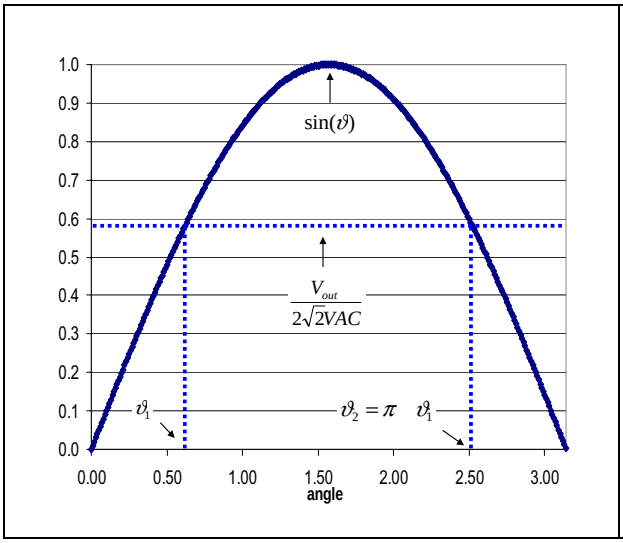
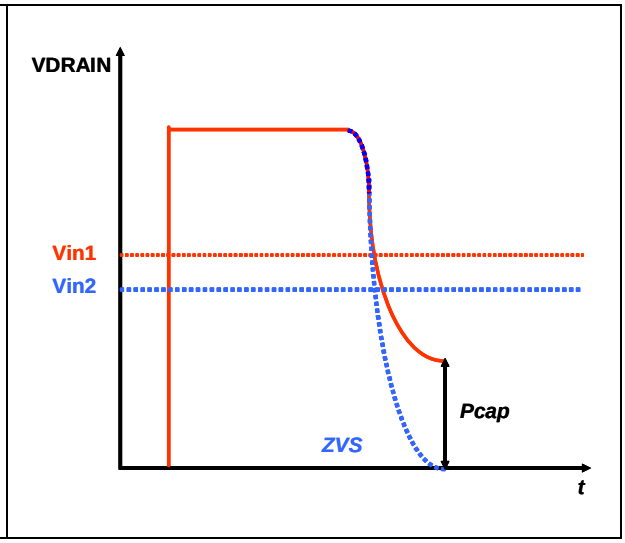


Figure 6. Capacitive losses



The dependence on the input voltage is shown in *Figure 5* and *6*. On the right is represented the drain voltage waveform. The MOSFET turn-on occurs just on the valley because the inductor has depleted its energy and therefore it can resonate with the drain capacitance. The details are in the following ZCD pin description. It is clear that for an input voltage theoretically lower than half of the output voltage the resonance ideally should reach zero achieving zero-voltage operation, therefore there are no losses relevant to this edge. For input voltage corresponding to a positive value of the valley, capacitive losses are not generated. However, the MOSFET turn-on always occurs at the minimum voltage of the resonance and therefore the losses are minimized.

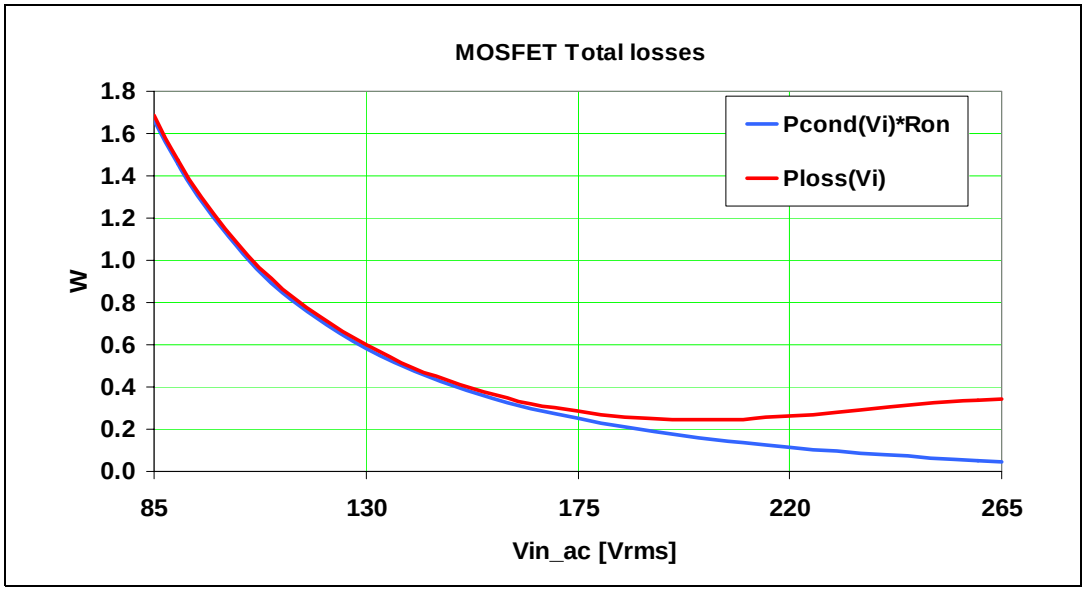
In practice it is possible to estimate the total switching and capacitive losses by solving the integral of the switching frequency depending on sin(θ) on the half-line cycle.

The total loss function of the input mains voltage is the sum of the three previous losses, see equations *(40)*, *(42)* and *(44)* multiplied for the MOSFET parameters:

$$P_{loss}(VAC) = RDS_{on} \cdot P'_{cond}(VAC) + \frac{t_{fall}^2}{C_d} \cdot P'_{sw}(VAC) + C_d \cdot P'_{cap}(VAC) \quad (47)$$

Figure 7 shows the trend of the total losses *(47)* on the line voltage for the selected MOSFET STP8NM50. Capacitive losses are dominant at high mains voltage and the major contribution came from the conduction losses at low and medium mains voltage.

Figure 7. Conduction losses and total losses in the STP8NM50 MOSFET for the 80W TM PFC



From *(47)* using the data relevant to the MOSFET selected, and calculating the losses at VAC_{min} and VAC_{max}, we observe that the maximum total losses occurs at VAC_{min} which is 1.69 W. From this number and the maximum ambient temperature *(12)*, the total maximum thermal resistance required to keep the junction temperature below 125 °C is:

$$R_{th} = \frac{125°C - T_{ambx}}{P_{loss}(VAC)} \qquad R_{th} = \frac{125°C - 50°C}{1.69W} = 44.50\frac{°C}{W} \quad (48)$$

If the result of equation *(48)* is lower than the junction-ambient thermal resistance given in the MOSFET datasheet for the selected device package, a heat sink must be used.

3.3.6 Boost diode selection

Following a similar criterion as that for the MOSFET, the output rectifier can also be selected. A minimum breakdown voltage of 1.2·(Vout + ΔVovp) and a current rating higher than 3·Iout *(13)* can be chosen for a rough initial selection of the rectifier. The correct choice is then confirmed by the thermal calculation. If the diode junction temperature operates

within 125 °C the device has been selected correctly, otherwise a bigger device must be selected.

In this 80 W application an STTH1L06 (600 V, 1 A) has been selected.

The rectifier AVG *(13)* and RMS *(20)* current values and the parameter V_{th} (rectifier threshold voltage) and R_d (dynamic resistance) given in the datasheet allow calculating the rectifier losses.

From the STTH1L06 datasheet, V_{th} is 0.89 V and R_d is 0.165 Ω.

$$P_{diode} = V_{th} \cdot I_{out} + R_d \cdot ID^2_{rms} \qquad P_{diode} = 0.89V \cdot 0.2A + 0.165\Omega \cdot (0.59A)^2 = 0.23W \tag{49}$$

From *(12)* and *(49)* the maximum thermal resistance to keep the junction temperature below 125 °C is then:

$$R_{th} = \frac{125°C - T_{ambx}}{P_{diode}} \qquad R_{th} = \frac{125°C - 50°C}{0.23W} = 317\frac{°C}{W} \tag{50}$$

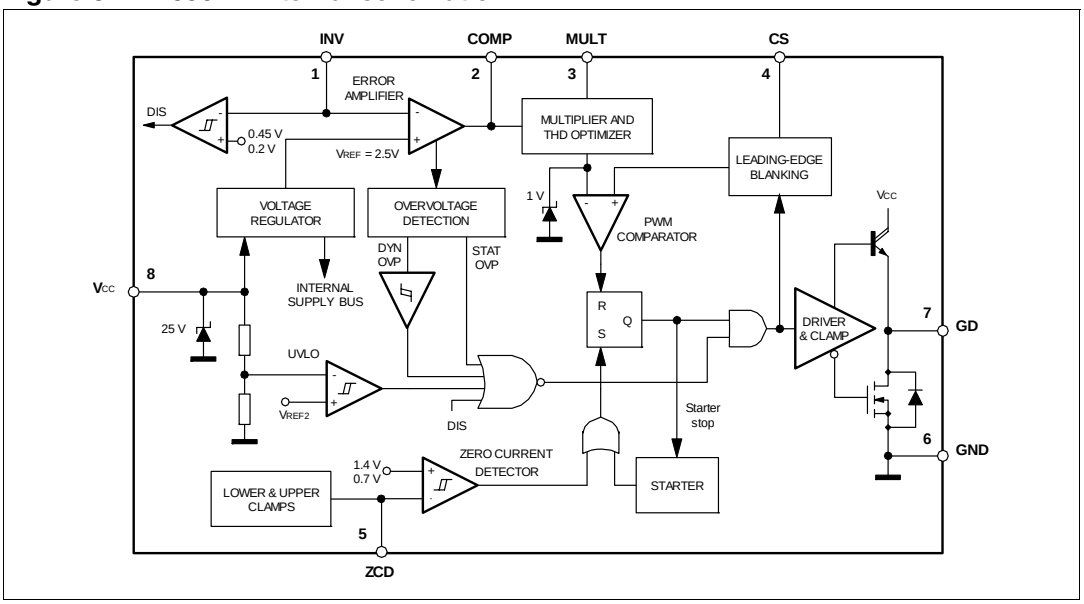
Because the calculated R_{th} is higher than the STTH1L06 thermal resistance junction-ambient, no any heat sink is needed for the rectifier.

3.4 L6562A biasing circuitry

Following the dimensioning of the power components, the biasing circuitry for the L6562A is also described. For reference, the internal schematic of the L6562A is represented below in *Figure 8*.

For more details on the internal function, please refer to the datasheet.

Figure 8. L6562A internal schematic



- Pin 1 (INV): This pin is connected both to the inverting input of the E/A and to the DIS circuitry. A resistive divider is connected between the boost regulated output voltage and this pin. The internal reference on the non-inverting input of the E/A is 2.5 V (typ), while the DIS intervention threshold is 27 µA (typ). R_{outH} and R_{outL} are then selected as follows:

$$R_{outH} = \frac{\Delta V_{OVP}}{27\mu A} \quad R_{outH} = \frac{55V}{27\mu A} = 2.03M\Omega \tag{51}$$

$$\frac{R_{outH}}{R_{outL}} = \frac{V_{out}}{2.5V} - 1 \quad \frac{R_{outH}}{R_{outL}} = \frac{400V}{2.5V} - 1 = 159 \tag{52}$$

$$R_{outL} = \frac{R_{outH}}{159} \quad R_{outL} = \frac{2M\Omega}{159} = 12.6k\Omega \tag{53}$$

The commercial values selected are R_{outH} = 2 MΩ and R_{outL} = 15 kΩ in parallel to a 82 kΩ. Please note that for R_{outH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series have to be used.

This pin can also be used as an ON/OFF control input if tied to GND by an open collector or open drain.

- Pin 2 (COMP): This pin is the output of the E/A that is fed to one of the two inputs of the multiplier. A feedback compensation network is placed between this pin and INV (1). It has to be designed with a narrow bandwidth in order to avoid that the system rejects the output voltage ripple (100 Hz) that would bring high distortion of the input current waveform. A simple criterion to define the capacitance value is to set the bandwidth (BW) from 20 to 30 Hz. The compensation network can be just a capacitor, providing a low-frequency pole as well as a high DC gain. A more complex network, typically a type-II CRC network providing 2 poles and a zero, is more suitable for constant power loads like a downstream converter.

In case a single capacitor is used, it can be dimensioned using the following formulas:

$$BW = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot C_{Compensation}} \tag{54}$$

$$C_{Compensation} = \frac{1}{2\pi \cdot (R_{outH} // R_{outL}) \cdot BW} \tag{55}$$

For a more complex compensation network calculation please refer to [2], [3].

For this 80 W TM PFC, a CRC network providing two poles and a zero has been implemented, using the following values:

$$C_{compP} = 150nF \quad C_{compS} = 2.2\mu F \quad R_{compS} = 22k\Omega \tag{56}$$

to which corresponds the following open-loop transfer function and its phase function.

Figure 9. Bode plot - open-loop transfer function

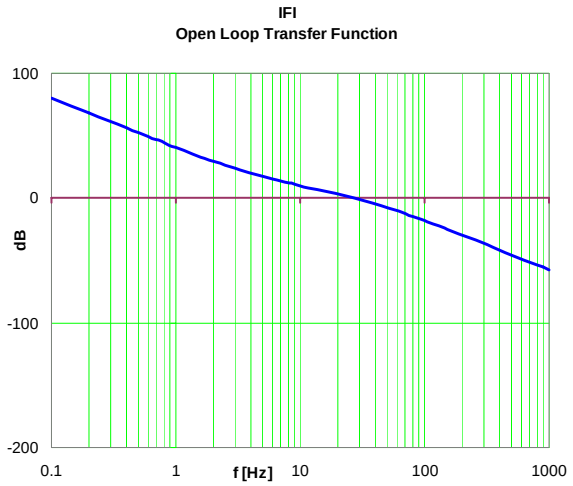
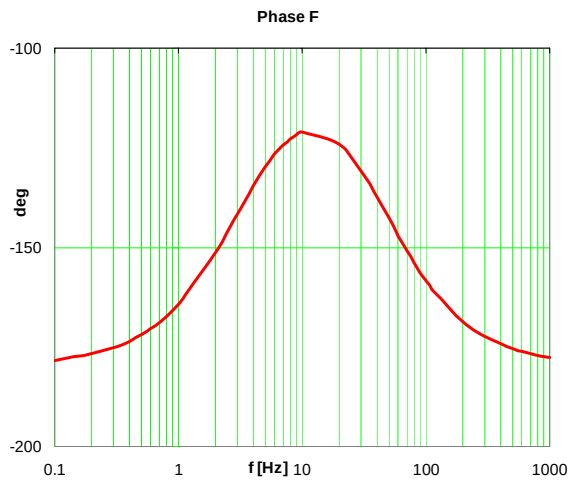


Figure 10. Bode plot - phase



The two Bode plot charts are in reference to the PFC operating at 265Vac and full load (*Figure 9* and *10*). In this condition the crossover frequency is fc = 28 Hz, the phase margin is 55°. The third harmonic distortion introduced by the E/A 100 Hz residual ripple is below 3%.

- Pin 4 (CS): The pin #4 is the inverting input of the current sense comparator. Through this pin, the L6562A senses the instantaneous inductor current, converted to a proportional voltage by an external sense resistor (R_s). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET stays in OFF-state until the PWM latch is reset by the ZCD signal. The pin is equipped with 200 ns leading-edge blanking to improve noise immunity.

The sense resistor value (R_s) can be calculated as follows. For the 80 W PFC it is:

$$R_s < \frac{Vcs_{min}}{IL_{pk}} \qquad R_s < \frac{1.0V}{2.89A} = 0.34\Omega \tag{57}$$

where:

- IL_{pk} is the maximum peak current in the inductor, calculated as described in *(16)*
- Vcs_{min} = 1.0 V is the minimum voltage allowed on the L6562A current sense (in the datasheet)

Because the internal current sense clamping sets the maximum current that can flow in the inductor, the maximum peak of the inductor current is calculated considering the maximum voltage Vcs_{max} allowed on the L6562A (in the datasheet):

$$IL_{pkx} = \frac{Vcs_{max}}{R_s} \qquad IL_{pkx} = \frac{1.16V}{0.34\Omega} = 3.41A \tag{58}$$

The calculated IL_{pkx} is the limit at which the boost inductor saturates and it is used for calculating the inductor number of turns and air gap length.

The power dissipated in R_s is given by:

$$P_s = R_s \cdot ISW_{rms}^2 \qquad P_s = 0.34\Omega \cdot (1.01A)^2 = 0.35W \tag{59}$$

According to the result two parallel resistors of 0.68 Ω with 0.25 W of power rating have been selected.

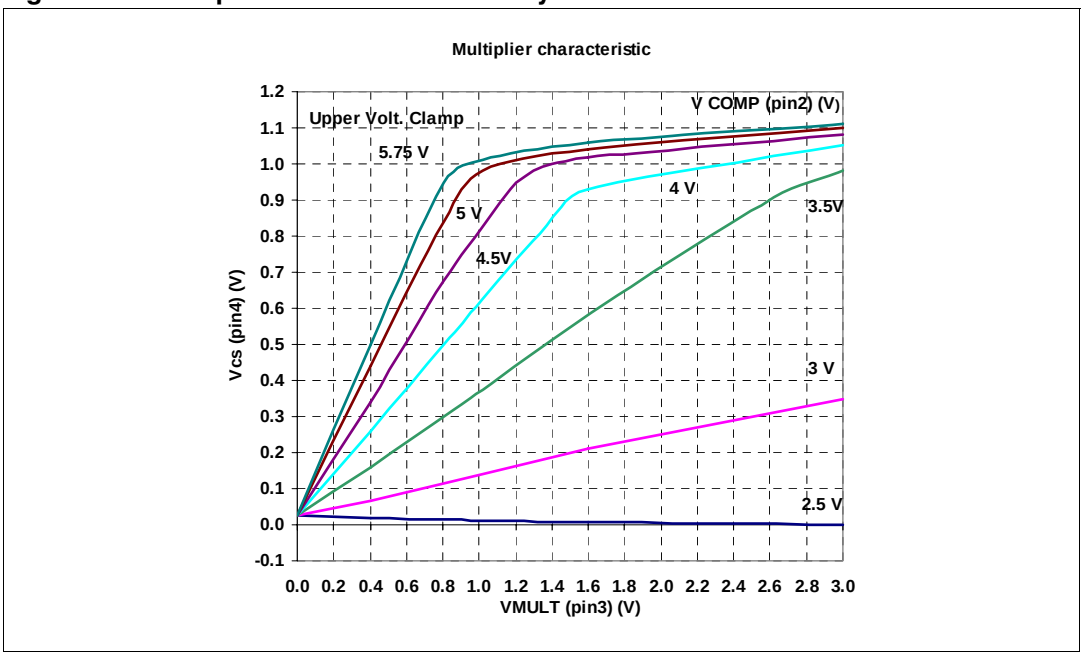
- Pin 3 (MULT): The MULT pin is the second multiplier input. It is connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

$$V_{CS} = k \cdot (V_{COMP} - 2.5V) \cdot V_{MULT} \tag{60}$$

where:

  - V_{CS} (multiplier output) is the reference for the current sense
  - k = 0.38 (typ) is the multiplier gain
  - V_{COMP} is the voltage on pin 2 (E/A output)
  - V_{MULT} is the voltage on pin 3

Figure 11. Multiplier characteristics family



A complete description is given in *Figure 11*, which shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed within the range 0 to 3 V of V_{MULT} and the range 0 to 1.16 V (typ) of V_{cs}, while the minimum guaranteed value of the maximum slope of the characteristics family (typ) is:

$$\frac{dV_{CS}}{dV_{MULT}} = 1.1\frac{V}{V} \quad (61)$$

Taking this into account, the following is the suggested procedure to properly set the operating point of the multiplier.

First, the maximum peak value for V_{MULT}, $V_{MULTmax}$ is selected. This value, which occurs at maximum mains voltage, should be 3 V or nearly so in wide-range mains and less in case of single mains. The sense resistor selected is R_s = 0.34 Ω and it is described in the paragraph concerning pin 4 of this section. The maximum peak value, occurring at maximum mains voltage is:

$$VMULT_{max} = \frac{IL_{pk} \cdot R_s}{1.1} \cdot \frac{VAC_{max}}{VAC_{min}} \qquad VMULT_{max} = \frac{2.89A \cdot 0.34\Omega}{1.1} \cdot \frac{265Vac}{85Vac} = 3.06V \quad (62)$$

where IL_{pk} and R_s have been already calculated, and 1.1 V/V is the multiplier maximum slope reported in the datasheet.

From *(62)* the maximum required divider ratio is calculated as:

$$k_p = \frac{V_{MULTmax}}{\sqrt{2} \cdot VAC_{max}} = \frac{3.06V}{\sqrt{2} \cdot 265Vac} = 8.16 \cdot 10^{-3} \quad (63)$$

Supposing a 200 µA current flowing into the multiplier divider, the lower resistor value can be calculated:

$$R_{multH} = \frac{1-k_p}{k_p} R_{multL} = \frac{1-8.16\cdot10^{-3}}{8.16\cdot10^{-3}} 15k\Omega = 1.85M\Omega \quad (64)$$

In this application example R_{multH} = 2 MΩ and R_{multL} = 15 kΩ have been selected. Please note that for R_{multH} a resistor with a suitable voltage rating (>400 V) is needed, or more resistors in series must be used.

The voltage on the multiplier pin with the selected component values recalculated is 0.89 V at minimum line voltage and is 2.8 V at maximum line voltage. The multiplier works correctly within its linear region.

- Pin 5 (ZCD): Pin #5 is the input of the zero current detector circuit. In transition mode PFC, the ZCD pin is connected, through a limiting resistor, to the auxiliary winding of the boost inductor. The ZCD circuit is negative-going edge triggered. When the voltage on the pin falls below 0.7 V, it sets the PWM latch and the MOSFET is turned on. To do so the circuit must first be armed. Prior to falling below 0.7 V, the voltage on pin 5 must experience a positive-going edge exceeding 1.4 V (due to the MOSFET's turnoff). The maximum main-to-auxiliary winding turn ratio, nmax, has to ensure that the voltage delivered to the pin during the MOSFET's OFF-time is sufficient to arm the ZCD circuit. A safe margin of 15% is added.

$$nmax = \frac{n_{primary}}{n_{auxiliary}} = \frac{V_{out} - \sqrt{2}\cdot VAC_{max}}{1.4V\cdot1.15} \qquad nmax = \frac{400V - \sqrt{2}\cdot265Vac}{1.4V\cdot1.15} = 15.7 \quad (65)$$

If the winding is also used for supplying the IC, the above criterion may not be compatible with the Vcc voltage range. To solve this incompatibility the self-supply network shown in the schematic of *Figure 18* can be used.

The minimum value of the limiting resistor can be found considering the maximum voltage across the auxiliary winding with a selected turn ratio = 10 and assuming 0.8 mA current through the pin.

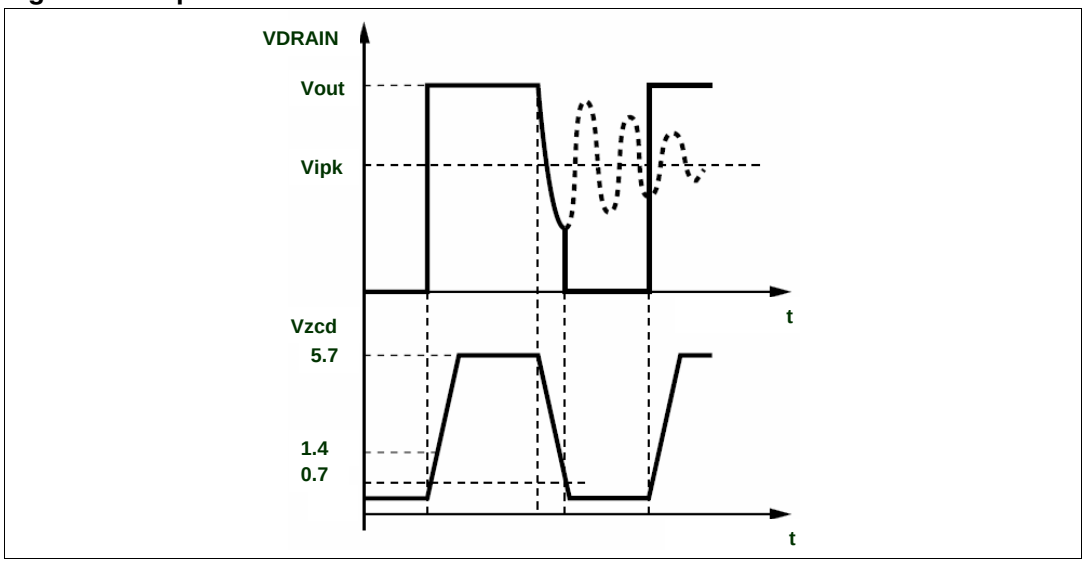
$$R_1 = \frac{\frac{V_{out}}{n_{aux}} - V_{ZCDH}}{0.8mA} \qquad R_1 = \frac{\frac{400V}{10} - 5.7V}{0.8mA} = 42.9k\Omega \quad (66)$$

$$R_2 = \frac{\frac{\sqrt{2}\cdot VAC_{max}}{n_{aux}} - V_{ZCDL}}{0.8mA} \qquad R_2 = \frac{\frac{\sqrt{2}\cdot265Vac}{10} - 0V}{0.8mA} = 46.8k\Omega \quad (67)$$

V_{ZCDH} = 5.7 V and V_{ZCDL} = 0 V are the upper and lower ZCD clamp voltages of the L6562A.

Considering the higher value between the two calculated, R_{ZCD} = 47 kΩ has been selected as the limiting resistor.

Figure 12. Optimum MOSFET turn-on



The actual value can then be tuned trying to make the turn-on of the MOSFET occur just on the valley of the drain voltage (which is resonating because the boost inductor has run out of energy, (*Figure 12*).This minimizes the power dissipation at turn-on.

- Pin 6 (GND): This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When laying out the printed circuit board, these two paths should run separately.
- Pin 7 (GD) is the output of the driver. The pin is able to drive an external MOSFET with 600 mA source and 800 mA sink capability. The high-level voltage of this pin is clamped at about 12 V to avoid excessive gate voltages in case the pin is supplied with a high Vcc. To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the L6562A is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 1.1 V maximum on the pin (at I_{sink} = 2 mA), with Vcc > Vcc_ON. This allows omitting the "bleeder" resistor connected between the gate and the source of the external MOSFET used for this purpose.
- Pin 8 (Vcc) is the supply of the device. This pin is externally connected to the startup circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit. Whatever the configuration of the self-supply system, a capacitor is connected between this pin and ground. To start the L6562A, the voltage must exceed the startup threshold (12.5 V typ). Below this value the device does not work and consumes less than 30 µA (typ) from Vcc. This allows the use of high value startup resistors (in the hundreds kΩ), which reduces power consumption and optimizes system efficiency at low load, especially in wide-range mains applications. When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 3.75 mA. The device keeps on working as long as the supply voltage is over the UVLO threshold (10.5 V max). If the Vcc voltage exceeds 25 V, an internal clamping circuitry, is activated in order to clamp the voltage. Please remember that during normal operation the internal clamp does not have to limit the voltage, in which case the power consumption of the device increases considerably and its junction temperature also increases. The suggested operating condition for safe operation of the device is powering the L6562A with a Vcc below the minimum calmping voltage of pin 8.

4 Design example using the L6562A-TM PFC Excel spreadsheet

An Excel spreadsheet has been developed to allow a quick and easy design of a boost PFC preregulator using the STM L6562A controller, operating in transition mode.

Figure 13 shows the first sheet already precompiled with the input design data used in *Section 3: Designing a TM PFC*.

Figure 13. Excel spreadsheet design specification input table

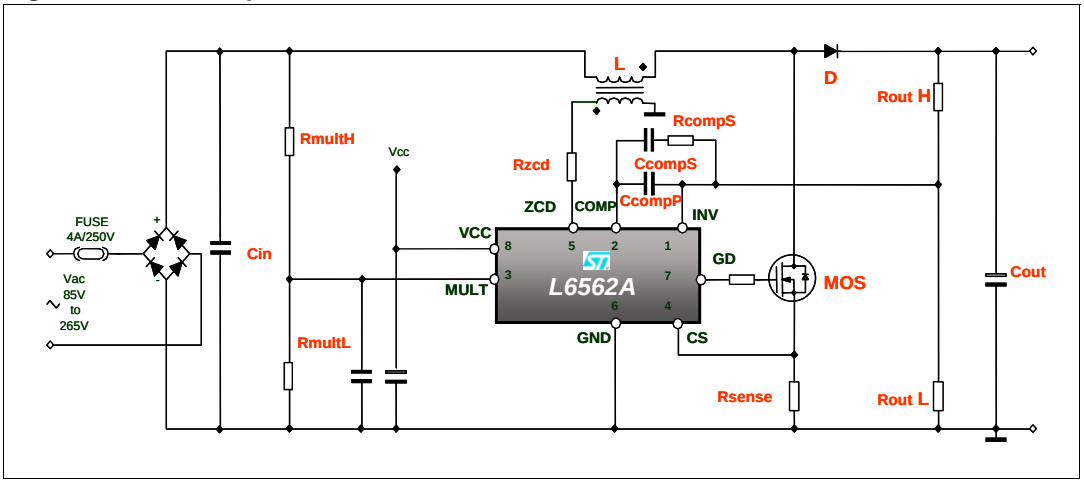
Parameter	Name	Value	Unit [ ]
Mains Voltage Range	VacMin	85	VACrms
Mains Voltage Range	VacMax	265	VACrms
Min.Mains Frequency	fl	47	Hz
Regulated Output Voltage	Vout	400	Vdc
Rated Output Power	Pout	80	W
Max. Output Low Frequency Ripple	Δ Vout	20	Vpk-pk
Max. Output Overvoltage	ΔOVP	55	Vdc
Holdup Capability	Thold	10	ms
Min. Output Voltage after Line drop	VoutMin	300	Vdc
Min. Switching Frequency:	fmin	35	kHz
Expected Efficiency	η	93	%
Expected Power Factor	PF	0.99	---
Maximum Ambient Temperature	Tambx	50	C

Figure 14. Other design data

Parameter	Name	Value	Unit [ ]
Maximum Magnetic Flux Density	Bx	0.25	T
Ripple VoltageCoefficient	r	0.2	---

The tool is able to generate a complete part list of the PFC schematic represented in *Figure 15*, including the power dissipation calculation of the main components.

Figure 15. Excel spreadsheet TM PFC schematic



The bill of material in *Figure 16* is automatically compiled by the Excel spreadsheet. It summarizes all selected components and some salient data.

Figure 16. Excel spreadsheet BOM - 80 W TM PFC based on L6562A

	80W TM PFC BASED ON L6562A			
	BILL OF MATERIAL			
		Selected Value	Unit [ ]	
BRIDGE RECTIFIER	*W08*			
MOSFET P/N	*STP8NM50*			
DIODE P/N	*STTH1L06*			
Inductor	*Lx*	*0.70*	*mH*	
Max peak Inductor current	*Ilpkx*	*3.41*	*A*	
Sense resistor	*Rsx*	*0.34*	*Ω*	
Power dissipation	*Ps*	*0.35*	*W*	
INPUT Capacitor	*Cin*	*0.22*	*µF*	
OUTPUT Capacitor	*Cout*	*47*	*µF*	
MULT Divider	*Rmult L*	*15*	*kΩ*	
	Rmult H	*2000*	*kΩ*	
ZCD Resistor	*Rzcd*	*47*	*kΩ*	
Feedback Divider	*RoutH*	*2000*	*kΩ*	
	RoutL	*12.68*	*kΩ*	
Comp Network	*CcompP*	*150*	*nF*	
	CcompS	*2200*	*nF*	
	RcompS	*22*	*kΩ*	
IC Controller	*L6562A*			

5 EVL6562A-TM-80W demonstration board

Figure 17. EVL6562A-TM-80W demonstration board

Figure 18. Wide range 80W demonstration board electrical circuit (EVL6562A-TM-80W)

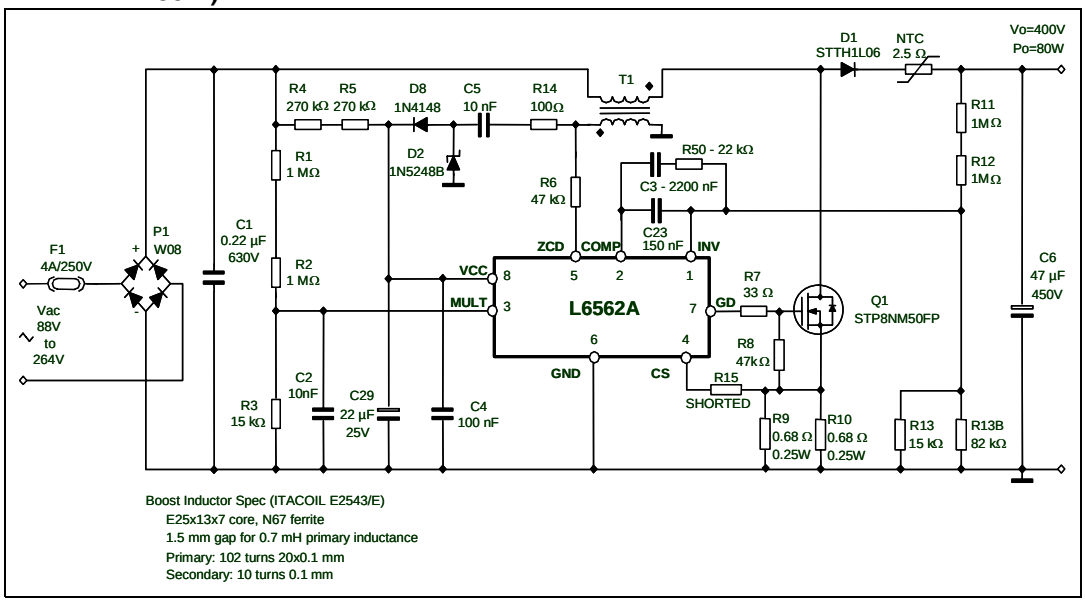


Figure 18 shows the schematic of an application board. It has been dimensioned using the Excel tool presented in *Section 4*.

The board implements a power factor correction (PFC) preregulator delivering 80 W continuous power, on a regulated 400 V rail from a wide-range mains voltage and providing

for the reduction of the mains harmonics, which complies with the European norm EN61000-3-2 or the Japanese norm JEIDA-MITI. This rail is the input for the cascaded isolated DC-DC converter provides the output rails required by the load. The board has been designed to allow full-load operation in still air.

The power stage of the PFC is a conventional boost converter, connected to the output of the rectifier bridge D2. It includes the coil T1, the diode D1 and the capacitor C6. The boost switch is represented by the power MOSFET Q1. The NTC limits the inrush current at plug-in. It has been connected on the DC rail, in series to the output electrolytic capacitor, in order to improve the efficiency during low line operation because the rectifier RMS current is significantly lower than the AC input current at minimum input voltage and maximum load. Even in this position the NTC limits the surge current due to the output electrolytic capacitor as well.

At startup the L6562A is powered by the Vcc capacitor C29 that is charged via the resistors R4 and R5. Then the T1 secondary winding and the charge pump circuit (R14, C5, D2 and D8) generate the Vcc voltage powering the L6562A during normal operations. The divider composed of R1 + R2 and R3 provides the L6562A multiplier with the information of the instantaneous voltage that is used to modulate the boost current. The divider composed of R11 + R12 and R13A in parallel with R13B is dedicated to sense the output voltage.

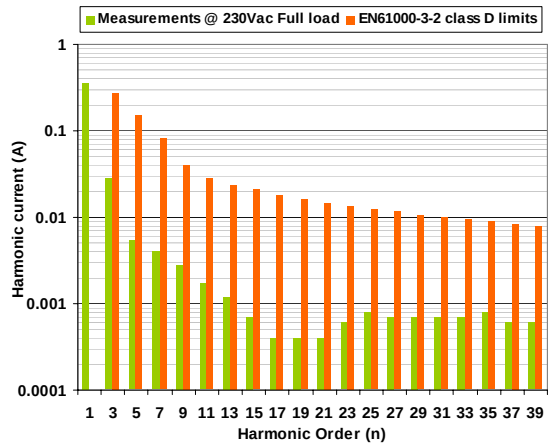
The board is not equipped with an input EMI filter. The filter must be added in the final application circuit by the user.

6 Test results and significant waveforms

One of the main purposes of a PFC preconditioner is the correction of input current distortion, decreasing the harmonic contents below the limits of the relevant regulations. Therefore, this demonstration board has been tested according to the European standard EN61000-3-2 Class-D and Japanese standard JEIDA-MITI Class-D, at full load at both nominal input voltage mains.

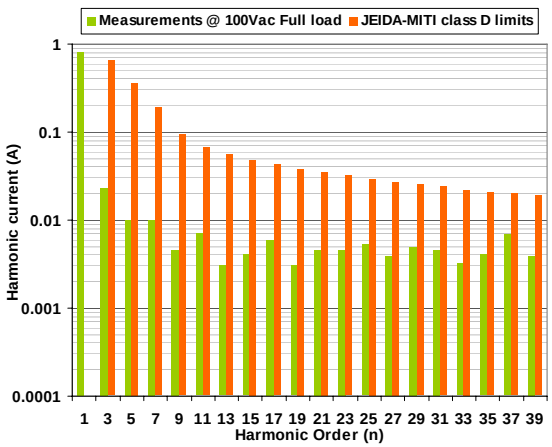
As shown in the following *Figure 19* and *20*, the circuit is able to reduce the harmonics well below the limits of both regulations from full load down to light load. Please note that all measures and waveforms have been done using a Pi-filter for filtering the noise coming from the circuit, using a 25 mH common mode choke and two 220NF-X2 filter capacitors.

Figure 19. EVL6562A-TM-80W compliance to EN61000-3-2 standard



Vin = 230 Vac - 50 Hz, Pout = 80 W
THD = 10.48 %, PF = 0.973

Figure 20. EVL6562A-TM-80W compliance to JEIDA-MITI standard



Vin = 100 Vac - 50 Hz, Pout = 80 W
THD = 3.18 %, PF = 0.997

Figure 21. EVL6562A-TM-80W power factor vs. Vin and load

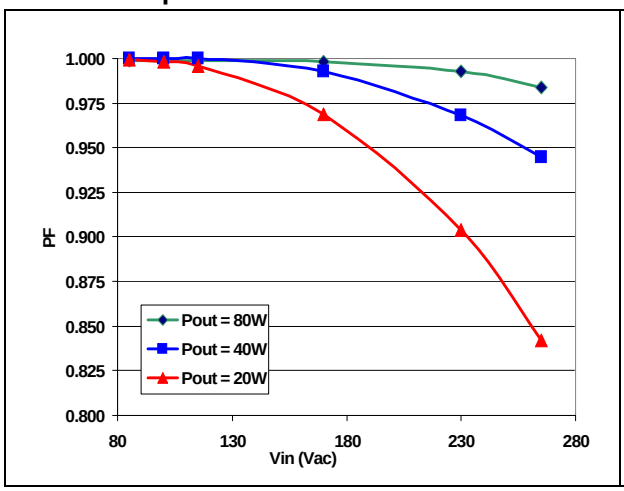
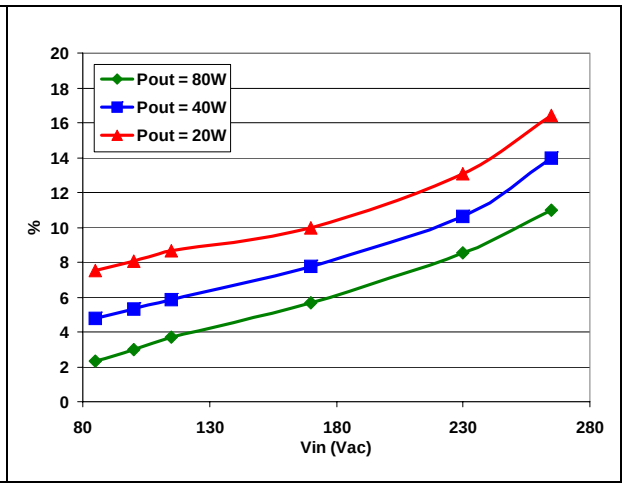


Figure 22. EVL6562A-TM-80W THD vs. Vin and load



The power factor (PF) and the total harmonic distortion (THD) have been measured and are illustrated in *Figure 21* and *22*. As shown, the PF measured at full load and half load remains close to unity throughout the input voltage mains range while, when the circuit is delivering 20 W, it decreases at high mains range. THD is low, remaining within 16% at maximum input voltage.

Figure 23. EVL6562A-TM-80W efficiency vs. Vin and load

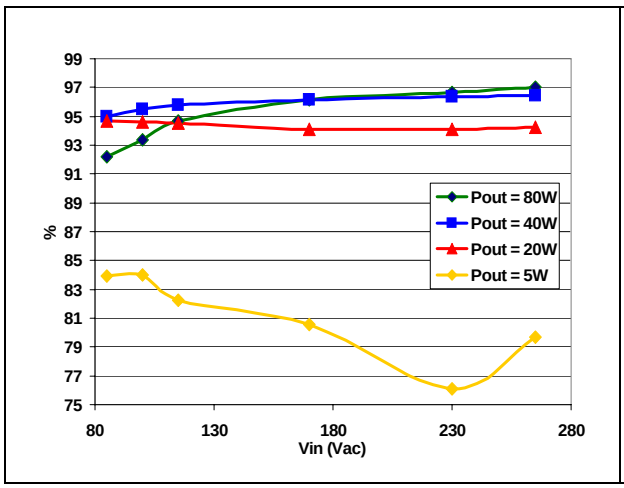
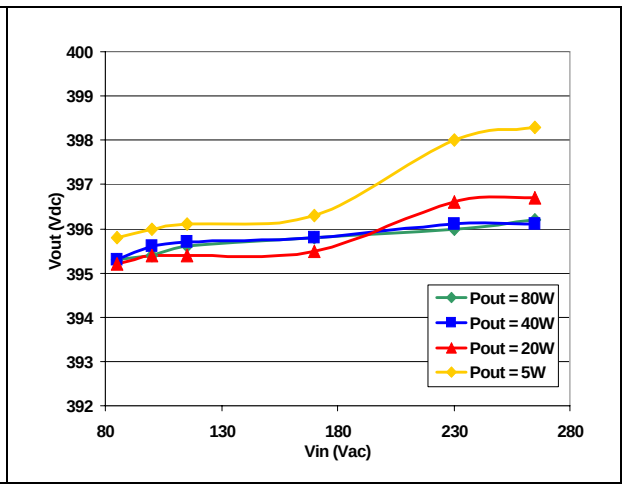


Figure 24. EVL6562A-TM-80W static Vout regulation vs. Vin and load



The efficiency is very good at all load and line conditions. At full load it is always significantly higher than 90%, making this design suitable for high-efficiency power supplies.

The measured output voltage variation at different line and load conditions is illustrated in *Figure 24*. As shown, the voltage is perfectly stable over the entire input voltage range. Just at 265Vac and light load, there are negligible deviations of 1 V due to the intervention of the burst mode function.

For user reference, waveforms of the input current and voltage at the nominal input voltage mains and different load conditions are shown in *Figure 25* through *Figure 30*.

Figure 25. EVL6562A-TM-80W input current at 100 V-50 Hz - 80 W load

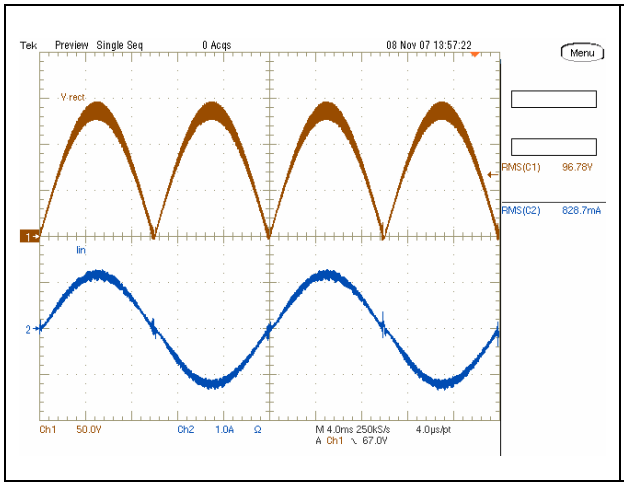


Figure 26. EVL6562A-TM-80W input current at 230 V-50 Hz - 80 W load

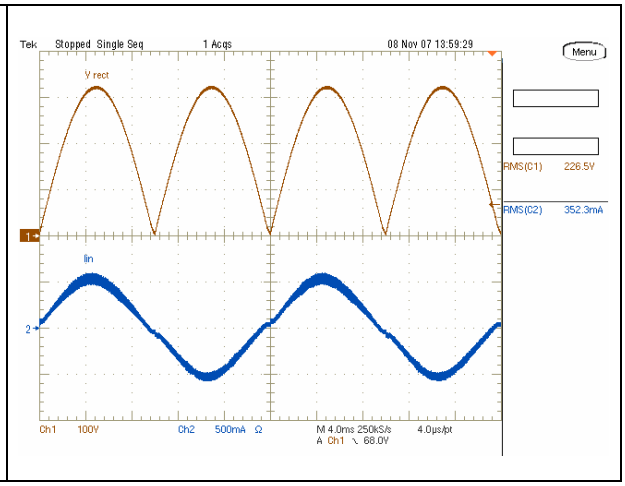


Figure 27. EVL6562A-TM-80W input current at 100 V-50 Hz - 40 W load

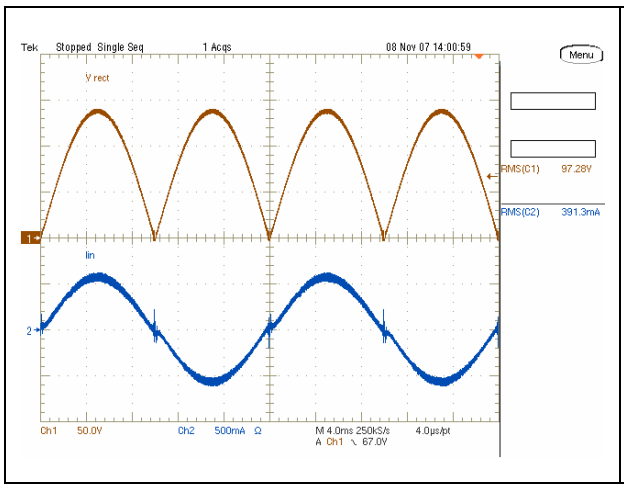


Figure 28. EVL6562A-TM-80W input current at 230 V-50 Hz - 40 W load

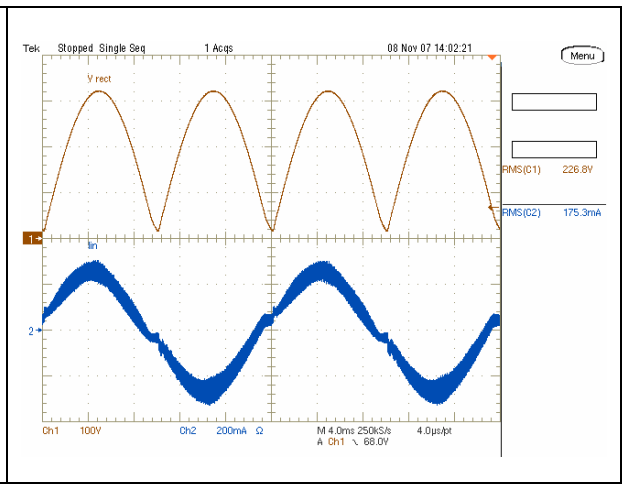


Figure 29. EVL6562A-TM-80W input current at 100 V-50 Hz - 20 W load

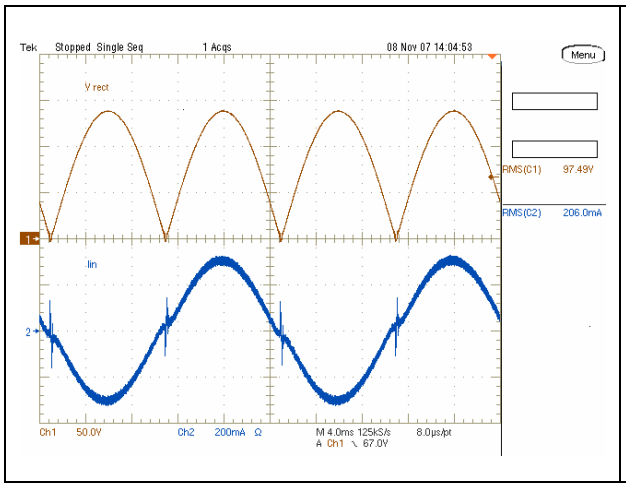
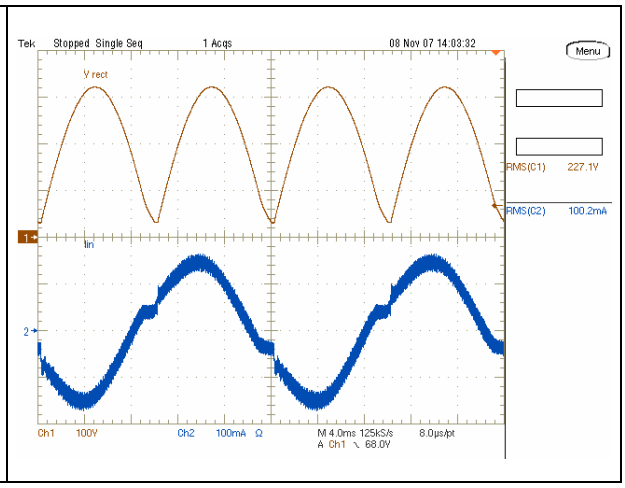


Figure 30. EVL6562A-TM-80W input current at 230 V-50 Hz - 20 W load



7 L6562A layout hints

The layout of any converter is a very important phase in the design process that sometimes does not get enough attention from the engineers. Even if it the layout phase sometimes looks time-consuming, a good layout does indeed save time during the functional debugging and the qualification phases. Additionally, a power supply circuit with a correct layout needs smaller EMI filters or less filter stages and which allows consistent cost savings.

The L6562A does not need any special attention to the layout, simply the general layout rules for any power converter must be carefully applied. Basic rules are listed below which can be used for other PFC circuits at any power level, working either in TM or with an FOT-control mode.

1. Keep power and signal RTNs separated. Connect the return pins of components carrying high currents such as input capacitors, sense resistors, or output capacitors as close as possible. This point is the RTN star point. A downstream converter or ballast must be connected to this return point.
2. Minimize the length of the traces relevant to the boost inductor, boost rectifier, and output capacitor.
3. Keep signal components as close as possible to L6562A pins. Specifically, keep the tracks relevant to pin #1 (INV) net as short as possible. Components and traces relevant to the error amplifier have to be placed far from traces and connections carrying signals with high dv/dt like the MOSFET drain.
4. Connect heat sinks to power GND.
5. Place an external copper shield around the boost inductor and connect it to power GND.
6. Please connect the RTN of signal components including the feedback and MULT dividers close to the L6562A pin #6 (GND).
7. Connect a ceramic capacitor (100÷470 nF) to pin #8 (Vcc) and to pin #6 (GND), close to the L6562A. Connect this point to the RTN start point 1.

8 Reference

1. L6562A datasheet
2. "A systematic Approach to Frequency Compensation of the voltage loop in Boost PFC pre regulator", Abstract
3. AN1089

9 Revision history

Table 1. Document revision history

Date	Revision	Changes
20-Aug-2008	1	Initial release
17-Nov-2009	2	*Figure 1*, *13*, *14*, *16* modified *(8)*, *(10)*, *(26)*, *(27)*, *(29)*, *(30)*, and *Section 3.3.3* modified