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**3 W, 5 V isolated flyback converter using the VIPer06HS, from the VIPer™ plus family**

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## Introduction

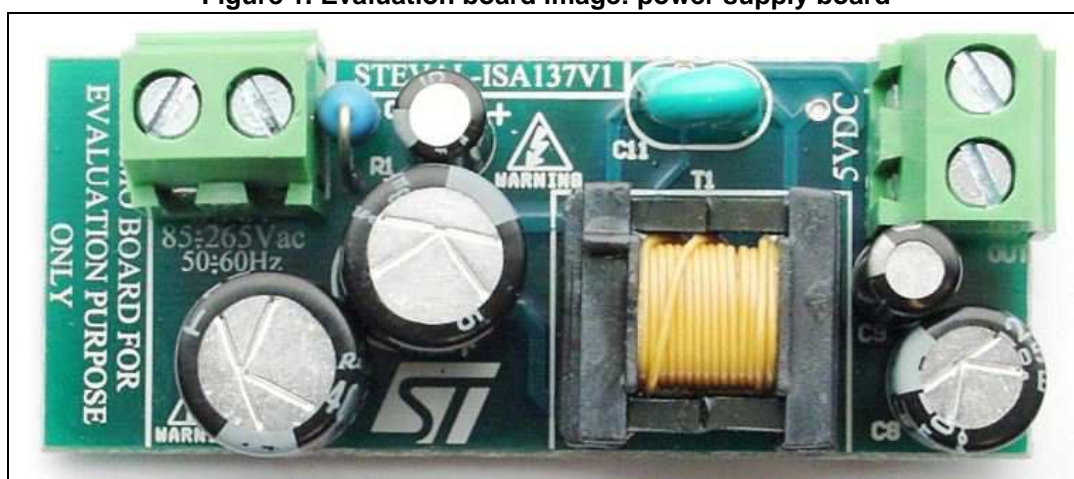
This document describes the STEVAL-ISA137V1, a 5 V - 3 W power supply in isolated flyback topology with VIPer06HS: a new off-line high voltage converter by STMicroelectronics.

The main features of the device are: 800 V avalanche rugged power section, PWM operation at 115 kHz with frequency jittering for lower EMI, cycle-by-cycle current limit with adjustable set point, on-board soft-start and safe auto-restart after a fault condition.

The available protections are: thermal shutdown with hysteresis, delayed overload protection and open loop failure protection (only available if auxiliary winding is used).

This flyback converter is suitable for different applications. It can be used as an external adapter or as an auxiliary power supply in consumer equipment.

**Figure 1. Evaluation board image: power supply board**



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## 1 Test board: design and evaluation

The electrical specifications of the test board are listed in [Table 1](#).

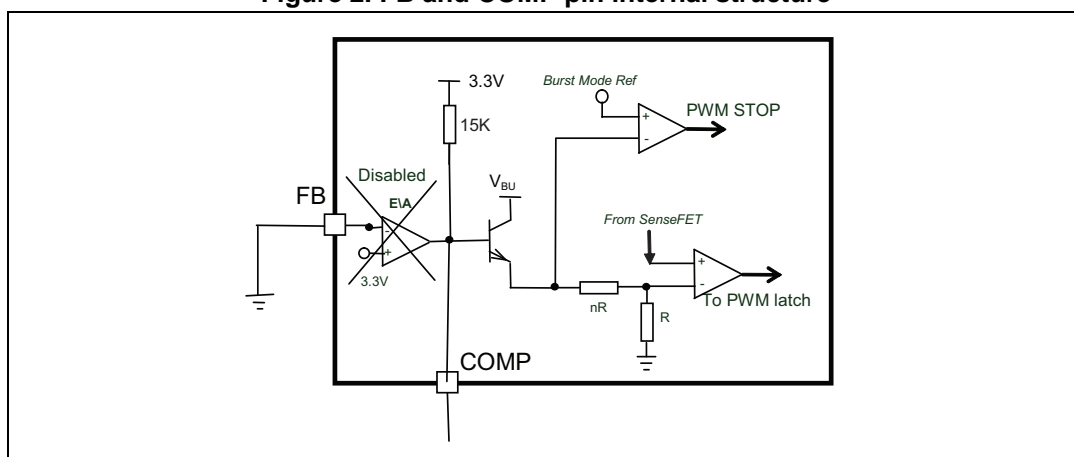
### Table 1. Electrical specifications

Parameter	Symbol	Value
AC main input voltage	$V_{IN}$	[85 V <sub>AC</sub> ; 265 V <sub>AC</sub> ]
Main frequency	$f_L$	[50 Hz; 60 Hz]
Output voltage	$V_{OUT}$	5 V
Max output current	$I_{OUT}$	600 mA
Precision of output regulation	$\Delta V_{OUT\_LF}$	±5%
High frequency output voltage ripple	$\Delta V_{OUT\_HF}$	50mV
Min active mode efficiency	$\eta_{AV}$	66.89%
Max ambient operating temperature	$T_{AMB}$	60 °C

The power supply is set in the isolated flyback topology. The schematic is given in [Figure 3](#) and the bill of materials (BOM) in [Table 2](#). The input section includes a resistor R1 to limit inrush current, a diode bridge (BR) and a  $\Pi$  filter for EMC suppression (C1, L1, C2). The transformer core is a standard E13. A clamp network (D1, R2, C3) is used for leakage inductance demagnetization.

As the device is used in a secondary regulation isolated topology, the FB pin must be connected to ground in order to disable the internal error amplifier. In this case, the feedback signal is transferred to the primary side through an opto-isolator connected in parallel with the compensation network (R5, C6, C7) to the COMP pin.

### Figure 2. FB and COMP pin internal structure



The resistor connected between the LIM pin and ground lowers the default current limitation of the device (according to the  $I_{DILIM}$  vs  $R_{LIM}$  illustration given in the datasheet) to the value

required for the desired power throughput, thus avoiding unnecessary overstress on the power components. A small LC filter has been added at the output in order to filter the high frequency ripple.

At power-up, the DRAIN pin supplies the internal HV start-up current generator which charges the C4 capacitor up to  $V_{DDon}$ . At this point the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C4.

The IC is supplied by the auxiliary winding and the voltage delivered must always remain above the  $V_{DDCS\_on}$  threshold (11.5V max.), in order to avoid activating the HV start-up. Auxiliary winding is connected to the  $V_{DD}$  pin through D3 and L2, where the inductor component is used to filter voltage spike on  $V_{DD}$  pin, during power MOSFET turn-off. This solution is preferred because, using a resistor, the continuous voltage on the  $V_{DD}$  pin drops and the voltage may fall below the  $V_{DDCS\_on}$  threshold.

An external clamp on the  $V_{DD}$  pin (Zener diode and resistor) is used to protect the pin when overvoltage, due to an increase of output voltage, occurs on the same pin.

### Figure 3. Electrical schematic

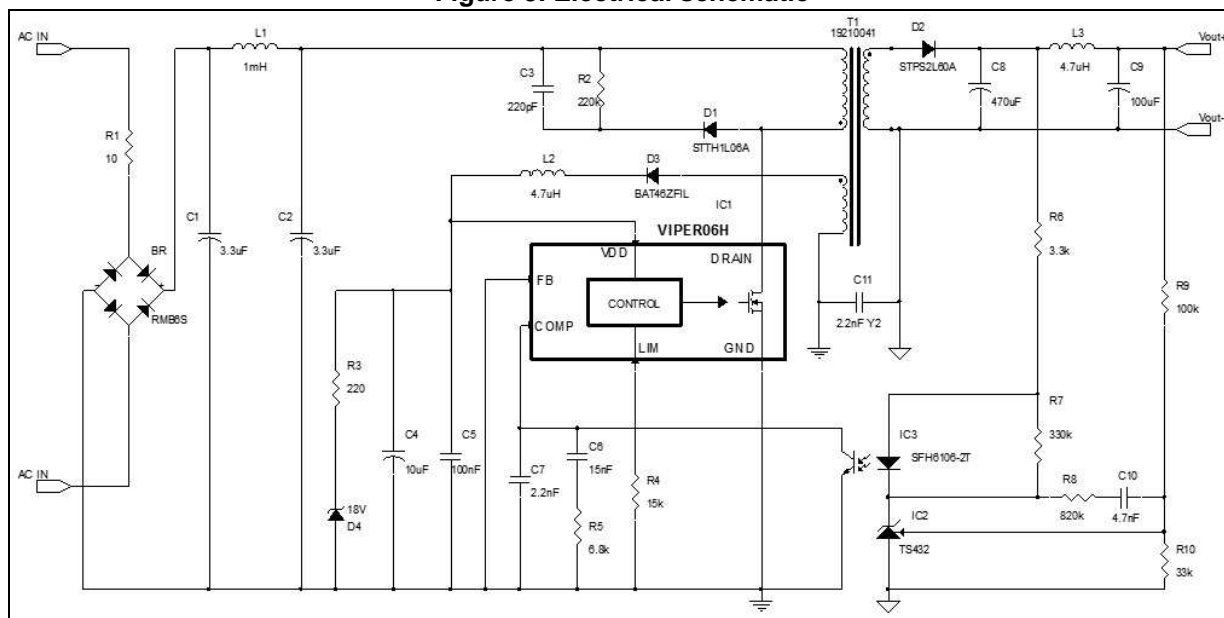


Table 2. Bill of materials (BOM)

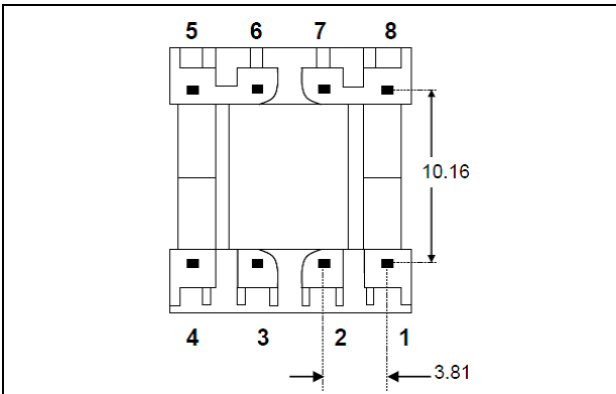
Reference	Part	Description	Note
BR	RMB6S	0.5A – 600V Bridge	Taiwan Semiconductor
R1	ROX1SJ10R	10 $\Omega$ ±5% - 1W Resistor	TE Connectivity
R2	ERJT08J224V	220k $\Omega$ ±5% - 1/3W Resistor	Panasonic
R3	ERJT08J221V	220 $\Omega$ ±5% - 1/3W Resistor	Panasonic
R4	CRG0603F15K	15k $\Omega$ ±1% - 1/10W Resistor	TE Connectivity
R5	ERJ3GEYJ682V	6.8k $\Omega$ ±5% - 1/10W Resistor	Panasonic
R6	ERJ3GEYJ332V	3.3k $\Omega$ ±5% - 1/10W Resistor	Panasonic
R7	ERJ3GEYJ334V	330k $\Omega$ ±5% - 1/10W Resistor	Panasonic
R8	ERJ3GEYJ824V	820k $\Omega$ ±5% - 1/10W Resistor	Panasonic
R9	CRG0603F100K	100k $\Omega$ ±1% - 1/10W Resistor	TE Connectivity
R10	CRG0603F33K	33k $\Omega$ ±1% - 1/10W Resistor	TE Connectivity
C1,C2	400LLE3R3MEFC8X11R5	3.3 $\mu$ F - Electrolytic capacitor 400V	Rubycon
C3	C3216C0G2J221J060AA	220pF - Capacitor 630V	TDK
C4	50YK10MEFCTA5X11	10 $\mu$ F - Electrolytic capacitor 50V	Rubycon
C5	GRM188R71H104KA93D	100nF - Capacitor 50V	Murata
C6	GRM188R71H153KA01D	15nF - Capacitor 50V	Murata
C7	GRM1885C1H222FA01D	2.2nF - Capacitor 50V	Murata
C8	16ZLH470MEFC8X11.5	470 $\mu$ F - Electrolytic capacitor 16V	Rubycon
C9	EEUEB1A101	100 $\mu$ F - Electrolytic capacitor 10V	Panasonic
C10	VJ0603Y472KNAAO	4.7nF - Capacitor 50V	Vishay
C11	DE2E3KY222MA2BM01	2.2nF - Capacitor Y2	Murata
D1	STTH1L06A	Ultrafast diode 1A – 600V	STMicroelectronics
D2	STPS2L60A	Power Schottky 2A – 60V	STMicroelectronics
D3	BAT46ZFILM	Signal Schottky 0.15A – 100V	STMicroelectronics
D4	MMSZ5248B-V-GS08	Zener diode 18V 0.5W	Vishay
T1	1921.0041	Flyback transformer	Magnetica
	750370423 Rev. 6A		Würth
IC1	VIPer06HS	Offline primary controller	STMicroelectronics
IC2	TS432ILT	Low voltage adjustable shunt reference	STMicroelectronics
IC3	SFH6106-2T	Optocoupler	Vishay
L1	LPS4414	1mH - Power Inductor	Coilcraft
L2	LPS3008	4.7 $\mu$ H - Power Inductor	Coilcraft
L3	ME3220	4.7 $\mu$ H - Power Inductor	Coilcraft

The transformer characteristics are listed in the table below.

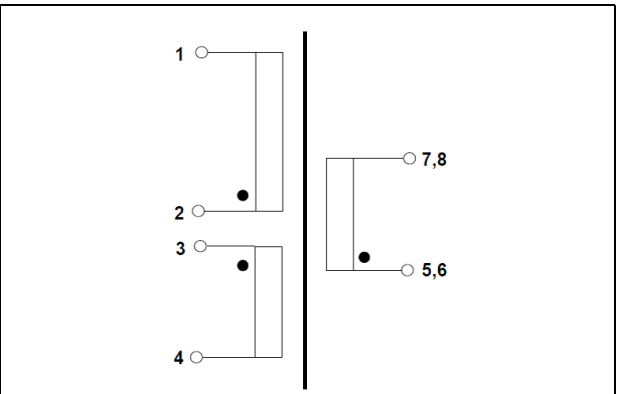
**Table 3. Transformer characteristics**

Parameter	Value	Test conditions
Manufacturer	MAGNETICA	
Part number	1921.0041	
Primary inductance	1.5 mH $\pm$ 20%	Measured at 1 kHz, $T_{AMB} = 20^{\circ}\text{C}$
Leakage inductance	19 $\mu\text{H}$ Nom.	Measured at 10 kHz, $T_{AMB} = 20^{\circ}\text{C}$
Primary to secondary turn ratio (3 - 4)/(5 - 8)	13.75	Measured at 10 kHz, $T_{AMB} = 20^{\circ}\text{C}$
Primary to auxiliary turn ratio (3 - 4)/(2 - 1)	4.78	Measured at 10 kHz, $T_{AMB} = 20^{\circ}\text{C}$
Saturation current	0.27 A	Primary, $B_{SAT} = 0.3 \text{ T}$ , $T_{AMB} = 20^{\circ}\text{C}$
Operating current	0.14 A	Primary, $P_{OUT} = 1.5 \text{ W}$ , $T_{AMB} = 20^{\circ}\text{C}$

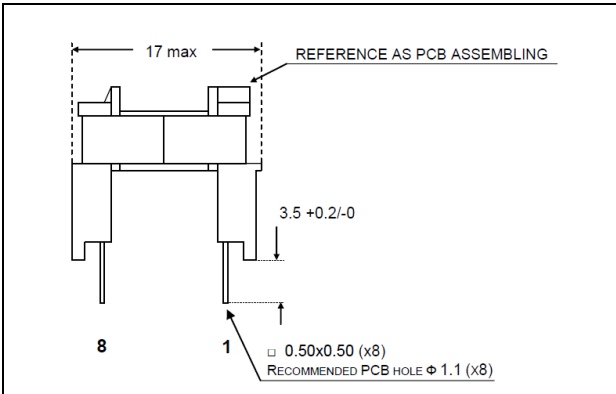
**Figure 4. Dimensional drawing and pin placement diagram - bottom view**



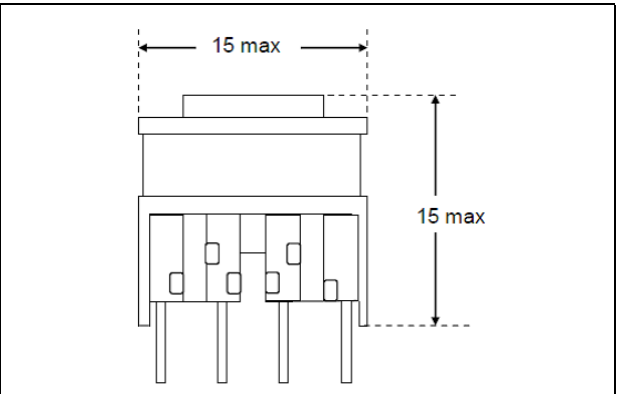
**Figure 5. Dimensional drawing and pin placement diagram - electrical diagram**



**Figure 6. Dimensional drawing and pin placement diagram - side view 1**



**Figure 7. Dimensional drawing and pin placement diagram - side view 2**



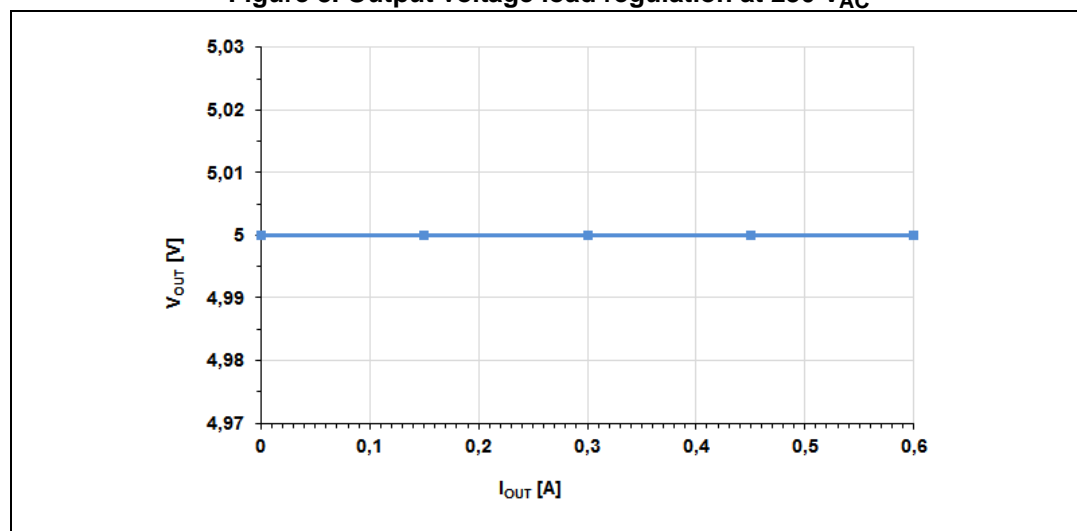
## 1.1 Output voltage characteristics

The output voltage of the board is measured under different line and load conditions. [Table 4](#) clearly demonstrates that the output voltage is not affected by line and load variations. For this reason, [Figure 8](#) shows the load regulation for only one input voltage (230 V<sub>AC</sub>).

**Table 4. Output voltage line-load regulation**

V <sub>IN</sub> (V <sub>AC</sub> )	V <sub>OUT</sub> (V)			
	No load	0.3 A	0.45 A	0.6 A
85	5.00	5.00	5.00	5.00
115	5.00	5.00	5.00	5.00
150	5.00	5.00	5.00	5.00
180	5.00	5.00	5.00	5.00
230	5.00	5.00	5.00	5.00
265	5.00	5.00	5.00	5.00

**Figure 8. Output voltage load regulation at 230 V<sub>AC</sub>**



## 1.2 Efficiency measurements

Any external power supply (EPS) must be capable of meeting the international regulation agency limits. The European code of conduct (EC CoC version 5) and US department of energy (DoE-US EISA 2007) limits are taken as references. EPS limits are fixed up to 66.89%, where the average efficiency is measured.

The efficiency of the converter has been measured under different load and line voltage conditions.

The efficiency measurements have been performed with loading at 25%, 50%, 75% and 100% of maximum rate at 115 V<sub>AC</sub> and 230 V<sub>AC</sub>.

[Table 5](#) and [Table 6](#) show the results.

**Table 5. Efficiency at 115 V<sub>AC</sub>**

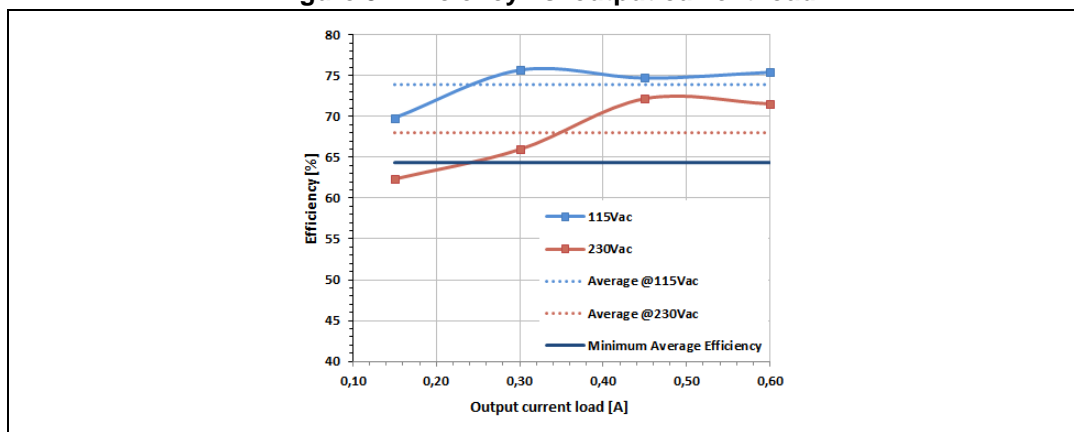
%Load	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>IN</sub> (W)	P <sub>OUT</sub> (W)	Efficiency (%)
25%	0.15	5.00	1.074	0.750	69.83
50%	0.30	5.00	1.982	1.500	75.68
75%	0.45	5.00	3.012	2.250	74.70
100%	0.60	5.00	3.978	3.000	75.41
Average efficiency					73.91

**Table 6. Efficiency at 230 V<sub>AC</sub>**

%Load	I <sub>OUT</sub> (A)	V <sub>OUT</sub> (V)	P <sub>IN</sub> (W)	P <sub>OUT</sub> (W)	Efficiency (%)
25%	0.15	5.00	1.203	0.750	62.34
50%	0.30	5.00	2.274	1.500	65.96
75%	0.45	5.00	3.117	2.250	72.18
100%	0.60	5.00	4.193	3.000	71.55
Average efficiency					68.01



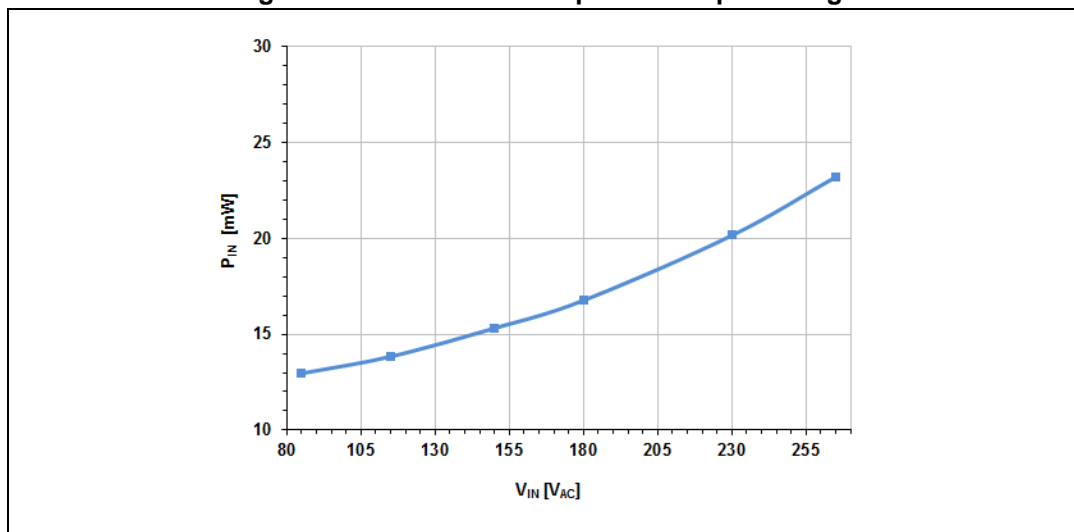
Figure 9. Efficiency vs. output current load



### 1.3 No load consumption

The input power of the converter has been measured under no load condition; in this situation, the converter works in burst mode so that the average switching frequency is reduced.

Figure 10. No load consumption vs. input voltage

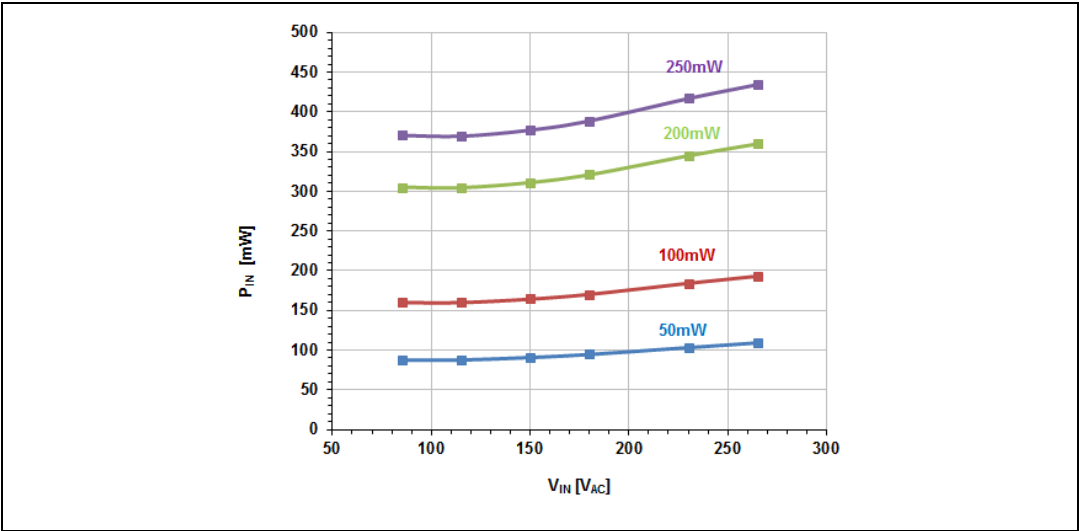


### 1.4 Light load consumption

Even if the EC CoC and DoE US EISA 2007 do not stipulate other requirements regarding light load performance, the input power of the demo-board under light load conditions is given in order to provide a complete picture.

In particular, in order to comply with EuP Lot 6, the EPS requires an efficiency higher than 50% when the output load is 250 mW. The test board also satisfies this requirement.

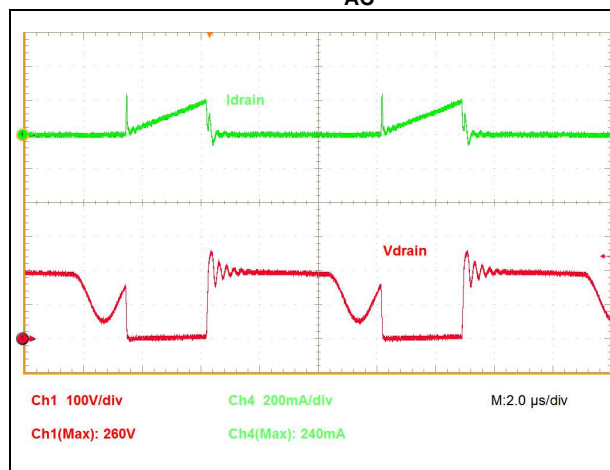
Figure 11. Light load consumption at different output power



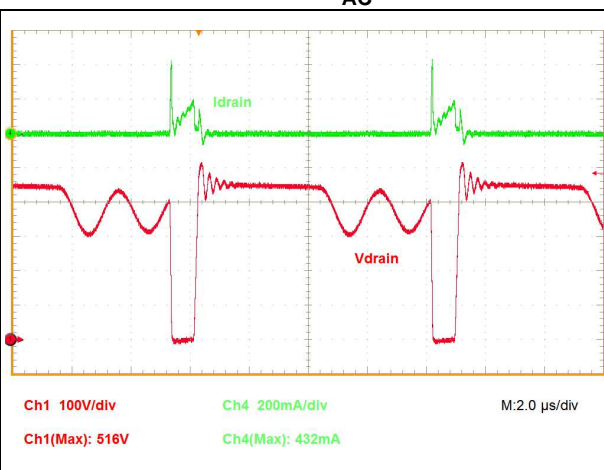
## 2 Typical board waveforms

Drain voltage and current waveforms under full load condition are reported for minimum and maximum input voltage in [Figure 12](#) and [Figure 13](#), and for the two nominal input voltages in [Figure 14](#) and [Figure 15](#) respectively.

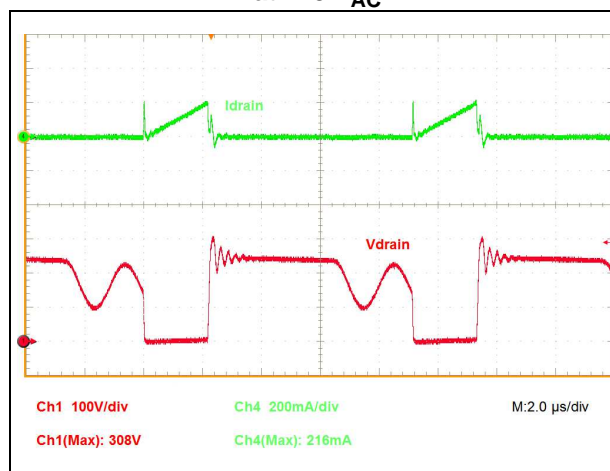
**Figure 12. Drain current and voltage at full load at 85 V<sub>AC</sub>**



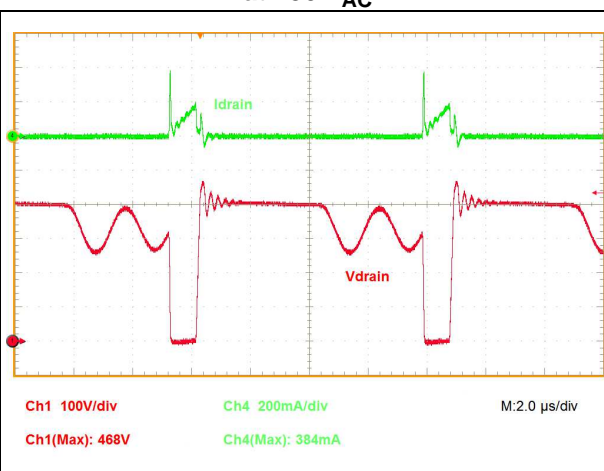
**Figure 13. Drain current and voltage at full load at 265 V<sub>AC</sub>**



**Figure 14. Drain current and voltage at full load at 115 V<sub>AC</sub>**

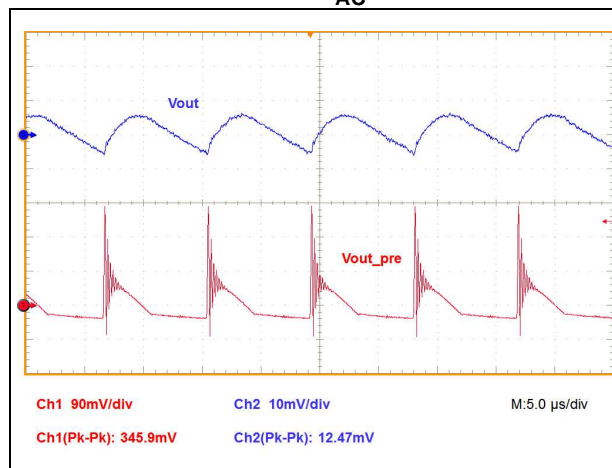
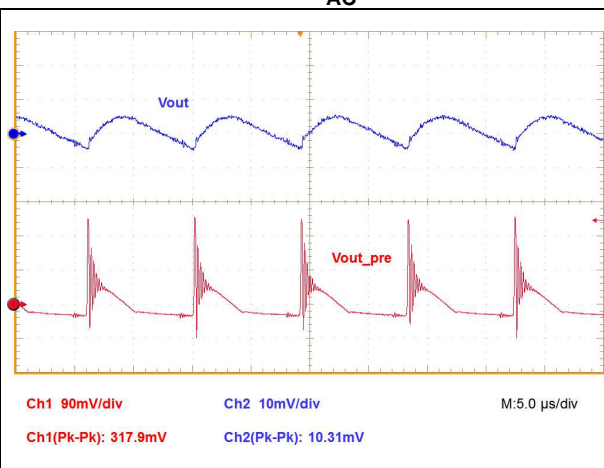


**Figure 15. Drain current and voltage at full load at 230 V<sub>AC</sub>**



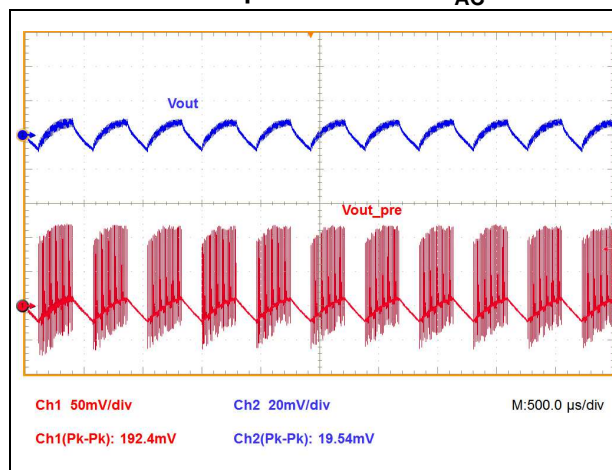
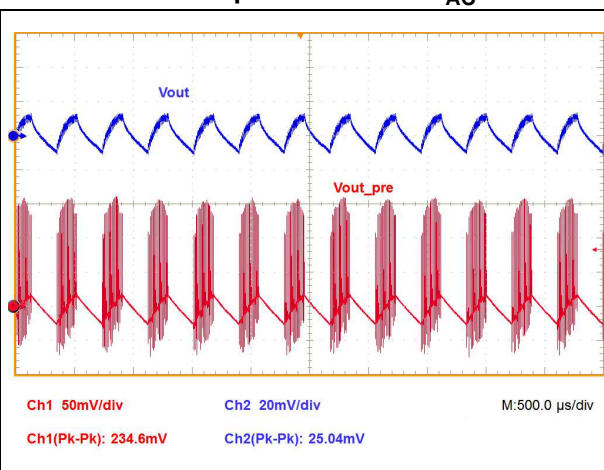
The output ripple at the switching frequency was also measured. The board is provided with an LC filter to further reduce the ripple without reducing the overall ESR of the output capacitor.

The voltage ripple across the output connector ( $V_{OUT}$ ) and before the LC filter ( $V_{OUT\_PRE}$ ) was measured in order to verify the effectiveness of the LC filter. The following two diagrams show the voltage ripple at 115 V<sub>AC</sub> ([Figure 16](#)) and at 230 V<sub>AC</sub> ([Figure 17](#)) under full load condition.

Figure 16. Output voltage ripple at full load at 115 V<sub>AC</sub>Figure 17. Output voltage ripple at full load at 230 V<sub>AC</sub>

As the load is so low that the voltage at the COMP pin falls below the V<sub>COMPL</sub> internal threshold (typically 1.1 V), the VIPer06HS is disabled. At this point, the feedback reaction to the energy delivery cutoff forces the COMP pin voltage to rise and, when it is 40 mV above the V<sub>COMPL</sub> threshold, the device begins switching again. This results in a controlled on/off operation which is referred to as “burst mode”. This mode of operation reduces frequency-related losses when the load is very light or disconnected, facilitating compliance with energy saving regulations.

The figures below show the output voltage ripple when the converter operates in burst mode and is supplied with 115 V<sub>AC</sub> and with 230 V<sub>AC</sub> respectively.

Figure 18. Output voltage ripple during burst mode operation at 115 V<sub>AC</sub>Figure 19. Output voltage ripple during burst mode operation at 230 V<sub>AC</sub>

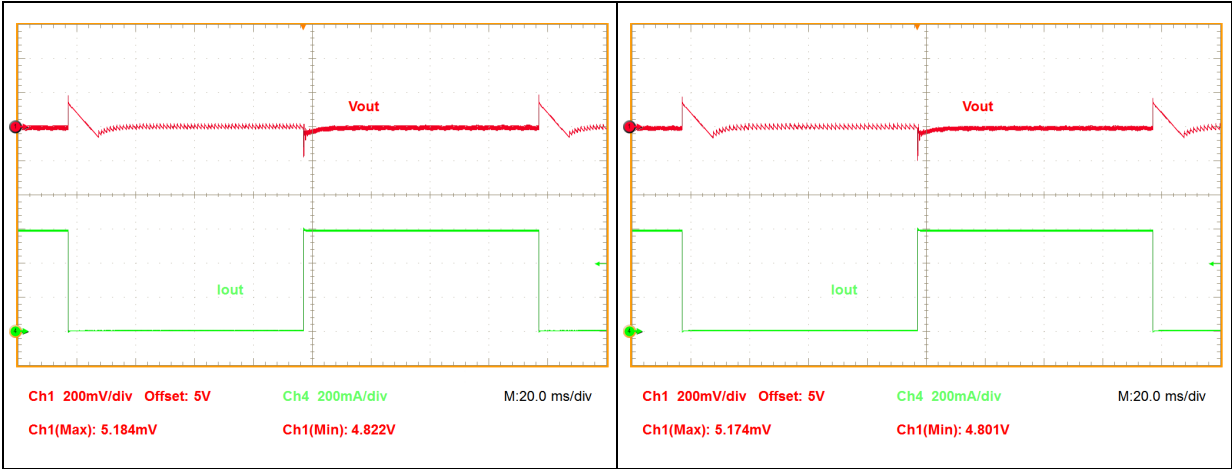
2.1 Dynamic step load regulation

In any power supply, it is important to measure the output voltage when the converter is subjected to dynamic load variations in order to ensure good stability and that no overvoltage or undervoltage occurs.

The test has been performed for both nominal input voltages, varying the output load from 0 to 100% of the nominal value.

In every tested condition, no abnormal oscillations were revealed on the output and over/under shoot were well within acceptable values.

Figure 20. Dynamic step load (0 to 100% output load) at 115 V<sub>AC</sub>      Figure 21. Dynamic step load (0 to 100% output load) at 230 V<sub>AC</sub>



### 3 Soft-start

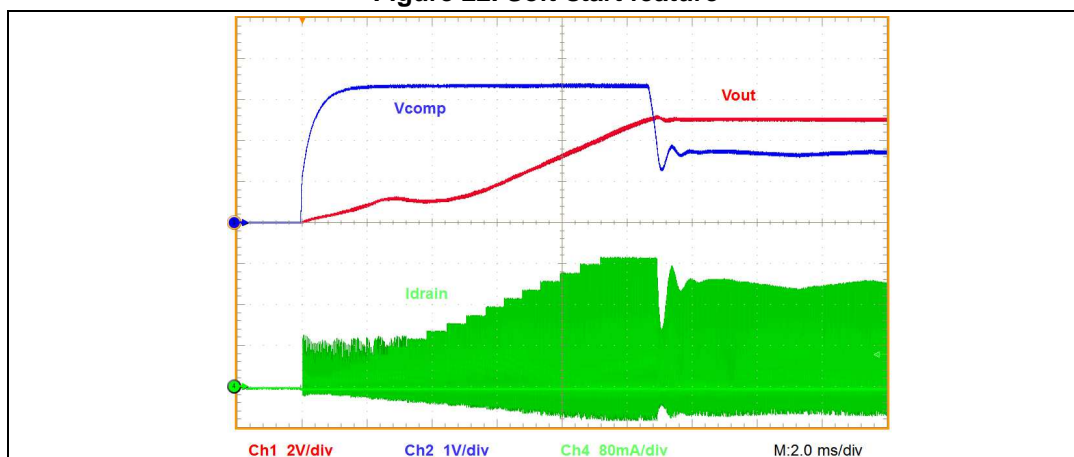
When the converter starts, the output capacitor has no charge and needs some time to reach the steady state condition. During this time, the power demand from the control loop is at its maximum, while the reflected voltage is low. These two conditions may lead to a deep continuous operating mode of the converter.

Also, when the power MOSFET is switched on, it cannot be switched off immediately as the minimum on time ( $T_{ON\_MIN}$ ) must first elapse. Because of the deep continuous operating mode of the converter, during  $T_{ON\_MIN}$ , an excessive drain current can overstress the component of the converter as well as the device itself, the output diode and the transformer. Transformer saturation is also possible under these conditions.

To avoid all the above mentioned negative effects, the VIPer06HS implements an internal soft-start feature. As the device begins operation, regardless of the control loop request, the drain current is allowed to gradually increase from zero to the maximum value.

The drain current limit is increased in steps, and the range from 0 to the fixed drain current limitation value (which can be adjusted through an external resistor) is divided in 16 steps. Each step length is 64 switching cycles, for a total duration of the soft-start phase around 8.5ms. [Figure 22](#) shows the soft-start phase of the converter when it is operating at minimum line voltage and maximum load.

Figure 22. Soft-start feature



## 4 Protection features

In order to increase end-product safety and reliability, VIPer06HS has the following protection mechanisms: overload and short-circuit protection and open loop failure protection.

In the following sections, these protection mechanisms are tested and the results are presented.

### 4.1 Overload and short-circuit protection

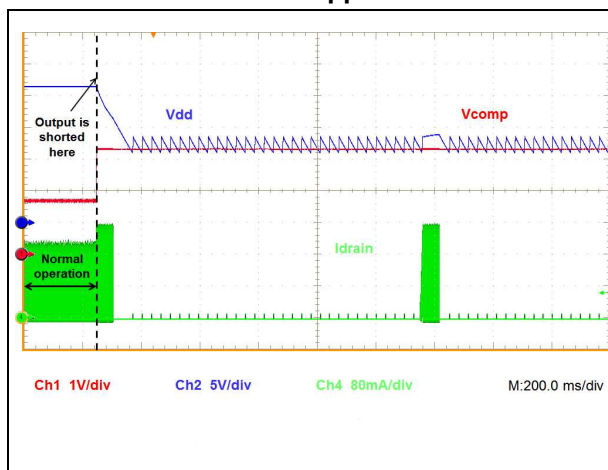
In case of overload or output short-circuit (see [Figure 23](#)), the drain current reaches the  $I_{DLIM}$  value (or the one set by the user through the  $R_{LIM}$  resistor). For each cycle that this condition is met, a counter increments; if this state is maintained continuously for the time  $t_{OVL}$  (50 ms typical, internally fixed), the overload protection is tripped, the power section is turned off and the converter is disabled for a  $t_{RESTART}$  time (typically 1 s). When this time has elapsed, the IC resumes switching and, if the short is still present, the protection again activates ([Figure 24](#)). This ensures that the restart attempts of the converter are at a low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in case of repeated overload events.

Moreover, whenever the protection is tripped, the internal soft start function is invoked ([Figure 25](#)) in order to reduce the stress on the secondary diode.

When the short is removed, the IC resumes normal operation. If the short is removed during  $t_{SS}$  or  $t_{OVL}$ , i.e., before the protection tripping, the counter decrements each cycle down to zero and the protection is thus not tripped.

If the short-circuit is removed during  $t_{RESTART}$ , the IC waits until  $t_{RESTART}$  has elapsed before resuming switching ([Figure 26](#)).

**Figure 23. Overload protection: output short-circuit applied**



**Figure 24. Overload protection: continuous output short-circuit**

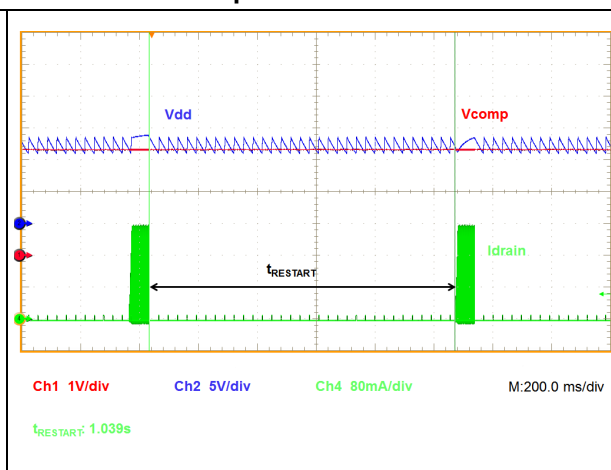


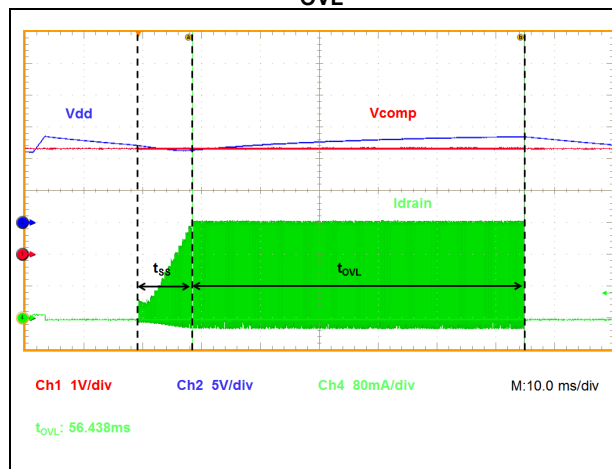
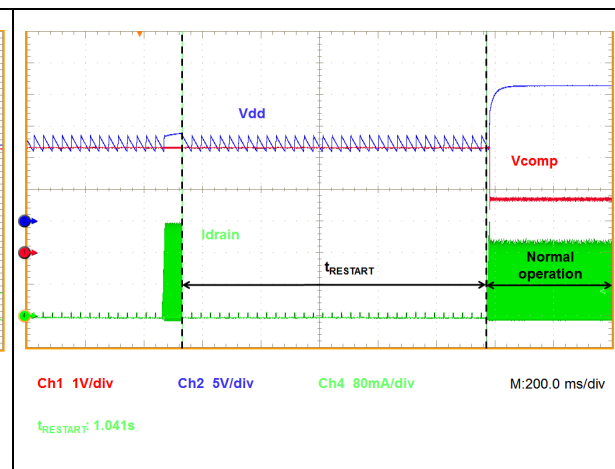
Figure 25. Overload protection: soft start and  $t_{OVL}$ 

Figure 26. Overload protection: short-circuit removal



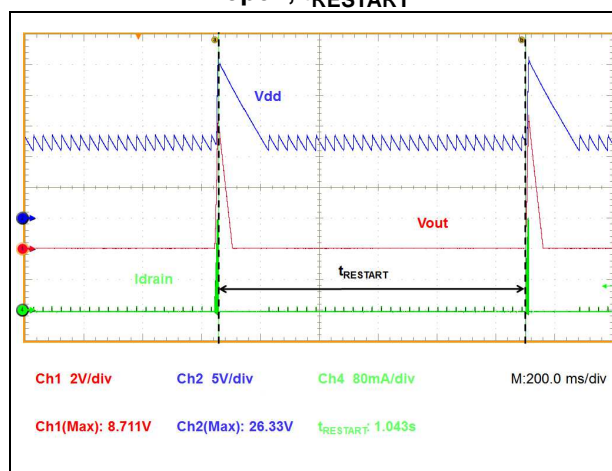
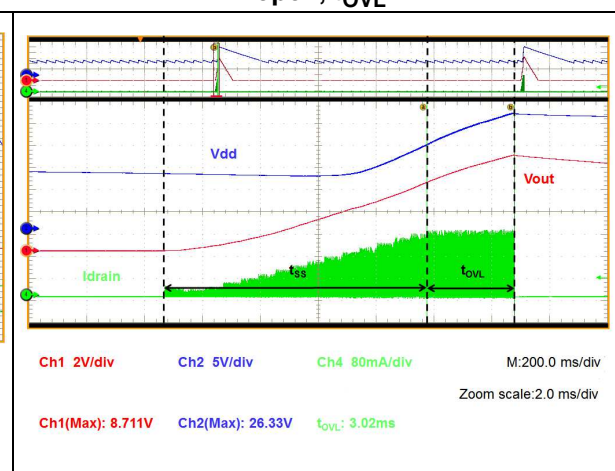
## 4.2 Open-loop failure protection

This kind of protection is useful when the device is supplied by an auxiliary winding and it is activated when feedback loop failure or auxiliary winding disconnection occurs.

If R9 is open or R10 is shorted, the VIPer06HS works at its drain current limitation. The output voltage,  $V_{OUT}$ , increases with the auxiliary voltage  $V_{AUX}$ , which is coupled with the output according to the secondary-to-auxiliary turns ratio.

As the auxiliary voltage rises to the internal  $V_{DD}$  active clamp,  $V_{DDclamp}$  (23.5 V min.), and the clamp current injected on the  $V_{DD}$  pin exceeds the latch threshold,  $I_{DDol}$  (4 mA min.), a fault signal is internally generated and the device stops switching even if  $t_{OVL}$  hasn't elapsed yet (see Figure 28).

To verify the effectiveness of this protection, the external clamp on the  $V_{DD}$  pin has been removed.

Figure 27. Open loop failure protection: R9 open,  $t_{RESTART}$ Figure 28. Open loop failure protection: R9 open,  $t_{OVL}$ 

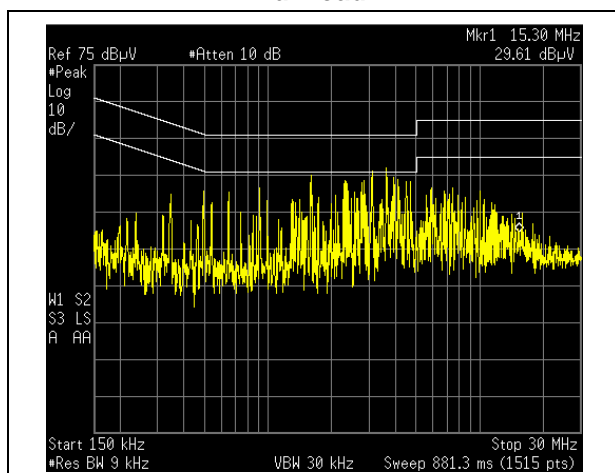


## 5 Conducted noise measurements

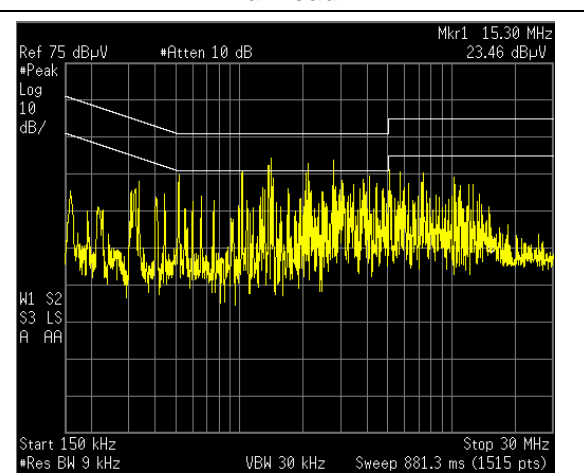
The VIPer06HS frequency jittering feature allows the spectrum to be spread over frequency bands rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dB $\mu$ V.

A pre-compliance test for the EN55022 (Class B) European normative was performed and peak measurements of the conducted noise emissions at full load and nominal mains voltages are shown in [Figure 29](#) and [Figure 30](#). The diagrams show that the measurements are well within the limits in all test conditions.

**Figure 29. CE peak measurement at 115 V<sub>AC</sub> full load**



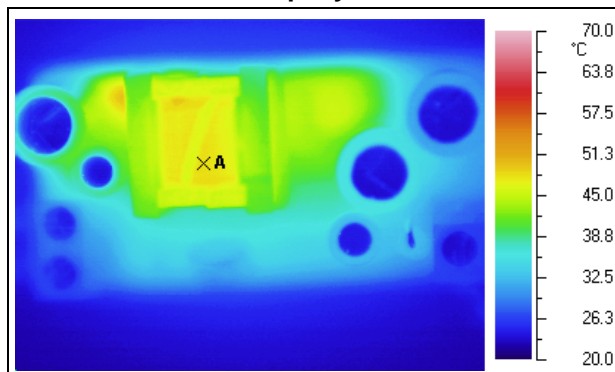
**Figure 30. CE peak measurement at 230 V<sub>AC</sub> full load**



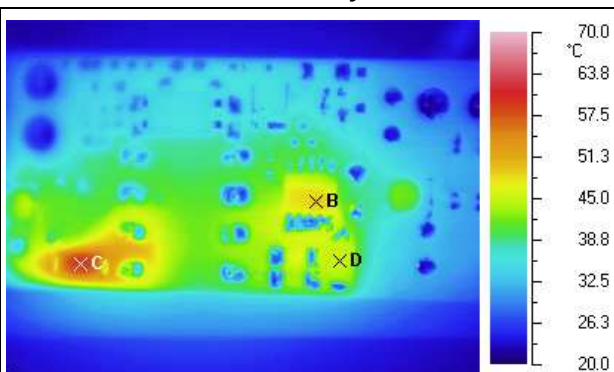
## 6 Thermal measurements

Thermal analysis of the board was performed using an IR camera for the two nominal input voltages (115 V<sub>AC</sub> and 230 V<sub>AC</sub>) under full load condition. The results are shown in [Figure 31](#) to [Figure 34](#) and summarized in [Table 7](#).

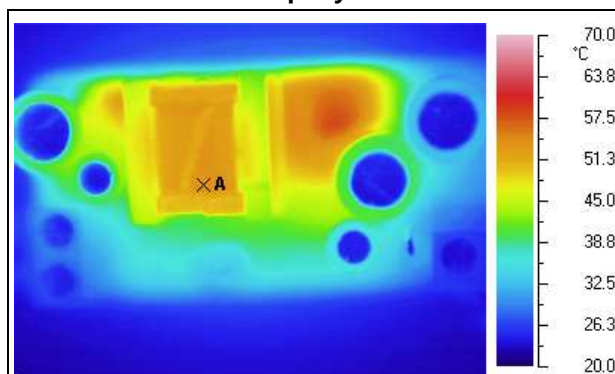
**Figure 31. Thermal map at 115 V<sub>AC</sub> full load.  
Top layer**



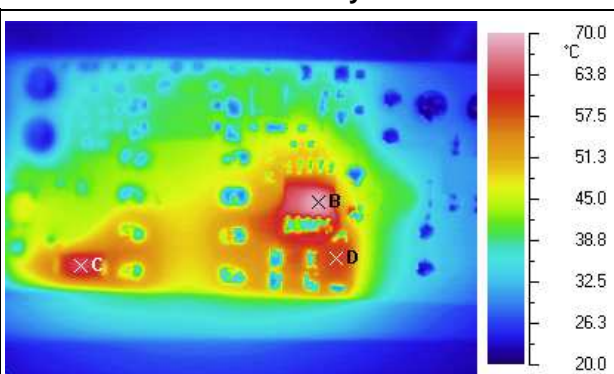
**Figure 32. Thermal map at 115 V<sub>AC</sub> full load.  
Bottom layer**



**Figure 33. Thermal map at 230 V<sub>AC</sub> full load.  
Top layer**



**Figure 34. Thermal map at 230 V<sub>AC</sub> full load.  
Bottom layer**



**Table 7. Temperature of key components (T<sub>amb</sub> = 25 °C, emissivity = 0.95 for all points)**

Point	Temp (°C)		Reference
	115 V <sub>AC</sub>	230 V <sub>AC</sub>	
A	48.1	54.0	Transformer
B	49.0	69.4	VIPer06HS
C	59.4	63.7	Output diode
D	45.0	59.2	Snubber diode

## 7 Conclusions

In this document, a flyback has been described and characterized. Special attention was paid to efficiency and low load performances and the bench results were good with very low input power under light load conditions. The efficiency performance was compared with the requirements of EC CoC and DoE regulation programs for external AC-DC adapters with very good results, with the measured active mode efficiency always higher than the required minimum.

The EMI emissions are also quite low, even when only using a low cost input filter.

## 8 Evaluation tools and documentation

The VIPer06HS evaluation board order code is: STEVAL-ISA137V1

Further information about this product is available in the VIPer06 datasheet at [www.st.com](http://www.st.com).

## 9 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
20-Aug-2014	1	Initial release.
12-May-2016	2	Added: new T1 part 750370423 Rev 6A on <a href="#">Table 2</a> .

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