# AN4479
# Application note

## 12 V, 15 W peak 20 W isolated flyback converter based on VIPer38LE

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## Introduction

This document describes the STEVAL-ISA153V1, a 12 V - 15 W power supply in isolated flyback topology with VIPer38LE, a new off-line high voltage converter by STMicroelectronics. The main features of the device are: 800 V avalanche rugged power section, PWM operation at 60 kHz with frequency jittering for lower EMI, cycle-by-cycle current limit with adjustable set point, on-board soft-start and safe auto-restart after a fault condition. The available protections are: thermal shutdown with hysteresis, two levels of overcurrent protection, overvoltage and overload protections. The peculiar characteristic of the VIPer38 is the possibility to manage an extra output power for a fixed time, which can be set by a capacitor connected to EPT pin. The present flyback converter is suitable for different applications. It can be used as an external adapter or as an auxiliary power supply in consumer equipment.

**Figure 1. Evaluation board image: power supply board (top layer)**


**Figure 2. Evaluation board image: power supply board (bottom layer)**

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# 1 Test board: design and evaluation

The electrical specifications of the demo board are listed in *Table 1*.

**Table 1. Electrical specifications**

| Parameter | Symbol | Value |
|---|---|---|
| AC main input voltage | $V_{IN}$ | [90 $V_{AC}$; 265 $V_{AC}$] |
| Main frequency | $f_L$ | [50 Hz; 60 Hz] |
| Output voltage | $V_{OUT}$ | 12 V |
| Max output current | $I_{OUT}$ | 1.25 A |
| Precision of output regulation | $\Delta V_{OUT\_LF}$ | ±5% |
| High frequency output voltage ripple | $\Delta V_{OUT\_HF}$ | 50 mV |
| Min output peak power | | 20 W |
| Min duration output peak power | | 1.2 s |
| Standby input power @230$V_{AC}$ | | 30 mW |
| Min active mode efficiency | $\eta_{AV}$ | 81.55% |
| Min active mode at 10% load efficiency | $\eta_{10\%}$ | 71.55% |
| Max ambient operating temperature | $T_{AMB}$ | 60 °C |

The power supply is set in isolated flyback topology. The schematic is given in *Figure 3*, the bill of materials (BOM) in *Table 2*. Input section includes a NTC for inrush current limiting, a diode bridge (BR), a $\Pi$ filter (C2, L1, C3) and an X-capacitor (C1) for differential EMC suppression and a CM choke for common mode EMC suppression.

A clamp network (D1, R1, C4) is used for leakage inductance demagnetization.

The resistor connected between CONT pin and ground, lowers the default current limitation of the device (according to the $I_{DLIM}$ vs $R_{LIM}$ graphic reported in the datasheet) to the value which is needed for the desired power throughput, thus avoiding unnecessary overstress on the power components. A small LC filter has been added at the output in order to filter the high frequency ripple.

**Figure 3. Electrical schematic**

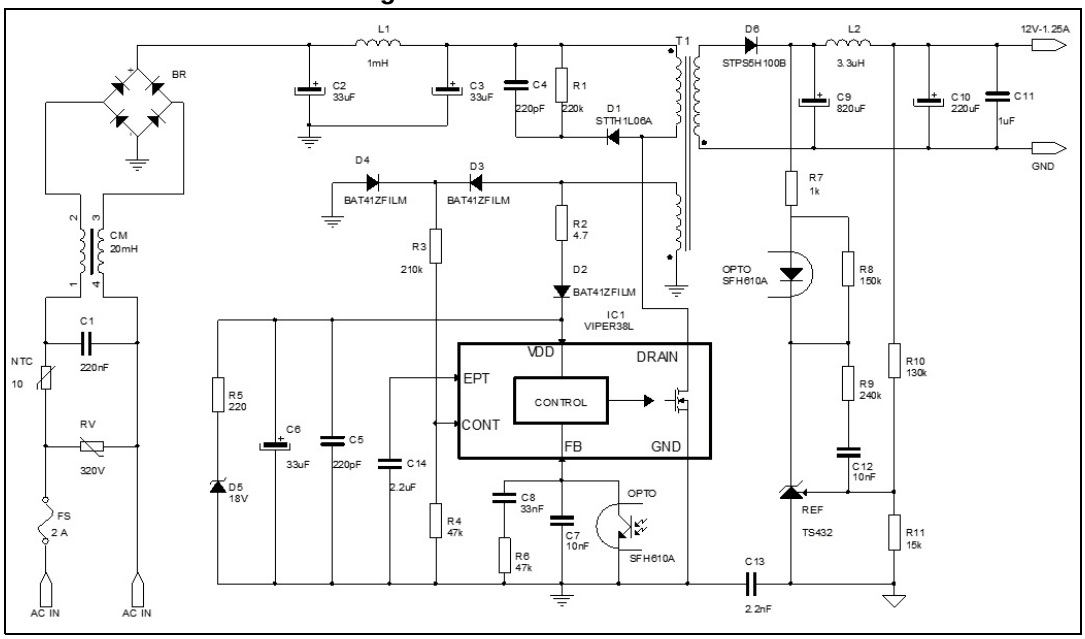



**Table 2. Bill of materials (BOM)**

| Reference | Part | Description | Note |
|---|---|---|---|
| BR | DBLS105G | 1 A - 600 V Bridge | Taiwan Semiconductor |
| RV | B72210S0321K101 | Varistor - 320 V | EPCOS |
| NTC | B57236S100M | 10 Ω | |
| FS | 0461002.ER | 2 A - Fuse | |
| R1 | ERJ-P08J224V | 220 kΩ - 0.33 W - 200 V Resistor | 5% tolerance |
| R2 | ERJ3RQF4R7V | 4.7 Ω - 1/10 W Resistor | 5% tolerance |
| R3 | ERJ-3EKF2103V | 210 kΩ - 1/10 W Resistor | 5% tolerance |
| R4 | ERJ-3EKF4702V | 47 kΩ - 1/10 W Resistor | 1% tolerance |
| R5 | ERJT06J221V | 220 Ω - 0.25 W Resistor | 5% tolerance |
| R6 | ERJ-3EKF4702V | 47 kΩ - 1/10 W Resistor | 5% tolerance |
| R7 | ERJ3GEYJ102V | 1 kΩ - 1/10 W Resistor | 5% tolerance |
| R8 | ERJ3GEYJ154V | 150 kΩ - 1/10 W Resistor | 5% tolerance |
| R9 | ERJ3GEYJ244V | 240 kΩ - 1/10 W Resistor | 5% tolerance |
| R10 | ERJP03F1303V | 130 kΩ - 0.22 W Resistor | 1% tolerance |
| R11 | ERJP03F1502V | 15 kΩ - 0.22 W Resistor | 1% tolerance |
| C1 | BFC233920224 | 220 nF - 275 V Capacitor X2 | |
| C2, C3 | 400BXW33MEFC10X30 | 33 µF-Electrolytic capacitor 400 V | Rubycon |
| C4 | C3216C0G2J221J060AA | 220 pF - Capacitor 630 V | |
| C5 | GRM188R71H221KA01D | 220 µF - Capacitor 50V | |

**Table 2. Bill of materials (BOM) (continued)**

| Reference | Part | Description | Note |
|---|---|---|---|
| C6 | 35YXM33MEFC5X11 | 33 µF - Electrolytic capacitor 35 V | Rubycon |
| C7 | GRM188R71H103KA01D | 10 nF - Capacitor 50 V | |
| C8 | GRM188R71H333KA61D | 33 nF - Capacitor 50 V | |
| C9 | 25ZLK820M10X20 | 820 µF - Electrolytic capacitor 25 V | Rubycon |
| C10 | 25YK220M6.3X11 | 220 µF - Electrolytic capacitor 25 V | Rubycon |
| C11 | GRM188C81E105KAADD | 1 µF - Capacitor 25 V | |
| C12 | GRM188R71H103KA01D | 10 nF - Capacitor 50 V | |
| C13 | DE2E3KY222MA2BM01 | 2.2 nF - 250 V Capacitor X1/Y2 | |
| C14 | GRM185R60J225KE26D | 2.2 µF - Capacitor 6.3 V | |
| D1 | STTH1L06A | Ultrafast diode 1 A - 600 V | STMicroelectronics |
| D2, D3, D4 | BAT41ZFILM | Signal Schottky 0.15 A - 100 V | STMicroelectronics |
| D5 | MMSZ5248B-V-GS08 | Zener diode 18 V 0.5 W | |
| D6 | STPS5H100B | Power Schottky 100 V - 5 A | STMicroelectronics |
| L1 | B82144A2105J | 1 mH Axial Inductor | EPCOS |
| L2 | SD43-332ML | 3.3 µH – Power Inductor | Coilcraft |
| CM | 744821120 | 20 mH CM CHOKE | Wurth Elektronik |
| IC1 | VIPer38LE | Offline primary controller | STMicroelectronics |
| OPT | SFH610A-2 | Optocoupler | Vishay |
| REF | TS432ILT | Reference | STMicroelectronics |
| T1 | YJ-310V600210 | Flyback transformer | Yujingtech |

The transformer characteristics are listed in the table below.

**Table 3. Transformer characteristics**

| Parameter | Value |
|---|---|
| Manufacturer | Yujing Technology CO. LTD. |
| Part number | YJ-310V600210 |
| Primary inductance | 0.85 mH ± 10% |
| Leakage inductance | 40 µH Max |
| Primary turns (N1+N3) | 75 |
| Secondary turns (N2) | 12 |
| Auxiliary turns (N4) | 14 |
| Core | EEE-13 V |
| Ferrite | 3C94 Ferroxcube |

Figure 4. Dimensional drawing and pin placement diagram - bottom view

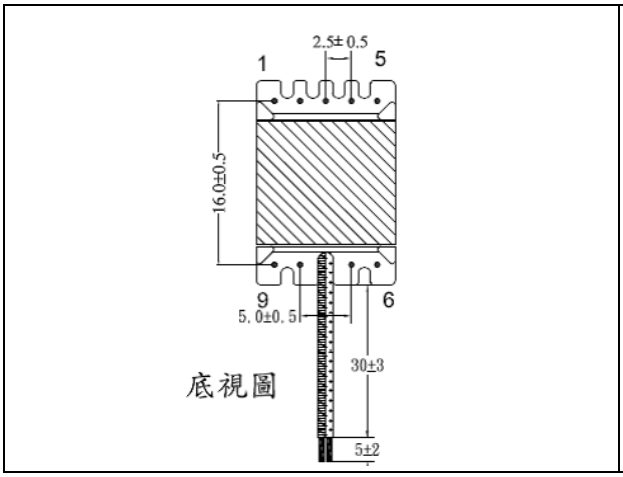



Figure 5. Dimensional drawing and pin placement diagram - electrical diagram

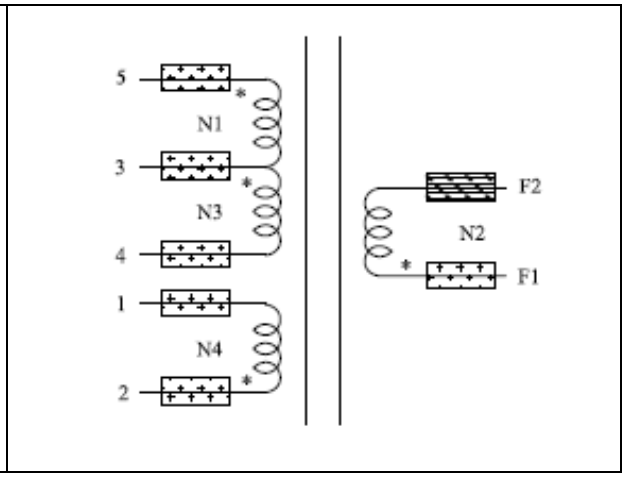
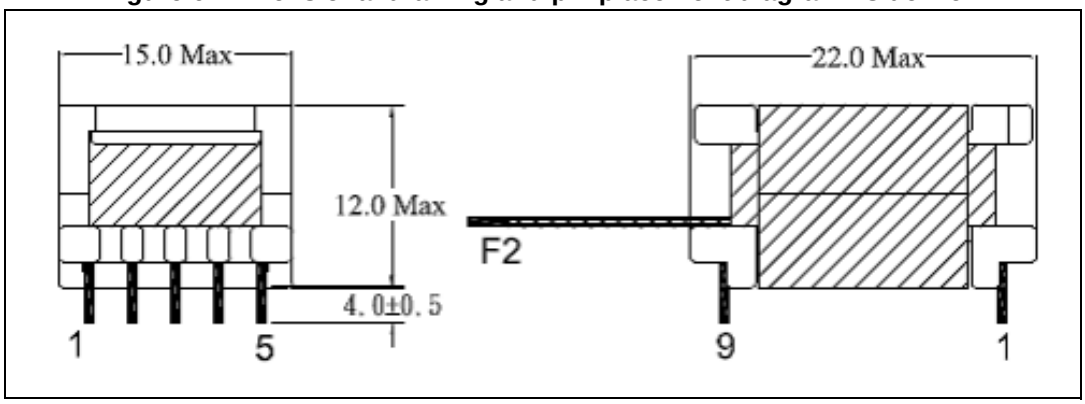



Figure 6. Dimensional drawing and pin placement diagram - side view




## 1.1 Output voltage characteristics

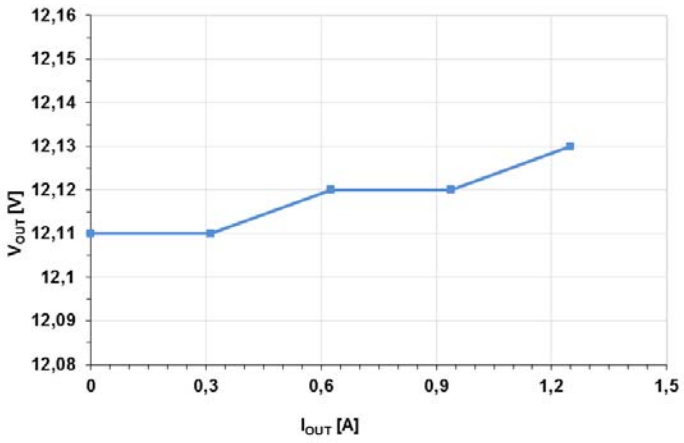
The output voltage of the board is measured in different line and load conditions. *Table 4* shows the results: the output voltage variation is negligible versus load and line variation.

As output voltage is low affected by line variations, just the load regulation at 230$V_{AC}$ is reported in *Figure 7*.

Table 4. Output voltage line-load regulation

| $V_{IN}$ [$V_{AC}$] | $V_{OUT}$ (V) | | | |
|---|---|---|---|---|
| | No load | 0.63 A | 0.94 A | 1.25 A |
| **90** | 12.12 | 12.12 | 12.13 | 12.14 |
| **115** | 12.12 | 12.12 | 12.13 | 12.14 |
| **150** | 12.12 | 12.12 | 12.13 | 12.14 |
| **180** | 12.12 | 12.12 | 12.12 | 12.13 |
| **230** | 12.11 | 12.12 | 12.12 | 12.13 |
| **265** | 12.11 | 12.12 | 12.12 | 12.13 |

Figure 7. Output voltage load regulation at 230 $V_{AC}$




## 1.2 Efficiency measurements

Any external power supply (EPS) must be capable to meet the international regulation agency limits. The European code of conduct (EC CoC Version 5) limit is taken as reference.

Since this power supply is considered a no low voltage power supply, the formula to calculate the minimum average efficiency is:

Table 5. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies)

| Nameplate output power (Pno) | Minimum average efficiency (expressed as a decimal) |
|---|---|
| 0 to ≤ 1 watt | ≥ 0.5 *Pno+0.146 |
| > 1 to ≤ 49 watts | ≥ [0.0626* In (Pno)]+ 0.646 |
| > 49 watts | ≥ 0.890 |

According to the above table, the minimum average efficiency is 81.55%, measured as average of the efficiencies at 25%, 50%, 75% and 100% of the rated output power at both 115 $V_{AC}$ and 230 $V_{AC}$.

Another requirement is the efficiency measured at 10% of the rated output power, according to the below table:

**Table 6. EC CoC version 5 energy-efficiency criteria for active mode (excluding low voltage external power supplies) at 10% maximum output load**

| Nameplate output power (Pno) | Minimum average efficiency (expressed as a decimal) |
|---|---|
| 0 to ≤ 1 watt | ≥ 0.5 *Pno+0.046 |
| > 1 to ≤ 49 watts | ≥ [0.0626* ln (Pno)]+ 0.546 |
| > 49 watts | ≥ 0.790 |

For the considered application the minimum efficiency is 71.55%. *Table 7* to *Table 9* show all the efficiency measurement results.

**Table 7. Average efficiency at 115 $V_{AC}$**

| %Load | $I_{OUT}$ (A) | $V_{OUT}$ (V) | $P_{IN}$ (W) | $P_{OUT}$ (W) | Efficiency (%) |
|---|---|---|---|---|---|
| 25% | 0.31 | 12.12 | 4.486 | 3.788 | 84.43 |
| 50% | 0.63 | 12.12 | 9.031 | 7.575 | 83.88 |
| 75% | 0.94 | 12.13 | 13.740 | 11.372 | 82.76 |
| 100% | 1.25 | 12.14 | 18.650 | 15.175 | 81.37 |
| **Average efficiency** | | | | | **83.11** |

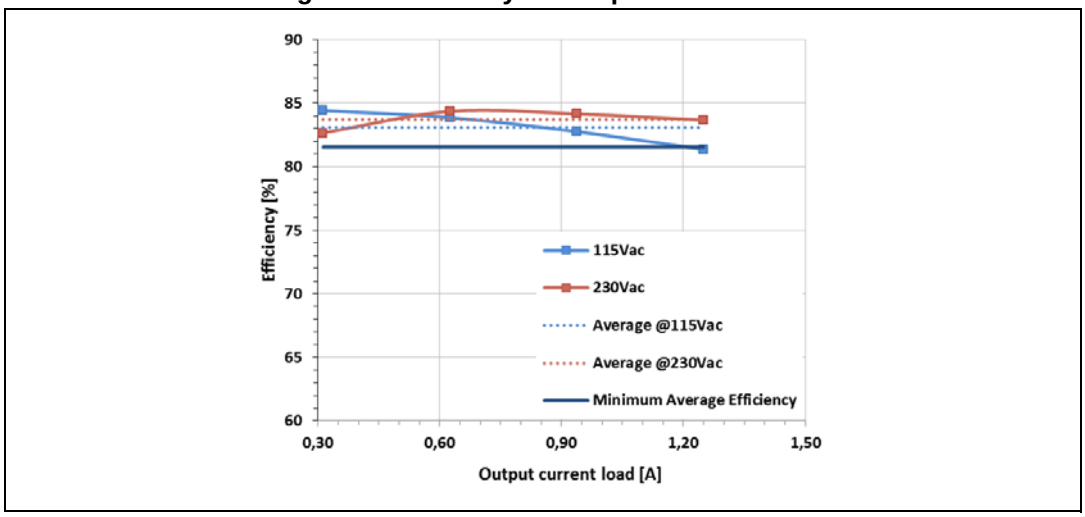
**Table 8. Average efficiency at 230 $V_{AC}$**

| %Load | $I_{OUT}$ (A) | $V_{OUT}$ (V) | $P_{IN}$ (W) | $P_{OUT}$ (W) | Efficiency (%) |
|---|---|---|---|---|---|
| 25% | 0.31 | 12.11 | 4.578 | 3.784 | 82.66 |
| 50% | 0.63 | 12.12 | 8.979 | 7.575 | 84.36 |
| 75% | 0.94 | 12.12 | 13.500 | 11.363 | 84.17 |
| 100% | 1.25 | 12.13 | 18.120 | 15.163 | 83.68 |
| **Average efficiency** | | | | | **83.72** |

**Table 9. Average efficiency at 10% of the max output load**

| $V_{IN}$ [$V_{AC}$] | $I_{OUT}$ (A) | $V_{OUT}$ (V) | $P_{IN}$ (W) | $P_{OUT}$ (W) | Efficiency (%) |
|---|---|---|---|---|---|
| 115 | 0.125 | 12.11 | 1.861 | 1.514 | **81.34** |
| 230 | 0.125 | 12.11 | 1.934 | 1.514 | **78.27** |

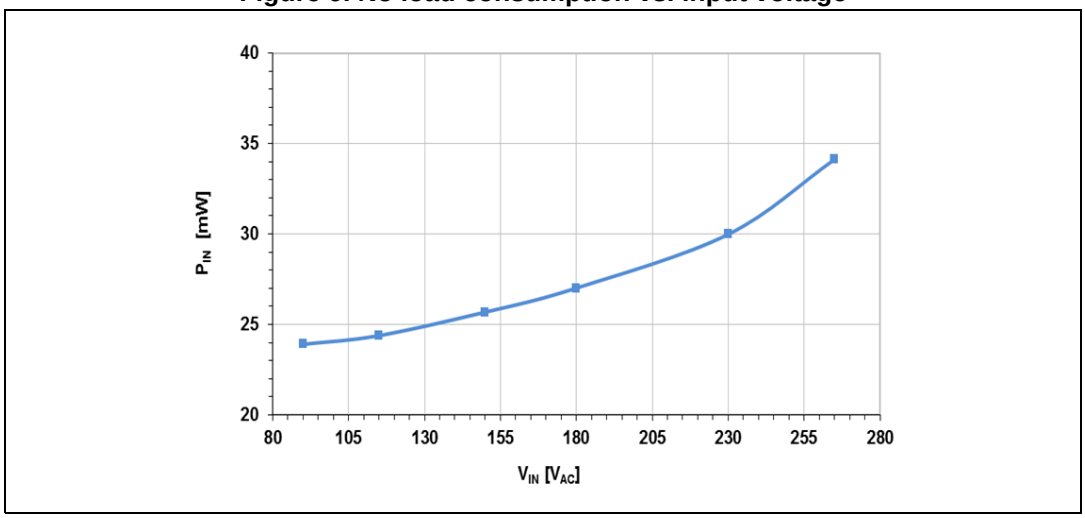
Figure 8. Efficiency vs. output current load




## 1.3 No load consumptions

The input power of the converter has been measured in no load, in this condition the converter works in burst mode so that the average switching frequency is reduced, thus minimizing the frequency related losses.

Figure 9. No load consumption vs. input voltage



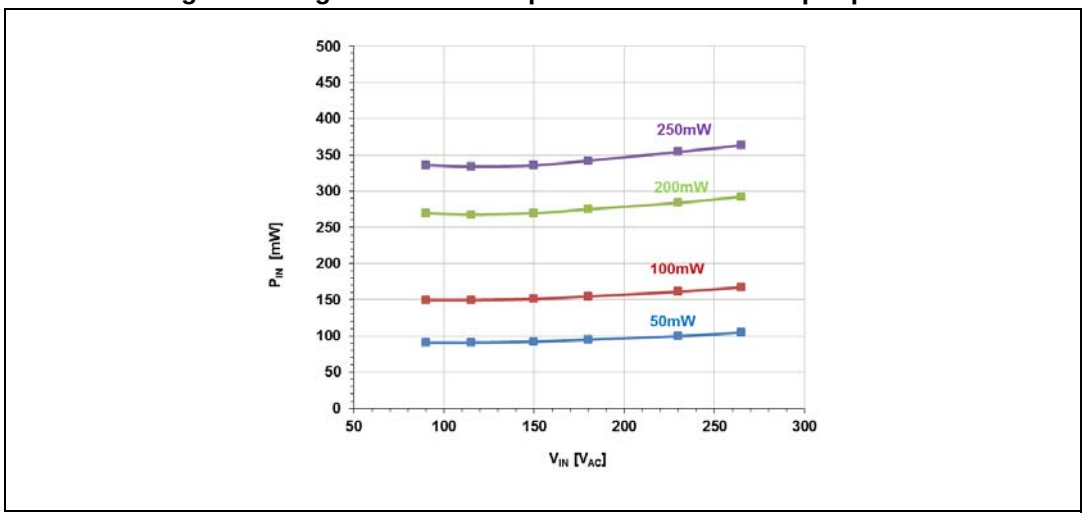

## 1.4 Light load consumption

Although the EC CoC hasn't other requirements regarding light load performance, in order to give quite complete information, the input power of the demo-board in light load conditions is reported.

In particular, in order to be complying with EuP Lot 6, the EPS requires an efficiency higher than 50% when the output load is 250 mW.

The presented demo meets also this requirement.

**Figure 10. Light load consumptions at different output power**



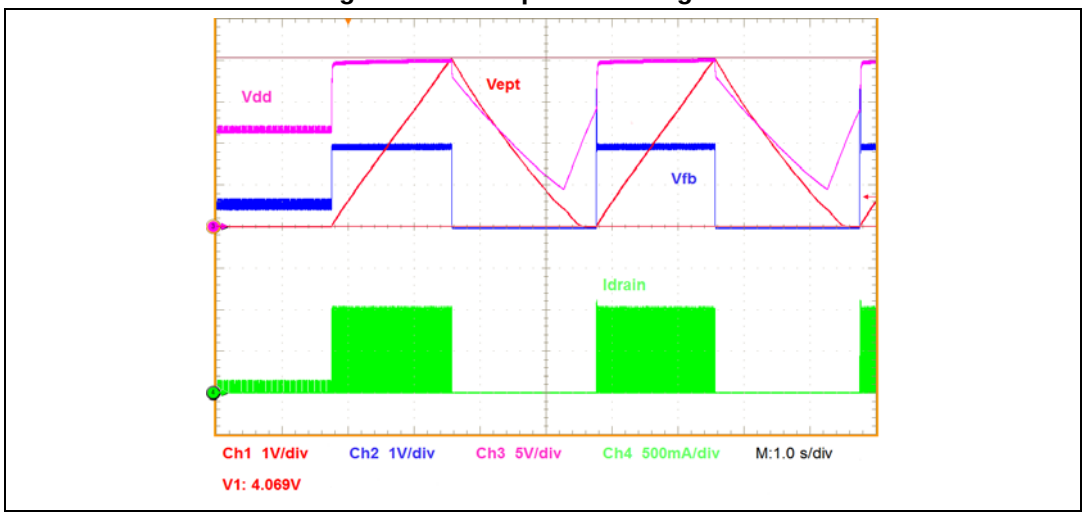
# 2 Extra power timer management function (EPT)

VIPer38 can manage an extra power for a limited time window during which the converter regulation has to be guaranteed.

This function is implemented by a capacitor connected on the EPT pin that is charged or discharged by means of a 5 µA internal current generator cycle by cycle. When the drain current raises over 85% of $I_{DLIM}$ value ($I_{DLIM\_EPT}$), the current generator charges C14 while, when the drain current is below $I_{DLIM\_EPT}$ value, discharges the capacitor. If the voltage across the C14 capacitor reaches the $V_{EPT}$ threshold (4 V typical), the converter is shut down.

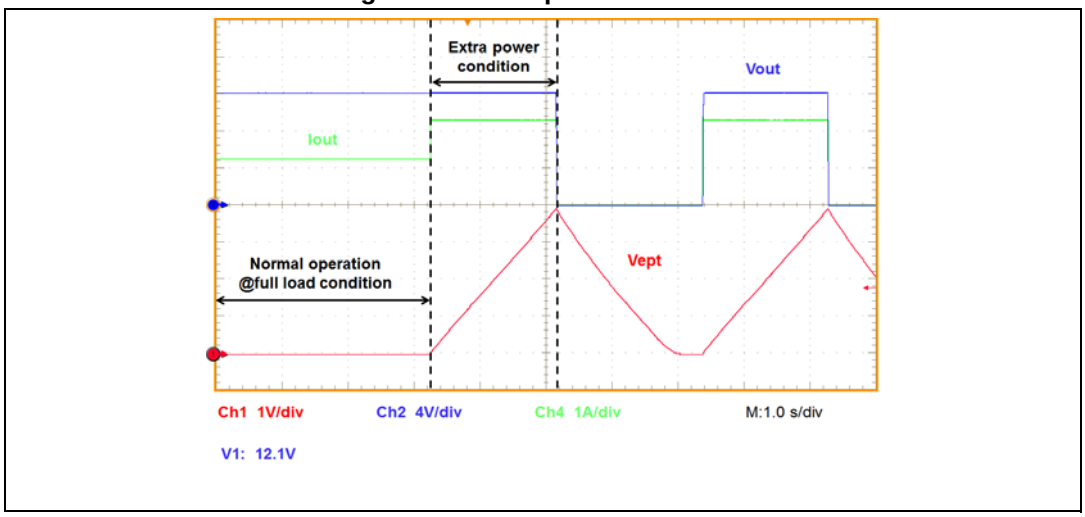
After the converter shut down, the $V_{DD}$ voltage will drop below the $V_{DDon}$ start up threshold and according to the auto restart operation the $V_{DD}$ pin voltage has to fall below the $V_{DD(RESTART)}$ (4.5 V typical) in order to charge again the $V_{DD}$ capacitor. Moreover the PWM operation is enabled again only when the voltage on EPT pin drops below the $V_{EPT(RESTART)}$ (0.6 V typical). Selecting a C14 value of 2.2 µF the extra power time is about 1.5 s, in this way it is possible to prevent the device overheating. The EPT pin must be connected to ground if the function is not used.

**Figure 11. Extra power management**




The *Figure 12* shows how the VIPer38 is able to manage an extra power for a limited period of time ensuring converter regulation during this time window ($V_{OUT}$ is constant to 12.1 V even during the extra power condition).

**Figure 12. Extra power condition**



# 3 Typical board waveforms

Drain voltage and current waveforms in full load condition are reported for minimum and maximum input voltage in *Figure 13* and *Figure 14*, and for the two nominal input voltages in *Figure 15* and *Figure 16* respectively.

**Figure 13. Drain current and voltage at full load at 90 $V_{AC}$**

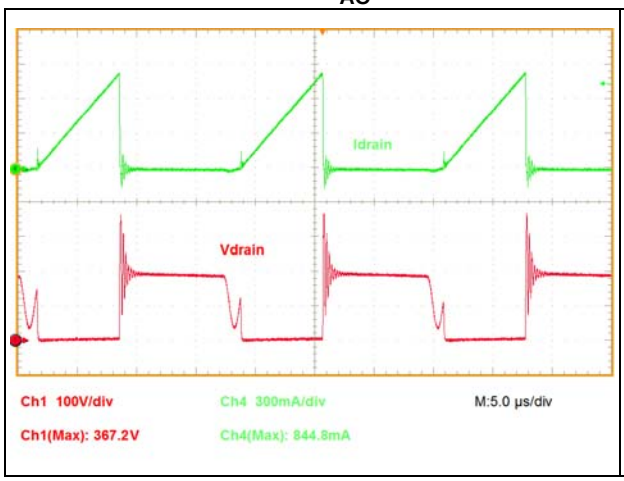



**Figure 14. Drain current and voltage at full load at 265 $V_{AC}$**

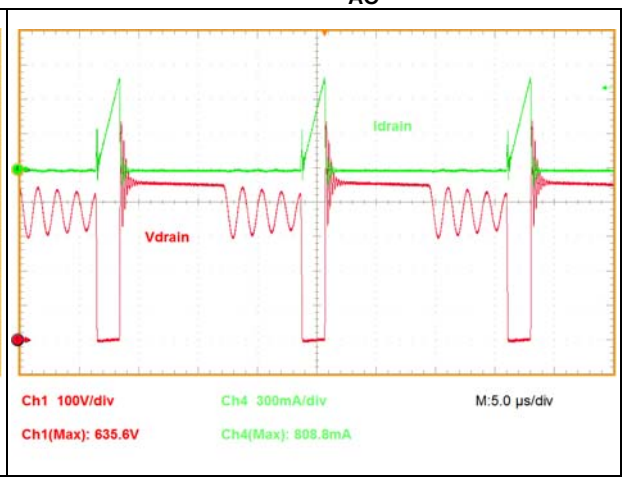



**Figure 15. Drain current and voltage at full load at 115 $V_{AC}$**

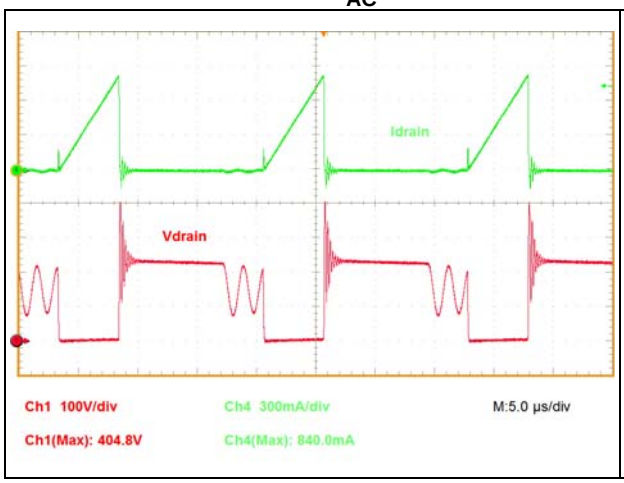
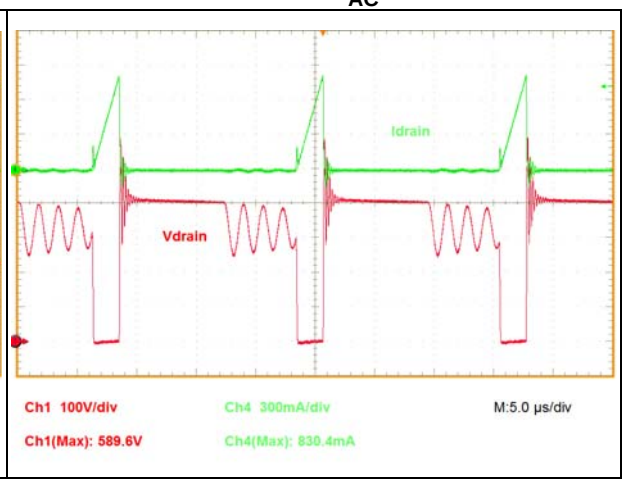



**Figure 16. Drain current and voltage at full load at 230 $V_{AC}$**




The output ripple at the switching frequency was also measured. The board is provided with LC filter, for further reduce the ripple without reducing the overall output capacitor's ESR.

The voltage ripple across the output connector ($V_{OUT}$) and before the LC filter ($V_{OUT\_PRE}$) was measured, in order to verify the effectiveness of the LC filter. The following two figures show voltage ripple at 115 $V_{AC}$ (*Figure 17*) and at 230 $V_{AC}$ (*Figure 18*) at full load condition.

Figure 17. Output voltage ripple at full load at 115 $V_{AC}$

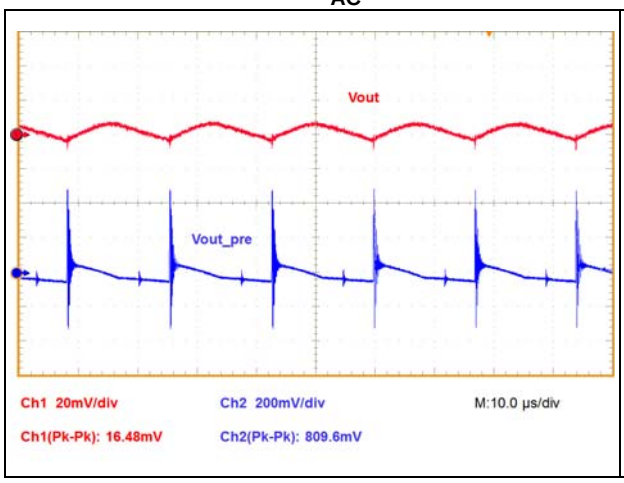
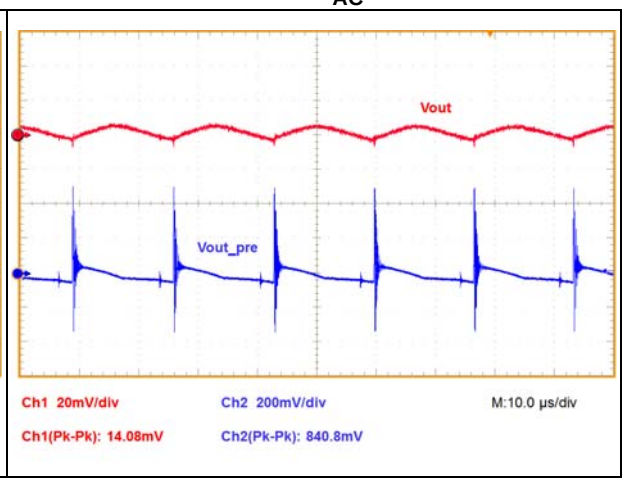



Figure 18. Output voltage ripple at full load at 230 $V_{AC}$




## 3.1 Dynamic step load regulation

In any power supply is important to measure the output voltage when the converter is submitted to dynamic load variations, in order to be sure that good stability is ensured and no overvoltage or undervoltage occurs.

The test has been performed, for both nominal input voltages, varying output load from 0 to 100% of nominal value.

In any tested conditions, no abnormal oscillations were noticed on the output and over/under shoot were well within acceptable values.

Figure 19. Dynamic step load (0 to 100% output load) at 115 $V_{AC}$

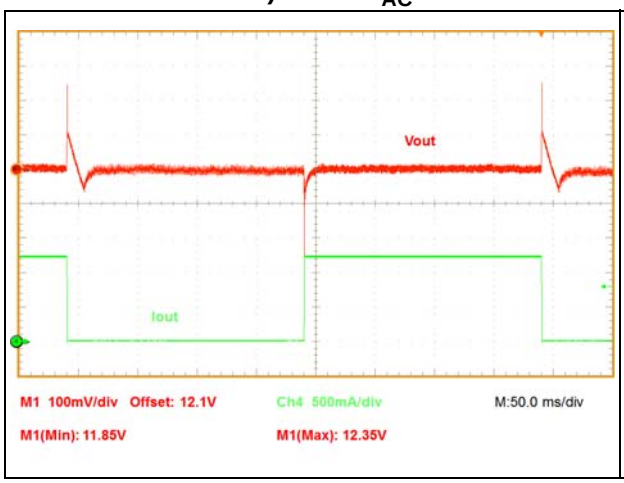
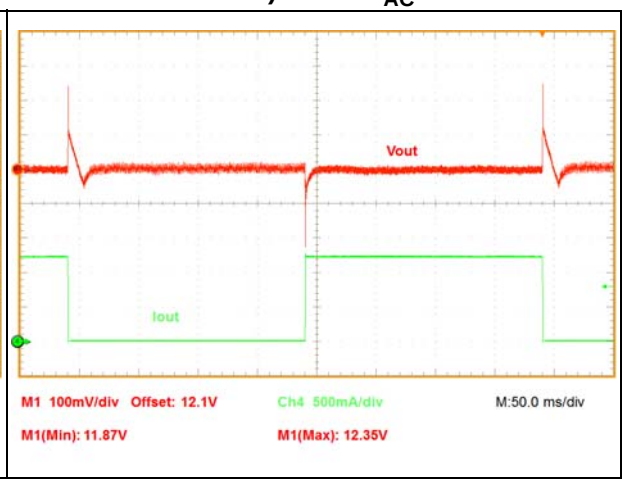



Figure 20. Dynamic step load (0 to 100% output load) at 230 $V_{AC}$



# 4 Soft-start

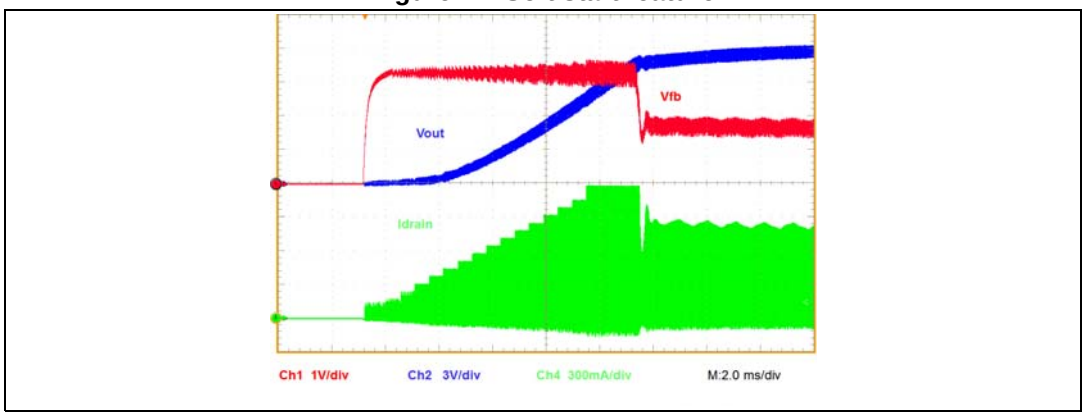
When the converter starts, the output capacitor is discharged and needs some time to reach the steady state condition. During this time, the power demand from the control loop is the maximum, while the reflected voltage is low. These two conditions could lead to a deep continuous operating mode of the converter.

Also, when the MOSFET is switched on, it cannot be switched off immediately as the minimum on time ($T_{ON\_MIN}$) has to be elapsed. Because of the deep continuous working mode of the converter, during this $T_{ON\_MIN}$, an excess of drain current can overstress the component of the converter as well as the device itself, the output diode and the transformer. Transformer saturation is also possible under these conditions.

To avoid all the described negative effects, the VIPer38 implements an internal soft-start feature. As the device starts to work, no matter the control loop request, the drain current is allowed to increase from zero to the maximum value gradually.

The drain current limit is increased in steps, and the values range from 0 to the fixed drain current limitation value (value that can be adjusted through an external resistor) is divided in 16 steps. Each step length is 64 switching cycles. The total length of the soft-start phase is about 8.5 ms. *Figure 21* shows the soft-start phase of the presented converter when it is operating at minimum line voltage and maximum load.

**Figure 21. Soft start feature**



# 5 Protection features

In order to increase end-product safety and reliability, VIPer38 has some protection features: overload protection, overvoltage protection, shorted secondary rectifier detection and transformer saturation protection.

In the following sections these protections are tested and the results are presented.

## 5.1 Overload and short circuit protection

When the load power demand increases, the feedback loop reacts increasing the voltage on pin. In this way the PWM current set point increases and the power delivered to the output rises. This process ends when the delivered power equals the load power request.

In case of overload or output short circuit (see *Figure 22*), the voltage on FB pin reaches the $V_{FBlin}$ value (3.5 V typical) and the drain current is limited to $I_{Dlim}$ (or the one set by the user through the $R_{LIM}$ resistor) by OCP comparator. In these conditions an internal current generator is activated and it charges the capacitor C8; when the voltage on FB pin reaches the $V_{FBolp}$ threshold (4.8 V typical), the converter is turned off and is not allowed to switch again until the $V_{DD}$ voltage falls below the $V_{DD\_RESTART}$ (4.5 V typical) and then rises to $V_{DDon}$ (14 V typical).

Overload condition can be obtained shorting the output connector. After the $V_{DD}$ voltage reaches the $V_{DDon}$ value, if the short-circuit is not removed, the system starts to work in auto-restart mode (see *Figure 23*): in this case the MOSFET switches for a short period of time, where the converter tries to deliver to the output as much power as it can, and a longer period where the device is not switching and no power is processed.

As the duty cycle of power delivery is very low (around 1.7%), the average power throughput is also very low, resulting in a very safe operation.

**Figure 22. Overload event, OLP triggering**

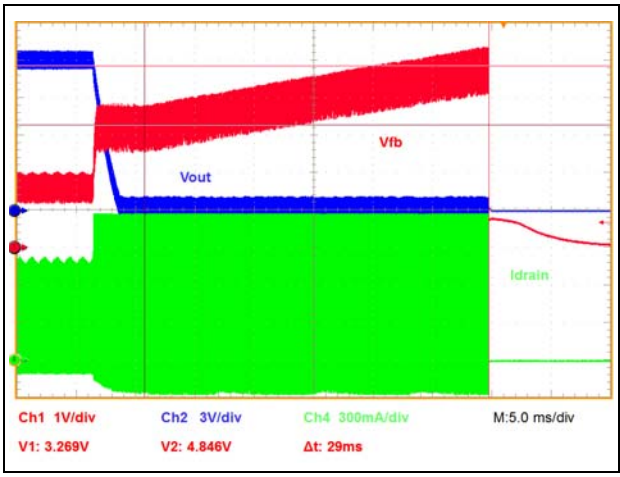
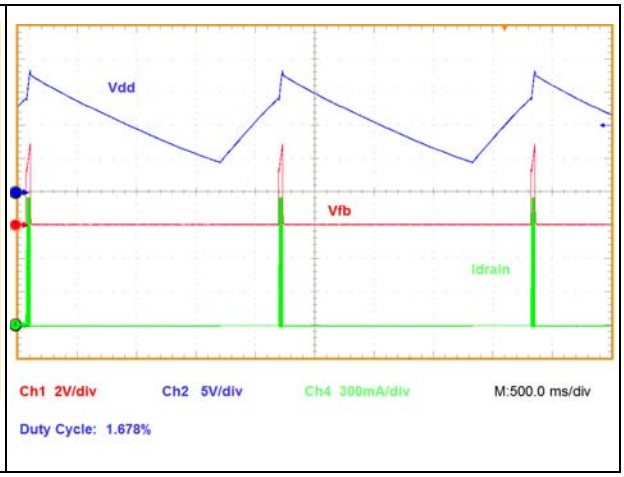



**Figure 23. Overload event, continuous overload**



## 5.2 Overvoltage protection

An output overvoltage protection is implemented monitoring the voltage across the auxiliary winding during the MOSFET turn off time, through the diode D3 and the resistor divider R3 and R4 connected on the CONT pin. If this voltage exceeds the $V_{OVP}$ (3 V typical) threshold, an overvoltage event is assumed and an internal counter is activated; if this event happens for four consecutive times, the controller recognizes an overvoltage condition and the device stops switching. This counter provides high noise immunity and avoids spikes erroneously tripping the protection. The counter is reset every time the OVP signal is not triggered in one oscillator cycle.

After the device has stopped switching, to re-enable operation, the $V_{DD}$ voltage must be recycled.

The protection can be tested by opening the resistor connected to the output voltage (R10). In this way, the converter operates in open loop and the excess of power with respect to the load, charges the output capacitance increasing the output voltage until the OVP is tripped and the converter stops switching.

In *Figure 24* and *Figure 25* it is possible to see that output voltage increases, and consequentially, the CONT pin voltage increases; as it reaches about 3 V the converter stops switching (at the same time the output voltage reaches about 16 V).

**Figure 24. Overvoltage event**

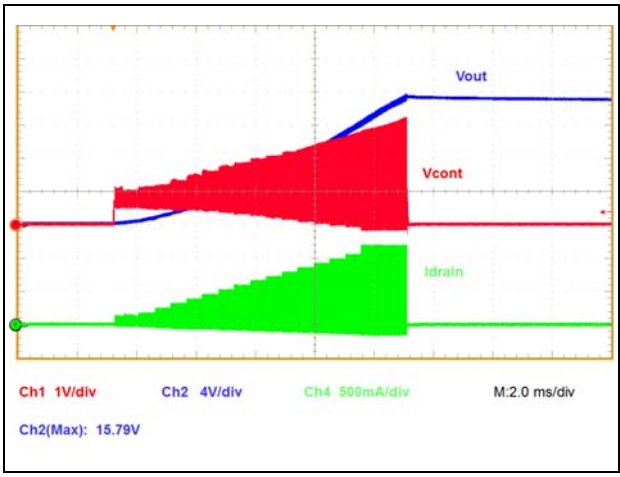
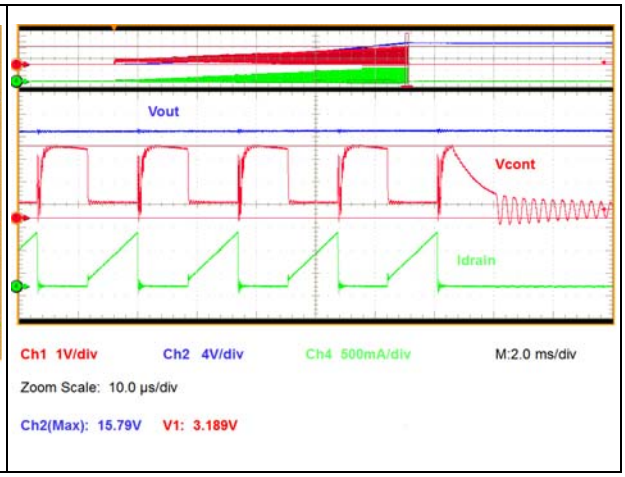



**Figure 25. Overvoltage magnification**



## 5.3 2nd level over current protection

The VIPer38 is protected against short circuit of the secondary rectifier, short circuit on the secondary windings or a hard saturation of flyback transformer. Such as anomalous condition is invoked when the drain current exceeds the threshold $I_{DMAX}$ (1.7 A typical).

To distinguish a real malfunction from a disturbance, a warning state is entered after the first signal trip. If in the subsequent switching cycle the signal is not tripped, a temporary disturbance is assumed and the protection logic will be reset; otherwise if the $I_{DMAX}$ threshold is exceeded for two consecutive switching cycles a real malfunction is assumed and the power MOSFET is turned off.

The shutdown condition is latched as long as the device is supplied. While it is disabled, no energy is transferred from the auxiliary winding; hence the $V_{DD}$ capacitor decays till the $V_{DD}$ under voltage threshold ($V_{DDoff}$), which clears the latch. $V_{DD}$ voltage recycles and if the fault condition is not removed the device enters in auto restart mode.

**Figure 26. 2nd level over current event**

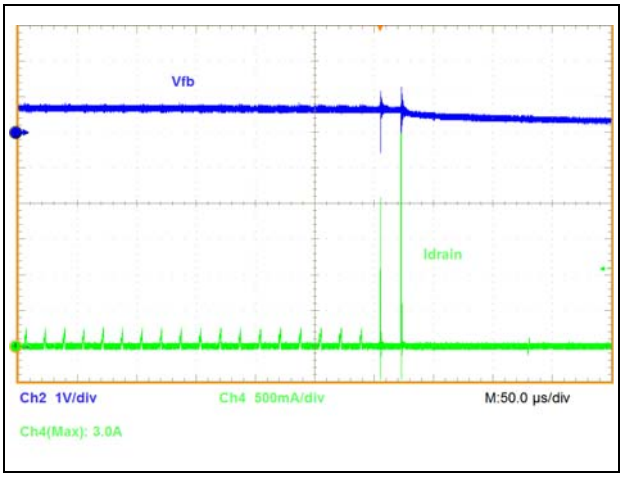
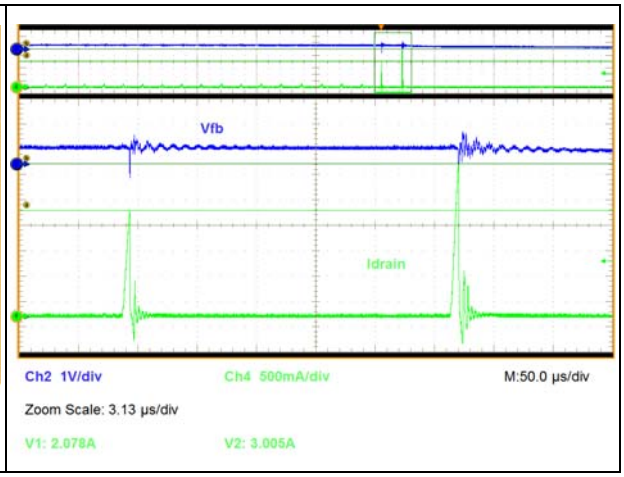



**Figure 27. 2nd level over current event magnification**



# 6 Conducted noise measurements

The VIPer38LE frequency jittering feature allows the spectrum to be spread over frequency bands, rather than being concentrated on single frequency value. Especially when measuring conducted emission with the average detection method, the level reduction can be several dB µV.

A pre-compliance test for the EN55022 (Class B) European normative was performed and peak measurements of the conducted noise emissions at full load and nominal mains voltages are shown in *Figure 28* and *Figure 29*. As seen in the diagrams, in all test conditions there is a good margin for the measurements with respect to the limits.

**Figure 28. CE peak measurement at 115 $V_{AC}$ full load**

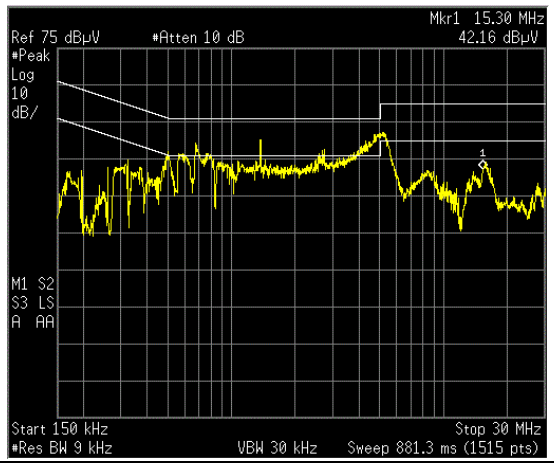
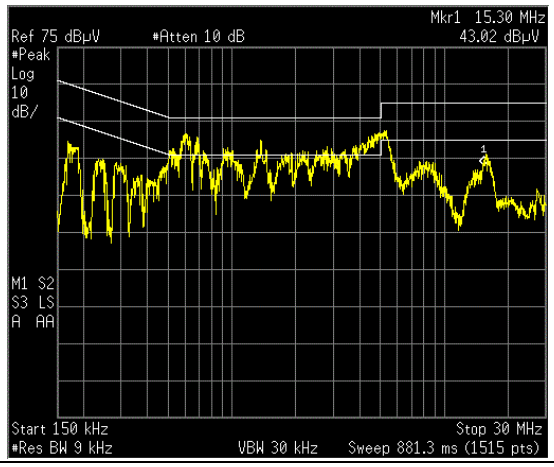



**Figure 29. CE peak measurement at 230 $V_{AC}$ full load**



# 7 Thermal measurements

A thermal analysis of the board has been performed using an IR camera for the two nominal input voltages ($115V_{AC}$ and $230V_{AC}$) in full load condition. The results are shown in *Figure 30* to *Figure 33* and summarized in *Table 10*.

**Figure 30. Thermal map at 115 $V_{AC}$ full load. Top layer**

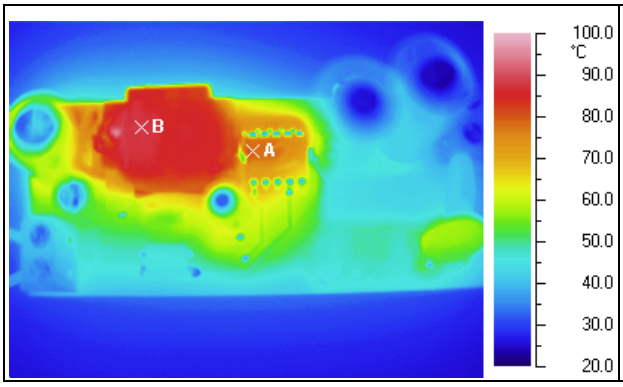



**Figure 31. Thermal map at 115 $V_{AC}$ full load. Bottom layer**

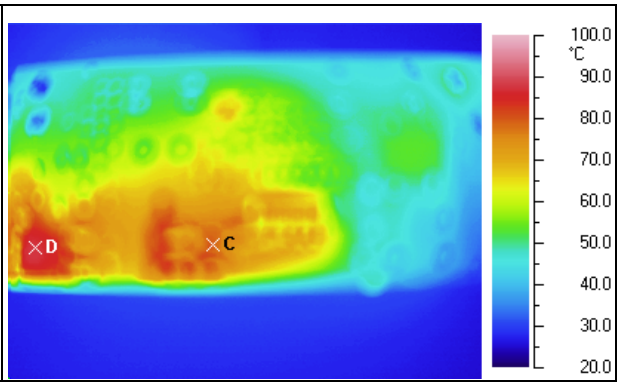



**Figure 32. Thermal map at 230 $V_{AC}$ full load. Top layer**

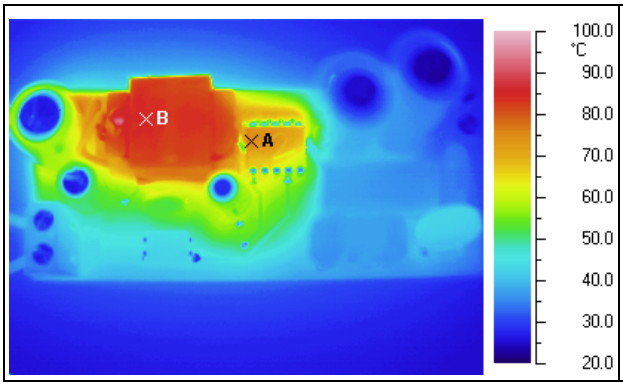



**Figure 33. Thermal map at 230 $V_{AC}$ full load. Bottom layer**

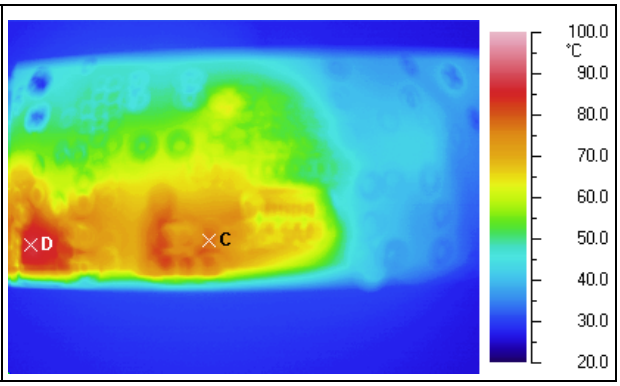



**Table 10. Temperature of key components ($T_{amb}$ = 25°C, emissivity = 0.95 for all points)**

| Point | Temp (°C) | | Reference |
|---|---|---|---|
| | 115 $V_{AC}$ | 230 $V_{AC}$ | |
| A | 79.5 | 76.7 | VIPer38LE |
| B | 88.5 | 85.4 | Transformer |
| C | 79.6 | 78.4 | Snubber diode |
| D | 87.7 | 87.2 | Output diode |

# 8 Conclusions

In this document a flyback has been described and characterized. Special attention was paid to efficiency and low load performances and the bench results were good with very low input power in light load condition. The efficiency performance have been compared with requirements of the EC CoC and DoE regulation programs for external AC-DC adapter with very good results, being the measured active mode efficiency always higher respect the minimum required.

Also the EMI emission are quite low, even is using low cost input filter.

# 9 References

The VIPER38LE evaluation board order code is: STEVAL-ISA153V1.

Further information about this product is available in the VIPER38 datasheet at www.st.com.

# 10 Revision history

Table 11. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 23-Jun-2014 | 1 | Initial release. |