AN4496

Application note

How to get a high power factor with the HVLED815PF device

Stefano Signoria

Introduction

The standard application of the HVLED8xxPF (HVLED807PF, HVLED815PF) is a constant current (CC) LED driver. The average output current I_{OUT}, as described in the HVLED815PF datasheet (section 4.5 Constant current operation), does not depend on the value or the waveform of the input voltage V_{IN}, then can be used in standard or high power factor implementation.

Two methods of implementing the high power factor (HPF) based on the HVLED8xxPF family are current in use: the current sense modulation and ILED modulation. In either case the input voltage after rectification is not smoothed and the waveform on the bulk capacitor is a semi-sinusoidal waveform. The voltage on the bulk capacitor, V_{RECT}, contains information about the phase and waveform of V_{IN}.

With the first method, the additional circuitry in *Figure 1* applies a DC offset and a modulation, both proportional to the V_{RECT}, to the CS pin and permits to obtain an HPF. This solution is described in detail in *1.* of *Section 3*.

The second one, shown in *Figure 2*, applies a modulation of the ILED pin proportional to the V_{RECT} and features HPF in a single range application (refer to the AN4129 for further details). This application note describes how to modify the basic circuit to support wide input range applications.

Figure 1. CS HPF; additional components

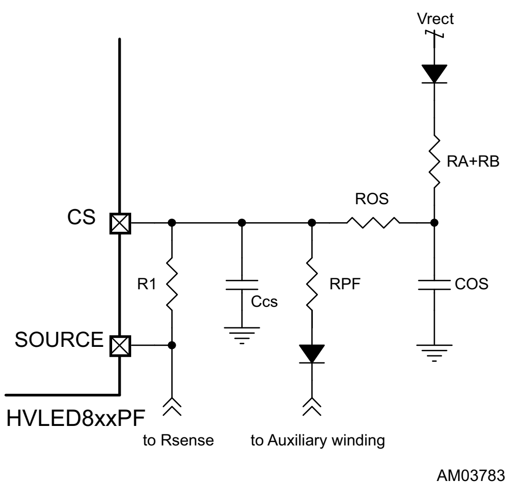
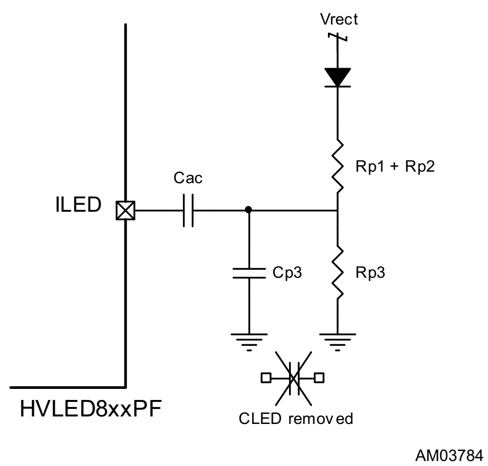


Figure 2. ILED HPF; additional component



Contents

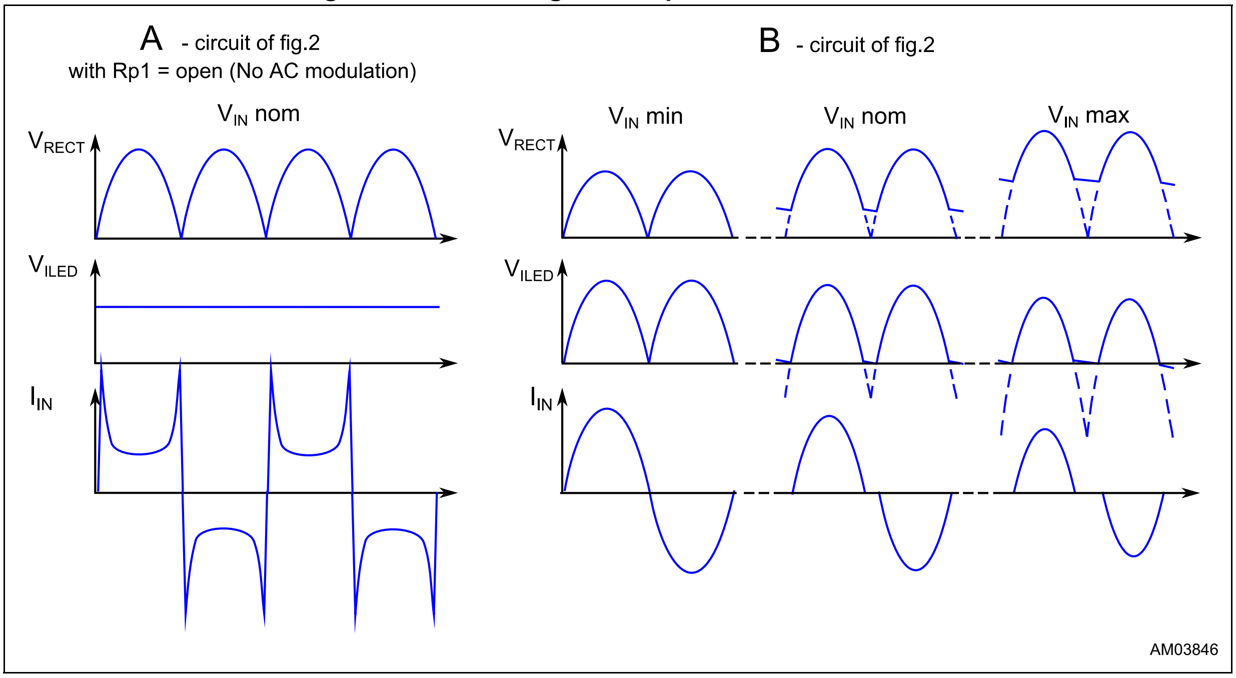
1 ILED pin

The ILED pin voltage (V_{ILED}) is the constant current (CC) loop reference. This voltage divided by two is used as the reference for the MOSFET's peak drain current during the CC regulation. An external capacitor is used for filtering the ILED pin current with an appropriate time constants ($\tau_{ILED} >> 1 / 2 * \pi * f_{IN}$).

In this configuration the peak of the drain current remains constant during the semi-period but the t_{ON} of the primary MOSFET increases when the instantaneous input voltage decreases and with the mains near the zero-crossing the MOSFET remains in the ON state until the mains voltage becomes enough to source the peak drain current.

Then near the zero-crossing the mains current has a peak as in *Figure 3* A.

Figure 3. ILED voltage and input current waveform



1.1 DC analysis

With a DC input voltage (V_{IN}) and the device working in the transition mode (TM), the voltage on the ILED, V_{ILED}, is:

Equation 1

$$V_{ILED} = 2 * V_{CLED} \left(1 + \frac{V_r}{\eta * V_{IN}}\right)$$

This voltage changes in function of mains voltage to maintain constant the output current and V_{ILED} reaches the maximum value at the minimum mains voltage.

In case of sinusoidal mains voltage, if the input current is in phase and with the same waveform of the input voltage (i.e.: HPF and THD > 30%), the *Equation 1* becomes:

Equation 2

$$V_{ILEDavg} = 2 * V_{CLED}\left(1 + \frac{V_r}{\eta * V_{INrms}}\right)$$

Where $V_{ILEDavg}$ is the average voltage on the ILED pin, obtained by integration (τ_{ILED} >> 1 / 2 * π * f_{IN}) of the ILED current in an external capacitor.

Figure 4 shows the calculated and measured values of the voltage V_{ILED} vs. V_{IN} with V_R = 102 V; the measurements are made on the board EVLHVLED815W10F at V_{OUT} nominal (22 V, V_R = 102 V). The difference between the curves, when the V_{IN} increases, is due to increasing of switching frequency and then greater power transferred in valley skipping (not TM) . *Figure 5* shows the calculated and measured values of the voltage V_{ILED} vs. V_{IN} with V_R = 70 V and V_R = 122 V; the measurements are made on the same board EVLHVLED815W10F changing the number of the LED and then V_{OUT} and V_R.

Figure 4. V_{ILED} at V_R = 102 V (V_{OUT}= 22 V)

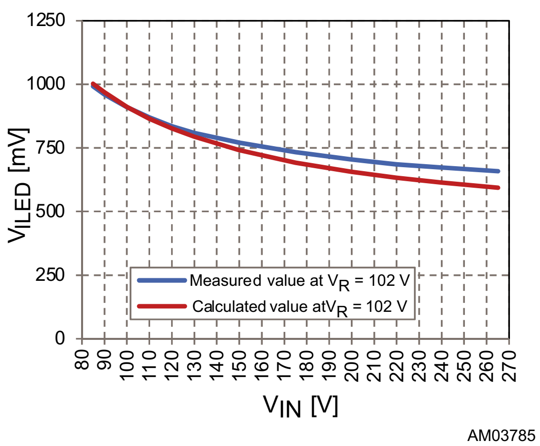
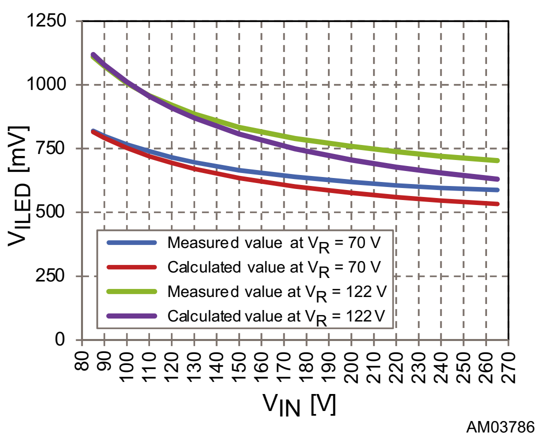


Figure 5. V_{ILED} at V_R = 70 V (V_{OUT} = 15 V) and V_{ILED} at V_R = 122 V (V_{OUT} = 26 V)



1.2 High power factor modulation analysis

A solution to obtain the high power factor and low THD, as shown in *Figure 2 on page 1*, is the AC coupling of the ILED pin with the rectified voltage. In this way the average of the voltage $V_{ILEDavg}$ is generated by the internal loop, which regulates the average output current, while the waveform is modulated through the voltage divider by V_{RECT} (see *Figure 3* B).

The average output voltage of an ideal single-phase full wave rectifier is:

Equation 3

$$V_{avg} = \frac{2}{\pi} * V_{peak}$$

Then the AC modulation is optimal when:

Equation 4

$$V_{ILEDavg} = \frac{2}{\pi} * V_{ILEDpeak}$$

To ensure accurate regulation, the peak voltage on the ILED pin ($V_{ILEDpeak}$) must be smaller than its maximum headroom voltage V_{ILEDx} (1.5 V). From *Equation 2* and *Equation 4* can be estimated the maximum reflected voltage:

Equation 5

$$V_{Rmax} = \eta_{VINmin} * V_{INmin} * \left(\frac{V_{ILEDx}}{\pi * V_{CLED}} - 1\right)$$

The effect of a reflected voltage greater of V_{Rmax} is the reduction of the output current when V_{IN} is lower than:

Equation 6

$$V_{IN} = \frac{V_R}{\eta_{VINmin} * \left(\frac{V_{ILEDx}}{\pi * V_{CLED}} - 1\right)}$$

The equivalent input resistance of the ILED pin (R_{inILED}) is 50 KΩ when $V_{ILEDavg}$ = 1 V and the voltage divider must drive the ILED pin with equivalent resistance $R_{AC} << R_{inILED}$. The phase rotation, at the input frequency, introduced from the capacitor CAC impacts on the power factor, then the value of the capacitor must be:

Equation 7

$$C_{AC} \geq 10 * \frac{1}{2 * \pi * f_{IN} * R_{AC}}$$

The selected value of V_R and V_{INmin} imposes the maximum value of:

Equation 8

$$V_{ILEDavg} = 2 * V_{CLED}\left(1 + \frac{V_{rR}}{\eta * V_{INmin}}\right)$$

Where V_{INmin} is the minimum RMS input voltage and η is the efficiency at the V_{IN} used in the equation.

The correct AC modulation is obtained setting the voltage divider ratio (K_{AC}) equal to:

Equation 9

$$K_{AC} = \frac{V_{RECT}}{V_{ILEDpk}} = \frac{\sqrt{2} * V_{INmin} - V_{drp}}{\frac{\pi}{2} * V_{ILEDavg}} = \frac{\sqrt{2} * V_{INmin} - V_{drp}}{\pi * V_{CLED}\left(1 + \frac{V_R}{\eta * V_{INmin}}\right)}$$

Where V_{drp} is the input drop voltage between V_{IN} and V_{RECT} (input bridge, input filter, fuse, etc.).

Referring *Figure 2 on page 1*, because K_{AC} is >> 1, then Rp3 can be set equal to R_{AC}:

Equation 10

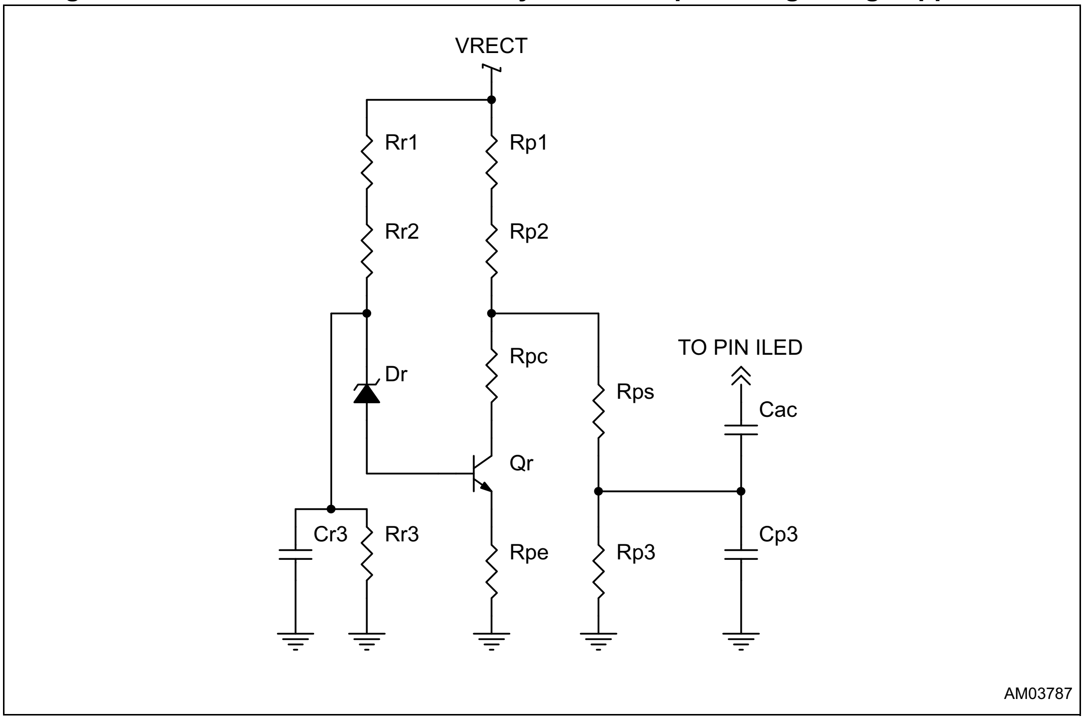
$$Rp1 + Rp2 = Rp3 * (K_{AC} - 1)$$

1.3 High power factor implementation in wide input range application

With the value of the components chosen in the previous paragraph, the AC modulation is optimized at the minimum input voltage. When the voltage increases, the ILED pin average voltage decreases, but the AC modulation increases and forces to zero the primary current for longer time near the zero crossing (see *Figure 3* B). The effect is the generation on the input current a zero crossing distortion, that initially, reduces the harmonics (and THD) of the flyback configuration, but when the input voltage reaches a value around 1.25 * V_{INmin}, the distortion begins again to increase. If is desired a THD under 20 - 25%, the ratio between the maximum and minimum of V_{IN} must be lower than 1.5.

In *Figure 6* is presented a solution that permit to cover wide-range application with THD under 20 - 25% and high PF. The circuitry uses in the low range (USA and Japan) a different voltage divider ratio (K_{AC}), than in the high range (European). The transistor Qr is used to change the voltage divider ratio between the value K_{ACL} in the US and Japanese and K_{ACH} in the European range.

Figure 6. Pin ILED modulation circuitry for wide input voltage range application



In the low range (88 V - 132 V) the transistor Qr is open and the circuit in *Figure 6* becomes as that in *Figure 7*. The value of K_{ACL} is obtained from *Equation 9*.

Equation 11

$$K_{ACL} = \frac{\sqrt{2} * V_{INmin} - V_{drp}}{\pi * V_{CLED}\left(1 + \frac{V_R}{\eta * V_{INmin}}\right)}$$

The sum Rp1 + Rp2 + Rps can be calculated by *Equation 10* that becomes:

Equation 12

Rp1 + Rp2 + Rps = Rp3 * (K_{ACL} - 1)

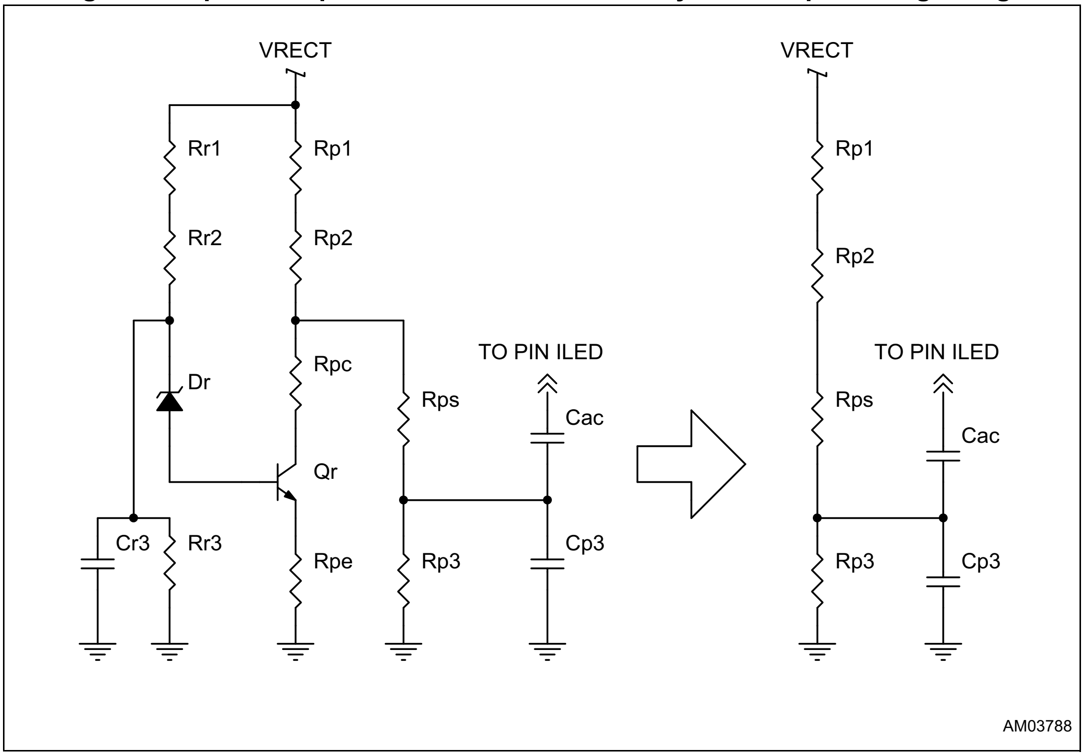
Where Rp3 = R_{AC} and Rph = Rp1 + Rp2.

Rph resistor is splitted into Rp1 and Rp2 to satisfy the maximum voltage ranting of the case, then Rp1 = Rp2, and choosing Rps = Rp1 / 3 permits to use a high value of Rpe.

Equation 13

Rp1 = Rp2 = 3 / 7 * Rp3 * (K_{ACL} - 1); Rps = 1 / 7 * Rp3 * (K_{ACL} - 1)

Figure 7. Equivalent pin ILED modulation circuitry in low input voltage range



In the high range (185 V - 265 V) the transistor Qr is saturated and the circuit in *Figure 6* becomes as that in *Figure 8*. The value of K_{ACH} is from *Equation 9*:

Equation 14

$$K_{ACH} = \frac{\sqrt{2} * V_{INminH} - V_{drp}}{\pi * V_{CLED}\left(1 + \frac{V_R}{\eta * V_{INminH}}\right)}$$

Where V_{INminH} is the high range minimum RMS input voltage and the value used for η and V_{drp} are the values at the V_{INminH}.

The value of Rpc + Rpe to obtain the selected value of K_{ACH} the will be:

Equation 15

$$Rpc + Rpe = \frac{(Rp1 + Rp2) * (Rps + Rp3)}{Rp3 * (K_{ACH} - 1) - Rp1 - Rp2 - Rps}$$

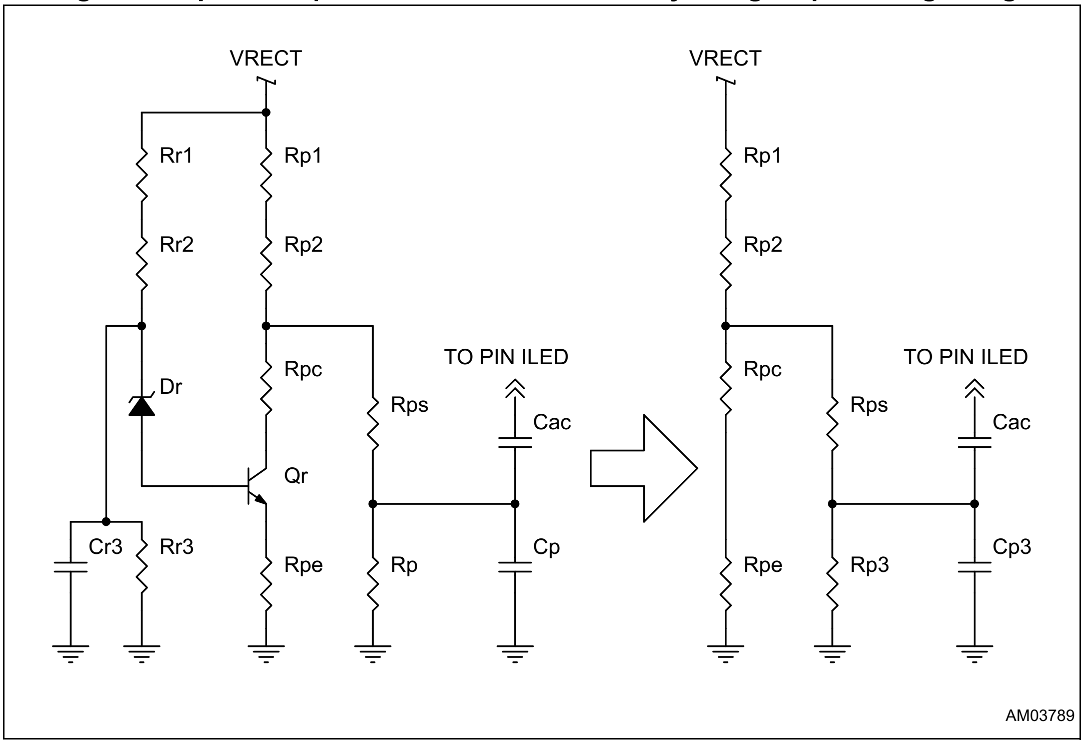
The resistors *Rr1*, *Rr2* and Rr3 implement a voltage divider. In parallel to the Rr3 is placed a capacitor Cr3 that filters the voltage ripple. When this voltage is greater than the sum of Dr Zener voltage (V_{Z_Dr}) and the base - emitter voltage of Qr (V_{BE_Qr}), the transistor Qr starts to switch on. The emitter resistor reduces the gain of Qr and permits a linear transition between the low and the high range, that allows to work without hysteresis and reduces the THD in the transition range (132 V -175 V).

Equation 16

$$Rr1 + Rr2 = \frac{\frac{2}{\pi} * \sqrt{2} * V_{INthL} * Rr3 - (V_{Z\_Dr} + V_{BE\_Qr})}{(V_{Z\_Dr} + V_{BE\_Qr})}$$

Where V_{INthL} is the lower transition voltage and Rr3 << (1 + hFE_Qr) * Rpe.

Figure 8. Equivalent pin ILED modulation circuitry in high input voltage range



The higher transition voltage (V_{INthL}) is determined by Rpe but the base of Qr is always biased while the collector voltage drops near to zero and modelling is not simple.

Starting from the below estimated values and the recommended value in *Section 2.10 on page 16* further fine tuning of the final application can be done assuming that:

- Decreasing/increasing the Dz Zener voltage the lower transition voltage decreases/increases
- Decreasing/increasing the Rr3 resistor value the lower and the higher transition voltage increase/decrease
- Decreasing/increasing the Rr1, Rr2 resistor value the lower and the higher transition voltage decrease/increase
- Decreasing/increasing the Rpe resistor value the spread between the lower and the higher transition voltage decreases/increases.

2 Designing a high PF wide range LED driver with the HVLED815PF

Main characteristics and circuit description

The main characteristics of the LED driver are listed here:

- Universal input mains range: 88 ÷ 265 VAC
- Output power 10 W continuous operation
- Output current: 460 mA at 22 V continuous operation
- Overall efficiency up to 85%
- Power factor higher than 0.95

2.1 Input specification

The following is a possible design procedure for a high power factor LED driver using the HVLED815PF device. This design is referred to the schematics of *Figure 9*. First step is to define the design specification.

Minimum mains voltage [VAC rms]:

Equation 17

$$V_{IN\ min} = 88\ V$$

Maximum mains voltage [VAC rms]:

Equation 18

$$V_{IN\ max} = 265\ V$$

Range (wide, US or European) = WIDE; in the European range maximum output power is 15 W, in an other case must be limited to 9 - 10 W. If the mains voltage range is a single range, the switch range network can be omitted (R13, D4, D7, Q2, R21, R20, R4). In a wide mains voltage range the network switches smoothly between the US range and European range.

Minimum mains frequency [Hz]:

Equation 19

$$F_{IN\ min} = 47\ Hz$$

Mean output current [mA]:

Equation 20

$$I_{OUT} = 460\ mA$$

Output current ripple [%]:

Equation 21

$$\Delta I_{OUT} = 140\ \%$$

Mean output voltage [V]:

Equation 22

$$V_{OUT} = 21.7\ V$$

The mean voltage LED string drop is the output voltage.

Overvoltage protection [V]:

Equation 23

$$V_{OVP} = 29\ V$$

The output voltage V_{OUT} has a ripple at twice the line frequency and whose amplitude is proportional to the output current and reverse proportional to output capacitance. This application has a high ripple voltage (due to the high power factor and small bulk capacitor). With a mean output voltage of 22 V the peak is at 25 V.

For reliability the output capacitor has a rated voltage of 35 V.

The selected OVP threshold of 29 V is set between these two limits (the peak output voltage and output capacitor rated voltage).

Supply voltage of the device [V]:

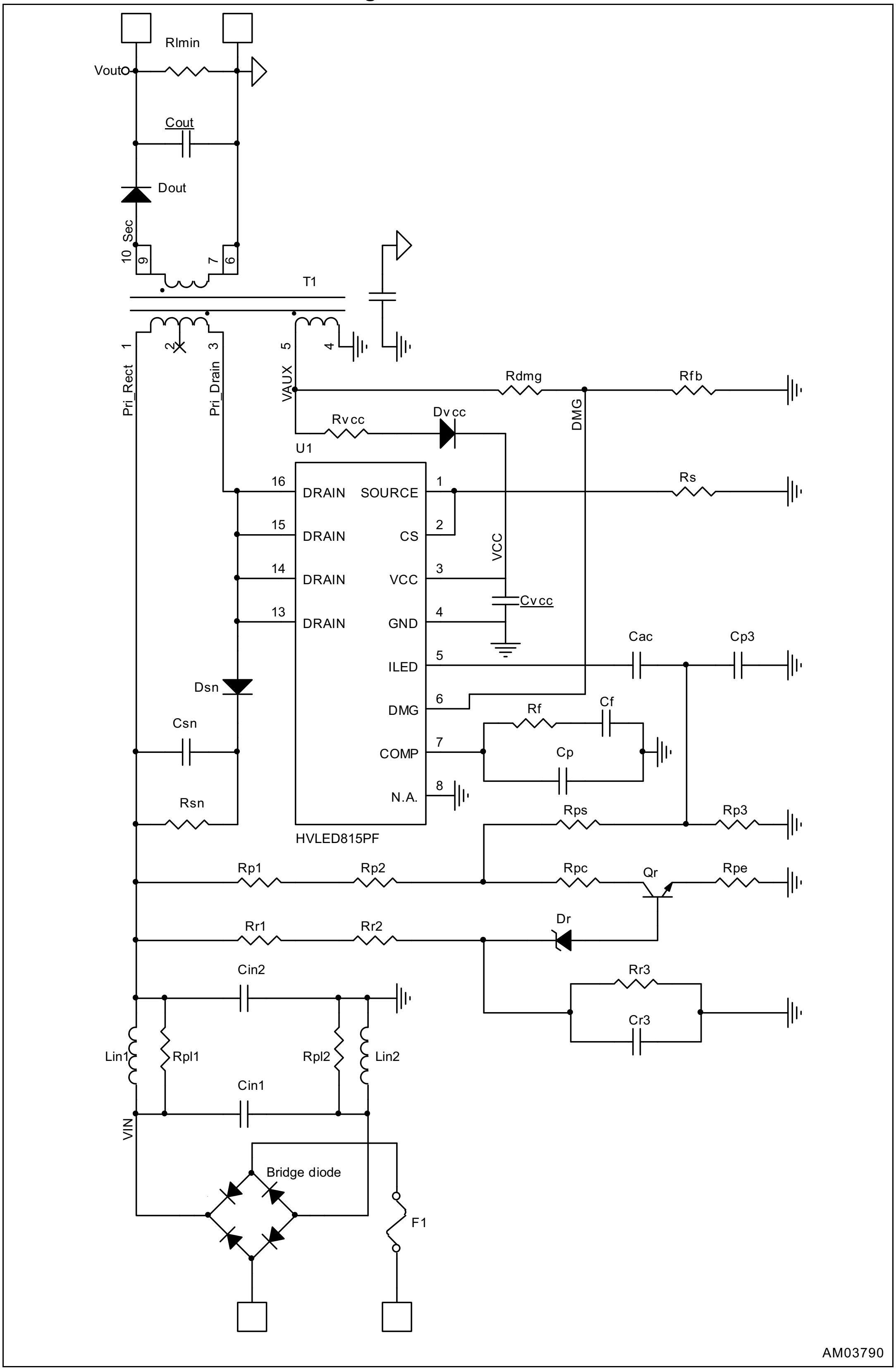
Equation 24

$$V_{CC} = 12\ V$$

In this design the supply voltage Vcc is low. That value is selected, because in this design the output voltage is fixed to 22 V. A higher value of Vcc is recommended (until 18 - 21 V) in case of application with variable output voltage [example: Iout = 460 mA, Vout = 14 V ~ 22 V)].

The efficiency is better if the supply current is sourced from the auxiliary winding rather than from the high voltage startup.

Figure 9. Schematic



2.2 Operating conditions

The first step is to verify:

Maximum power output [W]:

Equation 25

$$P_{OUT} = I_{OUT} * V_{OUT} \leq P_{OUT\_MAX}$$

In the European range ($V_{IN\ min}$ > 175 V) → $P_{OUT\ max}$ < 15 W

In the US and Japanese range ($V_{IN\ min}$ < 175 V) → $P_{OUT\ max}$ < 10 W.

2.3 Transformer design

The voltage at the ILED pin must be limited at 1.5 V.

Then for the best performance the optimal reflected voltage V_{Ropt} must be set for using all the dynamics of the ILED pin at minimum mains.

Equation 26

$$V_{Ropt} = \eta_{VINmin} * V_{INmin} * \left(\frac{V_{ILEDx}}{\pi * V_{CLED}} - 1\right) = 98\ V$$

Where:

η_{VINmin} = 80% → efficiency at minimum input voltage

V_{ILEDx} = 1.5 V → pin ILED maximum voltage

2.4 Drain source breakdown

Reflected voltage can be limited by drain-source breakdown voltage.

Equation 27

$$V_{Rbrk} = V_{(BR)DSS} - \sqrt{2} * V_{INmax} - V_{Spike} - V_{tol} = 800 - \sqrt{2} * 265 - 150 - 80 = 200\ V$$

Where V_{tol} is a margin for the components tolerance.

The value of V_R lower than V_{Ropt} and V_{Rbrk} is used to calculate the primary/secondary turns ratio *n*:

Equation 28

$$n = \frac{V_R}{V_{OUT} + V_{Fsec}} = \frac{98}{21.7 + 0.4} = 4.42$$

Where V_{Fsec} = secondary diode forward drop voltage.

When V_R is lower than V_{Ropt}, the dynamic is not optimized but the HVLED815PF device is working without problem.

Real value used: n = 4.52 → V_R = 100 V

2.5 Current sense resistor

Current sense resistor value is determined by the average LED current I_{OUT}.

Equation 29

$$R_S = \frac{n}{2} * \frac{V_{CLED}}{I_{OUT}} = \frac{4.52}{2} * \frac{0.2}{0.46} = 0.98\Omega$$

This formula is exact if:

- The peak voltage on the ILED pin is smaller than the maximum headroom voltage for all mains voltage range.
- OVP protection is set 20% over the maximum output peak voltage.
- Perfect transformer coupling.
- The LED driver works in the TM mode for over an half of the semi-period.

For different designs, fine tuning may be needed, but once the final values are selected, repeatability from unit to unit is excellent.

Real value used: **R_S = 1 Ω**

2.6 Primary inductance

The primary inductance L_p sets the working frequency.

For the best regulation is better to limit the minimum frequency at maximum mains voltage (265 V) to 90 KHz, in this way when the voltage is around the peak of the semi-period (and the instantaneous power is higher), the LED driver operates in transition mode (TM). In wide range application, at minimum mains voltage (88 V), this frequency drops to the minimum $f_{min} \approx 40$ KHz.

Equation 30

$$L_p = \frac{\sqrt{2} * V_{INmin}}{\left(1 + \frac{\sqrt{2} * V_{INmin}}{V_R}\right) * f_{min} * \frac{V_{ILEDx}}{2 * R_S}} = \frac{\sqrt{2} * 88}{\left(1 + \frac{\sqrt{2} * 88}{98}\right) * 50 * 10^3 * \frac{1.5}{2 * 1}} = 1.5\ \mathrm{mH}$$

The increase f_{min} reduces the primary inductance and the transformer can be smaller. In this case K_{Rs} can be used to compensate divergence of I_{OUT} from the case with optimal frequency.

Real value used: **L_P = 1.5 mH**

2.7 Secondary/auxiliary turn ratio

The operating range of V_{CC} is between 11.5 V and 23 V. The mid voltage is around 17 V.

The drop voltage on the limiting resistor R_{lim} (R9) and the auxiliary rectifier diode (D2) at the nominal operating point is set to 1 V.

Equation 31

$$V_{drop\ AUX} = V_{Faux} + V_{Rlim} = V_{Faux} + I_{CC} * R_{lim}$$

Then is defined the secondary/auxiliary turn ratio.

Equation 32

$$\frac{N_S}{N_{AUX}} = \frac{V_{OUT} + V_{Fsec}}{V_{CC} + V_{drop\ AUX}} = \frac{22 + 0.7}{12 + 1}$$

Two conditions must be checked:

1. In case of an open circuit the output voltage is a bit upper at the threshold $V_{OUT\ OVP}$, in this situation R_{lim} must limit the current to 25 mA.

Equation 33

$$R_{lim} = \frac{\frac{N_{AUX}}{N_S} * (V_{OUT\ OVP} + V_{Fsec}) - V_{Zmin}}{I_{CCmax}}$$

$$R_{lim} = \frac{V_{drop\ AUX} - V_{Faux}}{I_{CC}}$$

The higher value of R_{lim} must be used in the design, if greater R_{lim} is determined for the open circuit conditions, the secondary/auxiliary turn ratio to compensate the drop on R_{lim} must be recalculated.

2. If requested, wide range output voltage at the constant current V_{CC} must be increased to 21 V.

To demonstrate the high voltage startup functionality in this design V_{CC} is lower, then:

Real value used: **N_S / N_{AUX} = 1.75** → **V_{CC} = 12 V**

2.8 Feed forward

Equation 34

$$R_{dmg} = \frac{N_{AUX}}{N_P} * \frac{L_P * R_{FF}}{T_D * R_S} = \frac{N_{AUX}}{N_S} * \frac{N_S}{N_P} * \frac{L_P * R_{FF}}{T_D * R_S} = \frac{1}{1.75} * \frac{1}{4.52} * \frac{1.5 * 10^{-3} * 45}{100 * 10^{-9} * 1} = 86k\Omega$$

Real value used: Rdmg = 91 kΩ

2.9 OVP protection

In *Section 2.1 on page 10* the selected value V_{OUT_OVP} = 29 V, then:

Equation 35

$$R_{fb} = \frac{R_{dmg} * V_{ref}}{V_{OUT\,OVP} * \frac{N_S}{N_{AUX}} - V_{ref}} = \frac{91 * 10^3 * 2.5}{29 * 1.74 - 2.5} = 16.2k\Omega$$

Real value used: Rfb = 16kΩ

2.10 AC modulation

To obtain the high power factor and low THD, a signal proportional to rectified mains is applied to the ILED pin.

The other components of the network that switching the range can be calculated, but the non-linear behavior of Qr due the modulation of the Qr collector requires a fine tuning of the network; using the next recommended value for the components, the only value to be calculated is R3 to optimize the modulation at 85 - 90 V.

Equation 36

$$Rp3 = \frac{Rp1 + Rp2 + Rps}{(K_{ACL} - 1)} = 6.2k\Omega$$

With:

Rp1 = Rp2 = 180 kΩ

Rps = 120 kΩ

Rpc = 51 kΩ

Rpe = 15 kΩ

Rr1 = Rr2 = 120 kΩ

Rr3 = 62 kΩ

Cr3 = 4.7 µF

Dr = BZV55-C20

Qr = MMBTA42

3 Supporting material

Documentation

1. HVLED815PF - “Offline LED driver with primary-sensing and high power factor up to 15 W” datasheet.
2. AN4129 - “STEVAL-ILL044V1: 9 W Triac dimmable, high power factor, isolated LED driver based on the HVLED815PF (for US market)”.

4 Revision history

Table 1. Document revision history

Date	Revision	Changes
08-Sep-2014	1	Initial release.