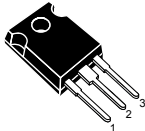




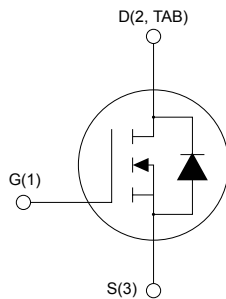
N-channel 500 V, 100 mΩ typ., 22 A MDmesh II Power MOSFETs in D²PAK and TO-247 packages



D²PAK



TO-247



AM01475v1_noZen



Product status links

[STB32NM50N](#)

[STW32NM50N](#)

Product summary

Order code	STB32NM50N
Marking	32NM50N
Package	D ² PAK
Packing	Tape and reel
Order code	STW32NM50N
Marking	32NM50N
Package	TO-247
Packing	Tube

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB32NM50N	500 V	130 mΩ	22 A
STW32NM50N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	500	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	22	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	13.86	
$I_{DM}^{(1)}$	Drain current (pulsed)	88	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	190	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Maximum operating junction temperature	150	$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 22\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DS(peak)} \leq V_{(BR)DSS}$, $V_{DD} = 400$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.66		$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	30 ⁽¹⁾	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on a standard 1 inch² area of FR-4 PCB with 2-oz copper.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	7	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	340	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	500			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 500\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 11\text{ A}$		100	130	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1973	-	pF
C_{oss}	Output capacitance		-	179	-	pF
C_{rss}	Reverse transfer capacitance		-	9.7	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }400\text{ V}$, $V_{GS} = 0\text{ V}$	-	325	-	pF
Q_g	Total gate charge	$V_{DD} = 400\text{ V}$, $I_D = 22\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see the Figure 16. Test circuit for gate charge behavior)	-	62.5	-	nC
Q_{gs}	Gate-source charge		-	8.6	-	nC
Q_{gd}	Gate-drain charge		-	33	-	nC
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	3.8	-	Ω

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$, $I_D = 11\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	21.5	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off delay time	(see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	110	-	ns
t_f	Fall time		-	23.6	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		22	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		88	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	328		ns
Q_{rr}	Reverse recovery charge		-	5		μC
I_{RRM}	Reverse recovery current		-	30.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 22\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	392		ns
Q_{rr}	Reverse recovery charge		-	6.5		μC
I_{RRM}	Reverse recovery current		-	32.8		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

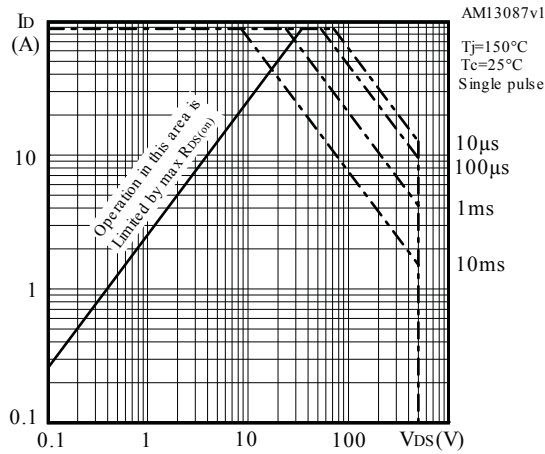
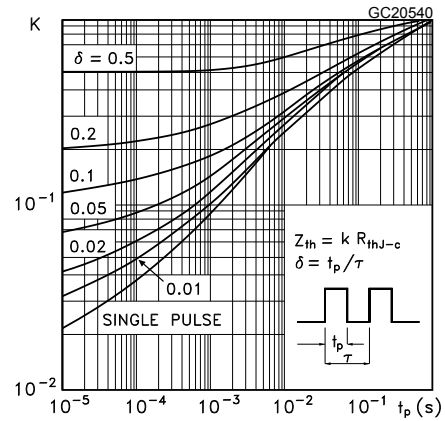
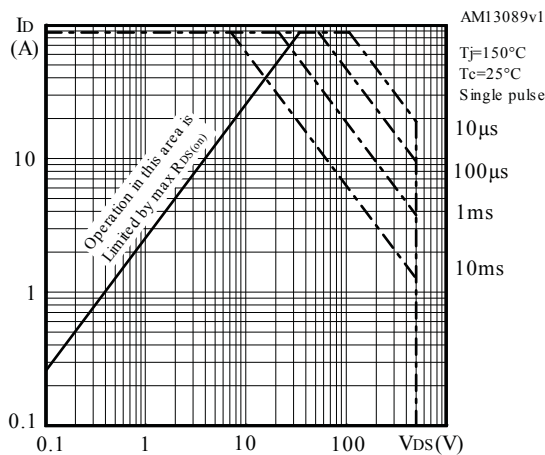
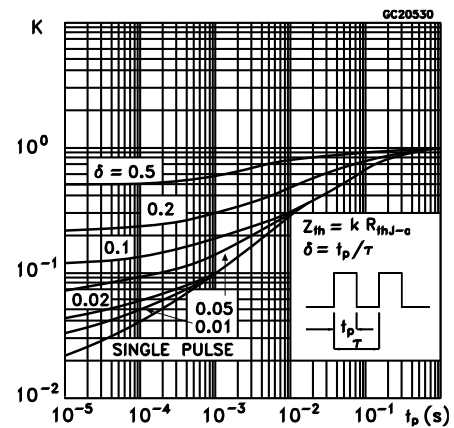
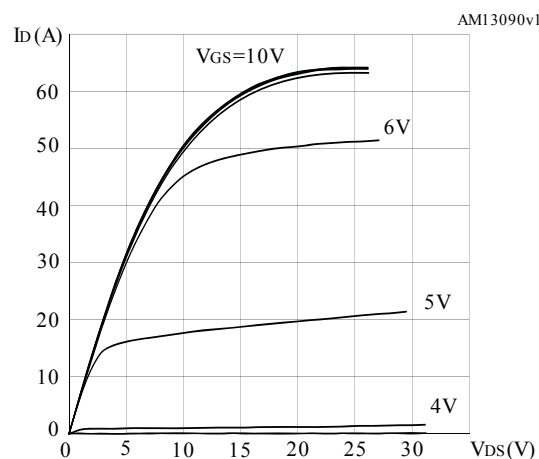
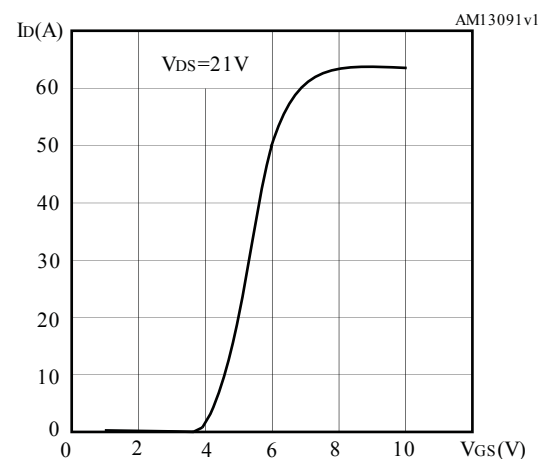
Figure 1. Safe operating area for D²PAK

Figure 2. Normalized transient thermal impedance for D²PAK

Figure 3. Safe operating area for TO-247

Figure 4. Normalized transient thermal impedance for TO-247

Figure 5. Typical output characteristics

Figure 6. Typical transfer characteristics


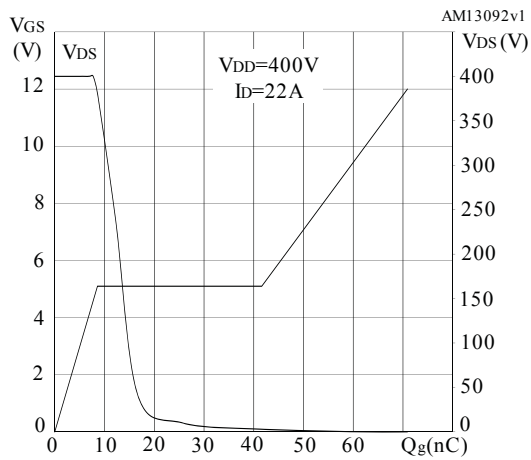
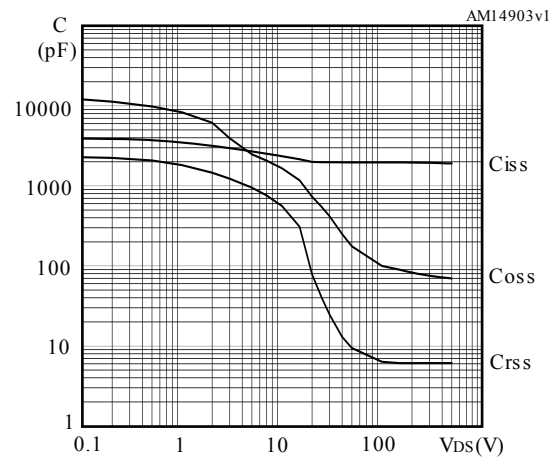
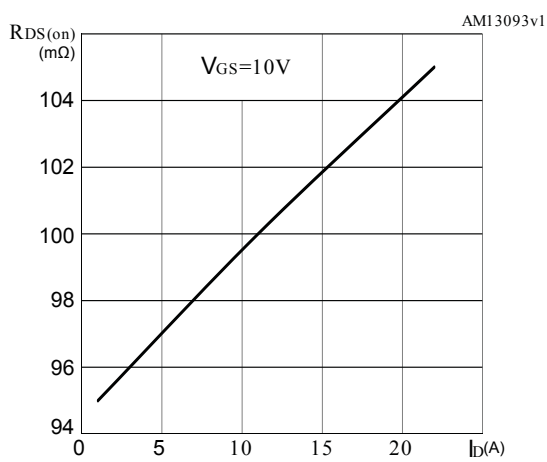
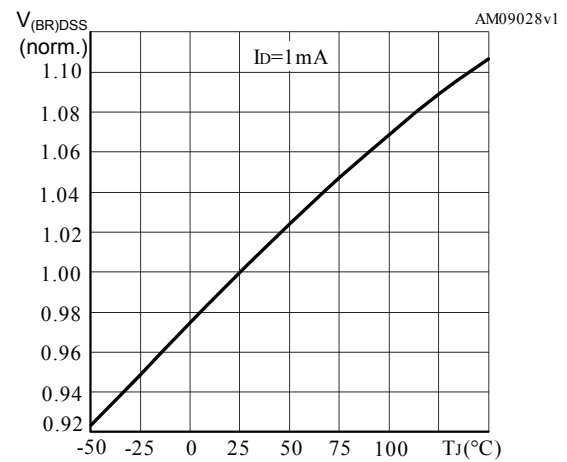
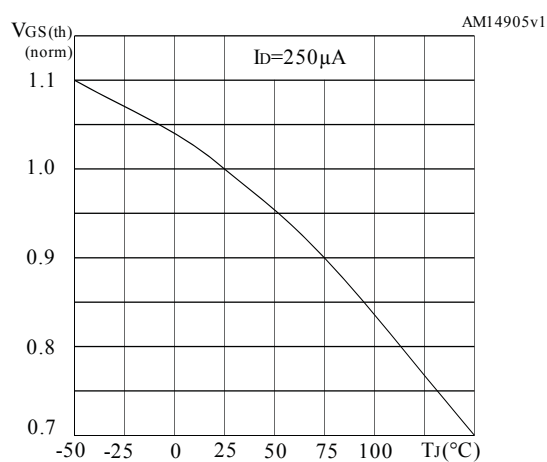
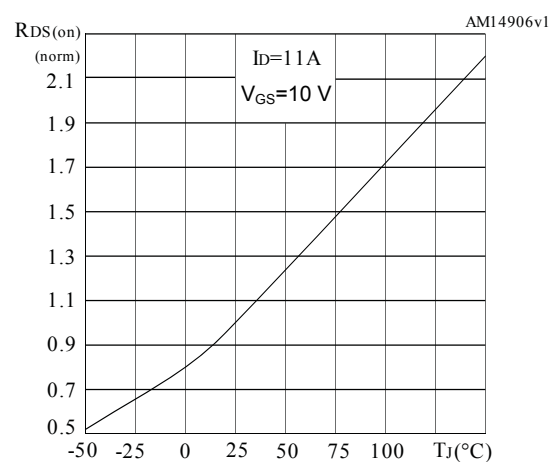
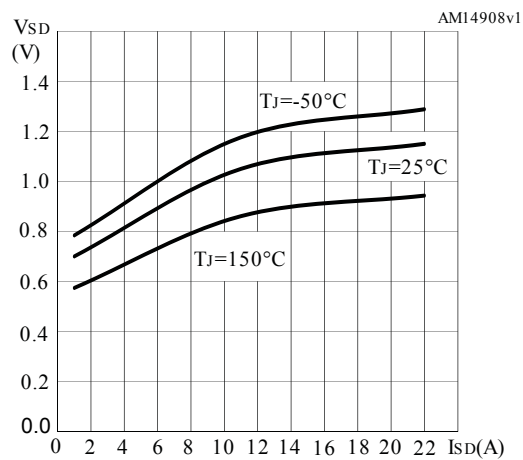
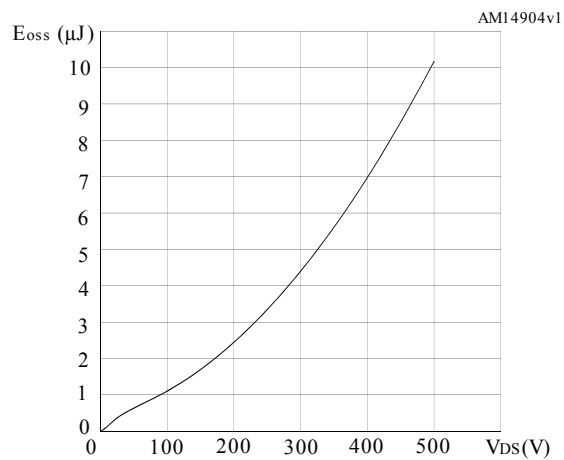
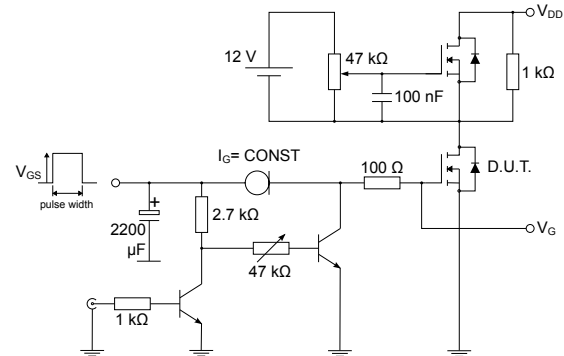
Figure 7. Typical gate charge characteristics

Figure 8. Typical capacitance characteristics

Figure 9. Typical drain-source on-resistance

Figure 10. Normalized breakdown voltage vs temperature

Figure 11. Normalized gate threshold vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Typical reverse diode forward characteristics

Figure 14. Output capacitance stored energy


3 Test circuits

Figure 15. Test circuit for resistive load switching times


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Figure 16. Test circuit for gate charge behavior


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Figure 17. Test circuit for inductive load switching and diode recovery times

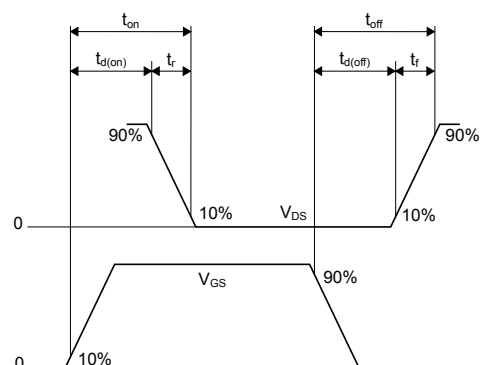

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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


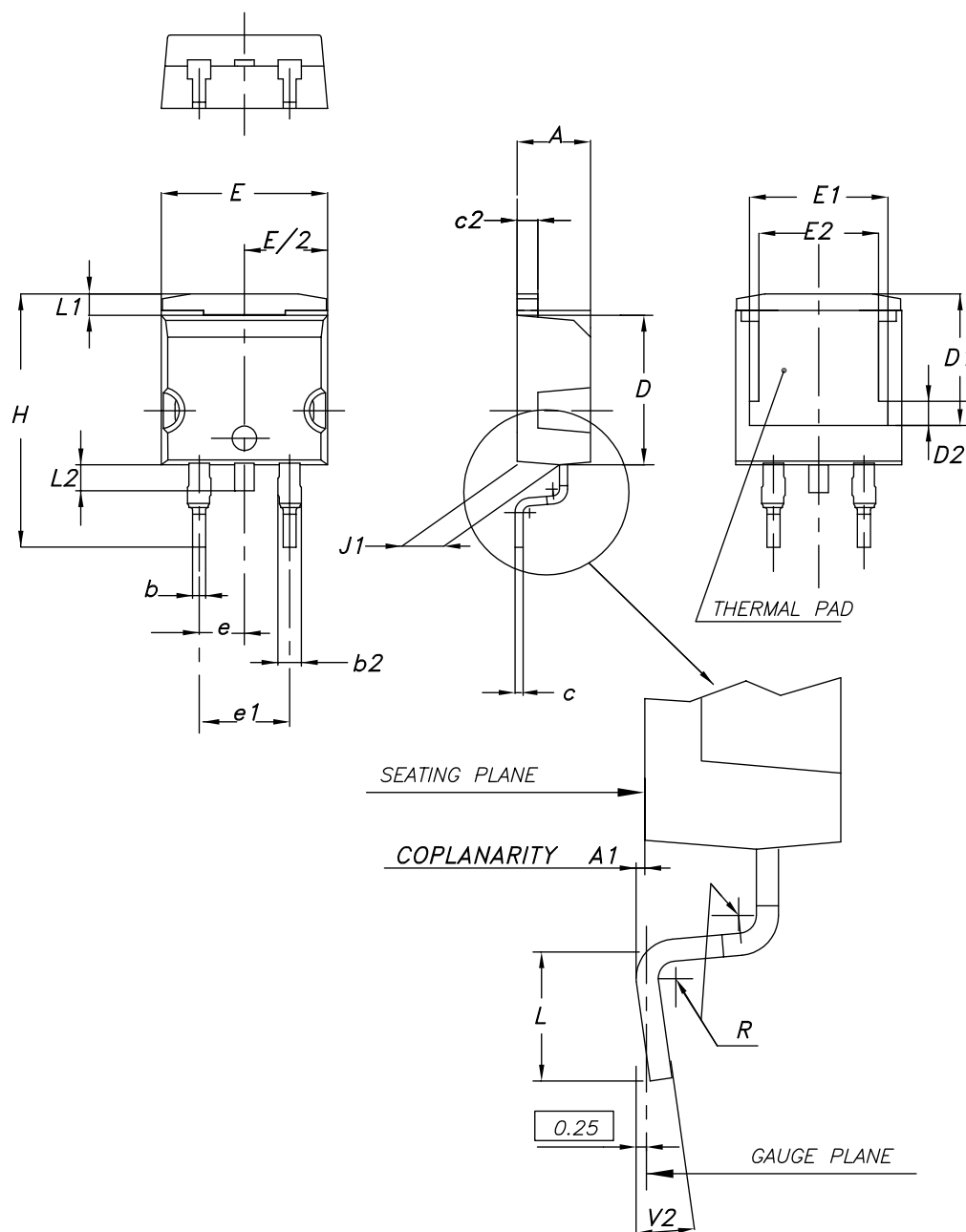
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 21. D²PAK (TO-263) type A2 package outline

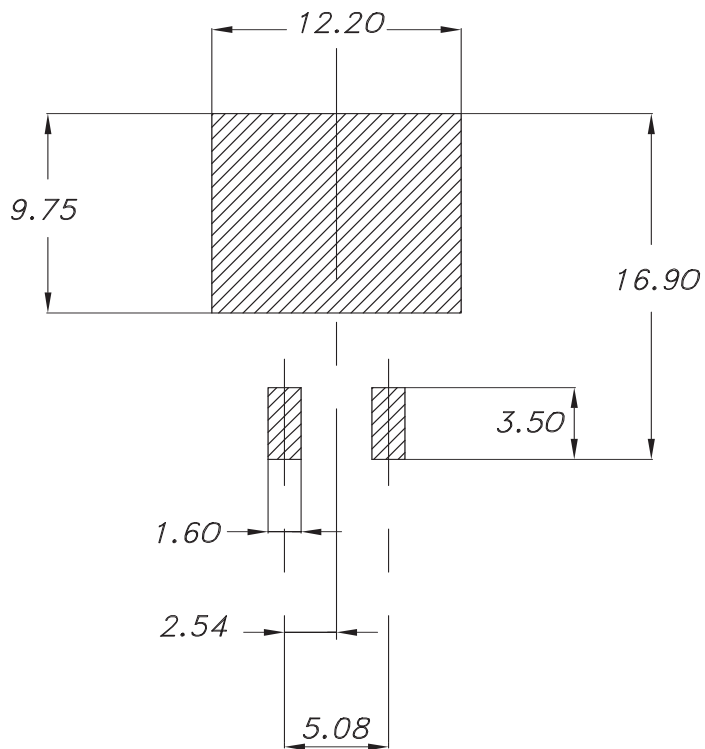


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Table 8. D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

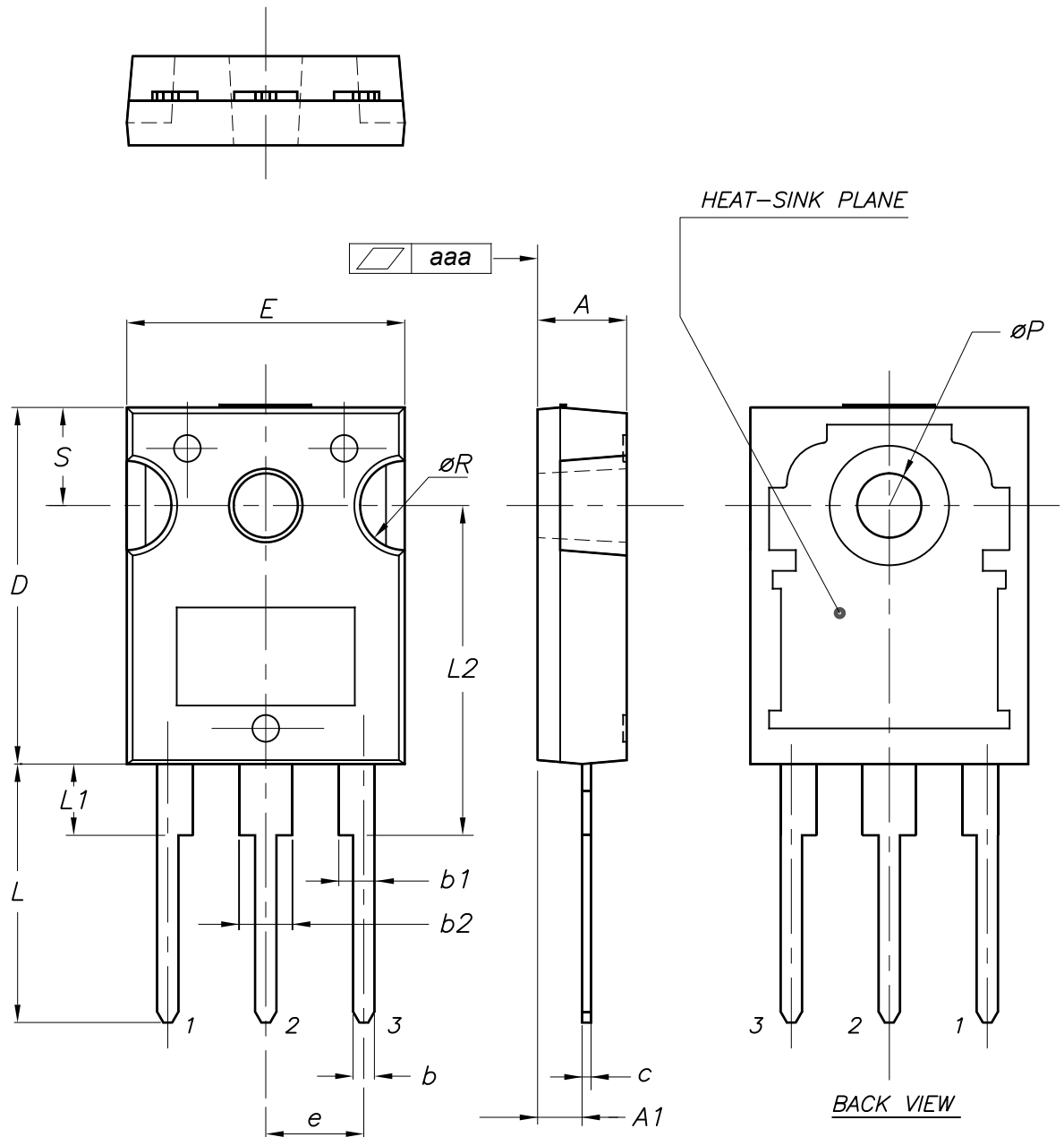
Figure 22. D²PAK (TO-263) recommended footprint (dimensions are in mm)



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4.2 TO-247 package information

Figure 23. TO-247 package outline



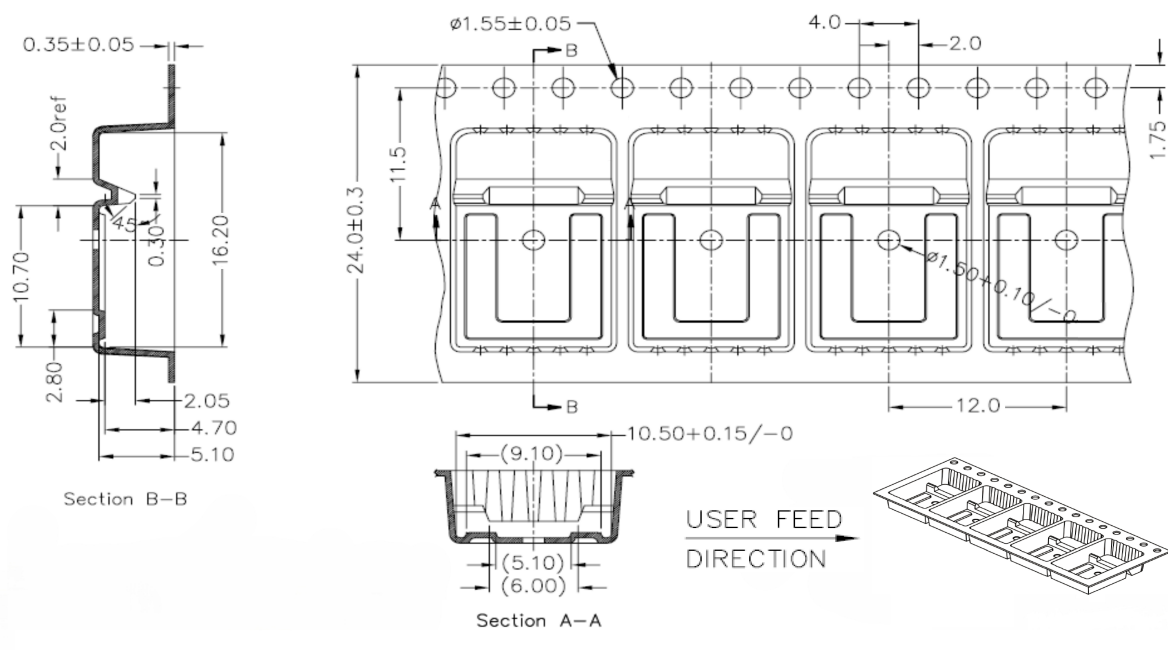
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Table 9. TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70
aaa		0.04	0.10

4.3 D²PAK packing information

Figure 24. D²PAK tape drawing (dimensions are in mm)



DM01095771 2

Revision history

Table 10. Document revision history

Date	Revision	Changes
01-Aug-2012	1	Initial release.
19-Sep-2025	2	The part numbers STF32NM50N and STP32NM50N have been removed and the document has been updated accordingly. Updated Section 4: Package information .

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