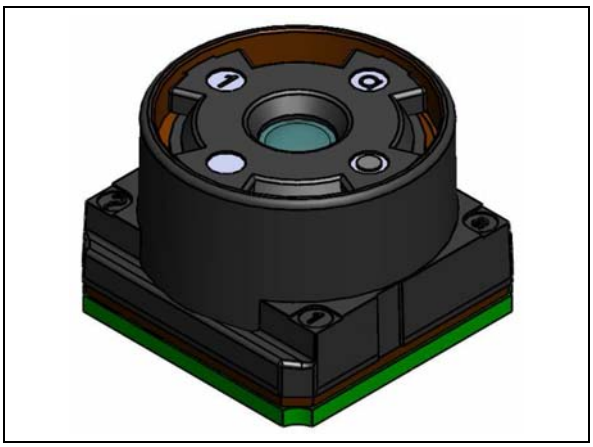
VX6854LC

QXGA EDOF camera module

Datasheet - production data



Features

- 3.15 megapixel resolution sensor (2048 x1536)
- Extended Depth of Field (EDOF)
- Compact size: 6.5 x 6.5 x 4.6mm
- SMIA Profile 2 compliant
- MIPI[a] CSI-2 (v0.9 D-PHY) and SMIA CCP2 video data interface
- CCI command interface 100 KHz up to 400 KHz
- 2.8V (analog) / 1.8V (digital) operation
- Integral EMC shielding
- Binning mode (2x2)
- Defect correction
- 4-channel lens shading correction

Description

The VX6854LC 3 megapixel camera module is designed to be used for high quality still camera function and also supports video modes. The camera silicon device is SMIA 1.0 profile 2 compliant and is capable of generating raw bayer 3 Mpixel images up to 20 fps. The VX6854LC supports the CCI control and CCP 2.0 and CSI-2 data interfaces.

The module design is optimized for both footprint and height. The module provides excellent image quality at focus distances from less than 50 cm to infinity.

VX6854LC offers an ultra low power consumption hardware standby mode consuming less than 50 µW (typical).

A separate hardware accelerator (STV0987) device can be incorporated in the phone system to run the associated image processing algorithms in hardware where the baseband cannot support this processing load.

Table 1. Device summary

Order code	Package	Packing
VX6854LCQ05I/1	SMIA65	Tape and reel

a. Copyright© MIPI alliance standard for camera serial interface 2v1.0 and MIPI alliance specification D-PHY v 0.9

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1 Overview

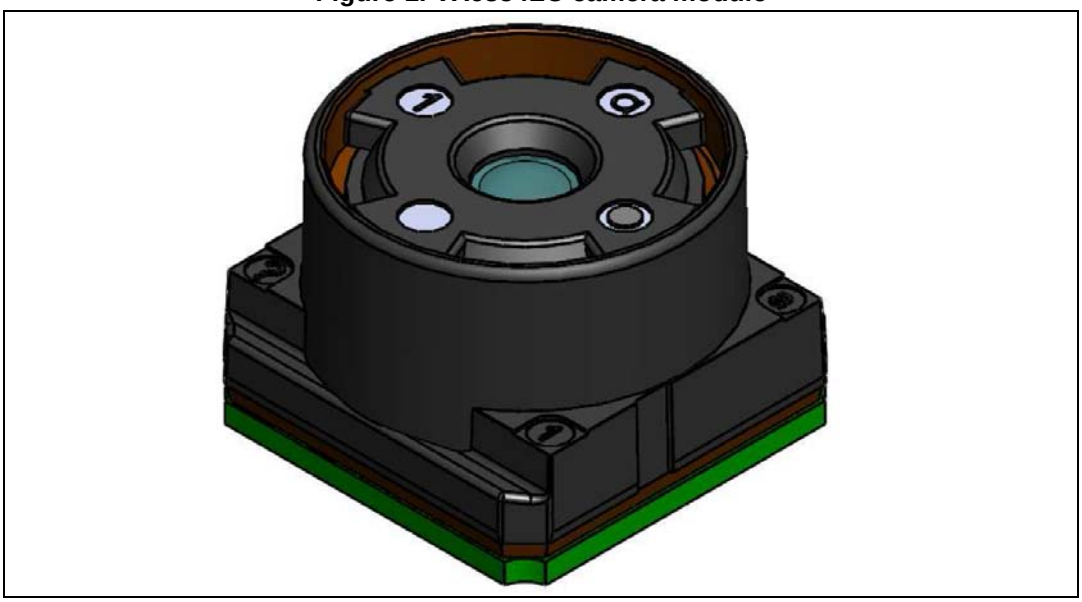
The VX6854LC image sensor produces raw 3.15 Mpixel digital video data at up to 20 frames per second.

The VX6854LC has both CCP2.0 and MIPI CSI-2 video data interfaces selectable over the Camera Control Interface (CCI). The VX6854LC is compliant with the SMIA 1.0[(b)] Specification Profile 2. The VX6854LC can also be used as Profile 0 or Profile 1 device. The sensor supports full horizontal and vertical scaling and output frequency derating as defined in the specification. The VX6854LC supports 2x2 binning modes which support frame rates of 40 fps and 80 fps respectively.

The image data is digitized using an internal 10-bit column ADC. The resulting pixel data is output as 8-bit, 10-bit or 10-8 bit compressed data and includes checksums and embedded codes for synchronization. The interface conforms to both the CCP 2.0 and MIPI CSI-2 interface standards. The sensor is fully configurable through a CCI serial interface.

The module is available in a SMOP type package measuring 6.5 mm x 6.5 mm x 4.6 mm. It is designed to be used with a board mounted SMIA65 socket.

Figure 1. VX6854LC camera module



b. Including up to ECR0002

Table 2. Technical specification

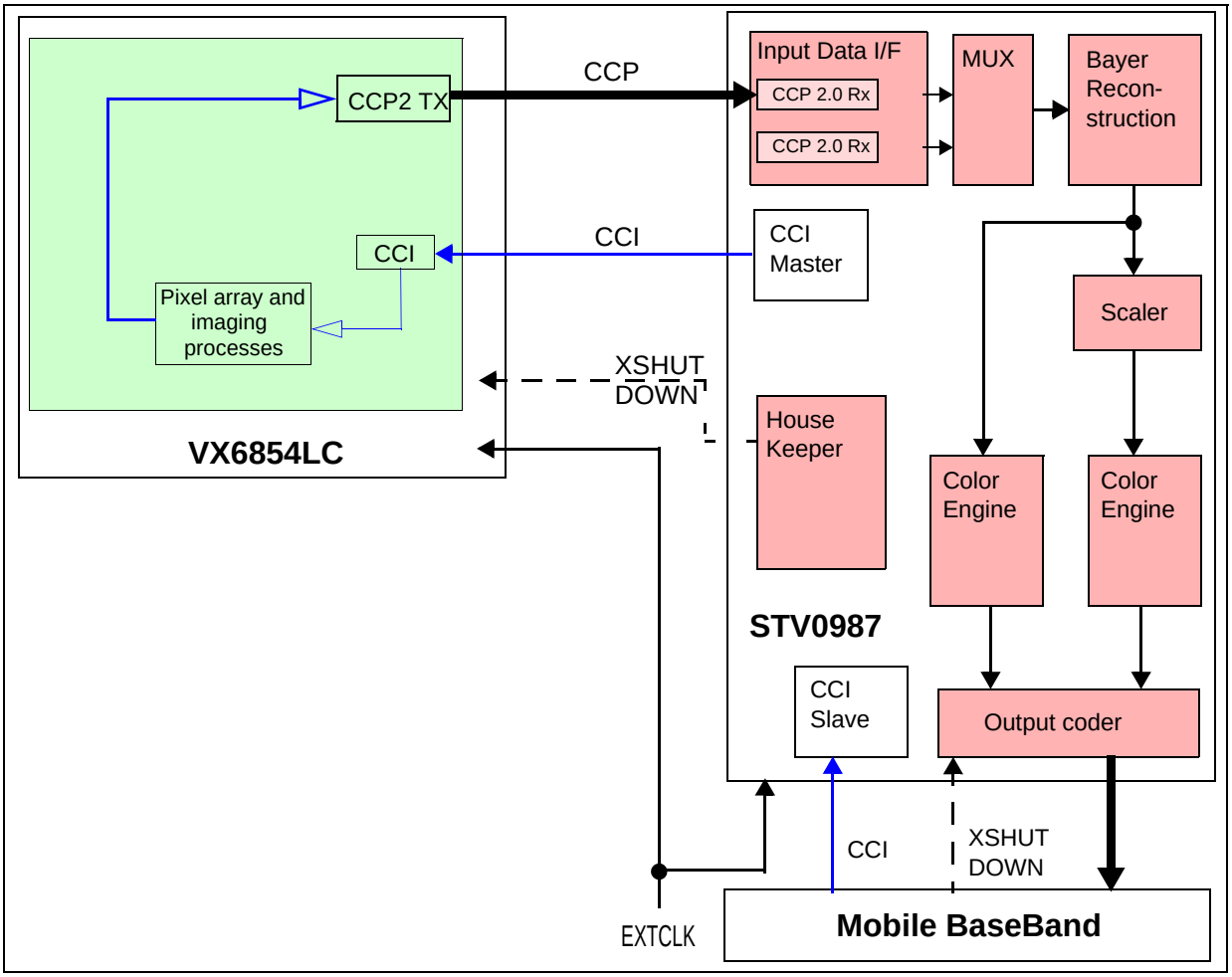
Feature	Detail
Pixel resolution	2048 x 1536 (QXGA)
Sensor technology	IMG140 ST's 65 nm based CMOS imaging process
Pixel size	1.75 µm x 1.75 µm
Exposure control	+ 81 dB
Analogue gain	+ 24 dB (max)
Digital gain	+ 6 dB (max)
Dynamic range	63 dB
Signal to noise	36 dB (@ 100 lux)
SNR10 value	60 Lux
Supply voltages	Analogue: 2.3V - 2.9V Digital: 1.7V - 1.9V
Average power consumption	<200 mW
Package size (L x W x H)	6.5 mm x 6.5 mm x 4.6 mm
Lens	58° +/-2° HFOV F/2.8
TV distortion	-0.3%
Relative illumination	75 % (typ.)
System attach	SMIA65 socket

1.1 VX6854LC use in system with hardware co-processor

The VX6854LC is an image sensor and it can be paired with the STMicroelectronics STV0987 companion processor. The coprocessor and the sensor together form a complete imaging system.

Figure 2 below illustrates a typical system using VX6854LC and STV0987.

Figure 2. VX6854LC in system with processor



The sensor main function is to convert the viewed scene into a data stream. The companion processor function is to manage the sensor so that it can produce the best possible pictures and to process the data stream into a form which is easily handled by up stream mobile baseband or MMP (multi-media processor) chipsets.

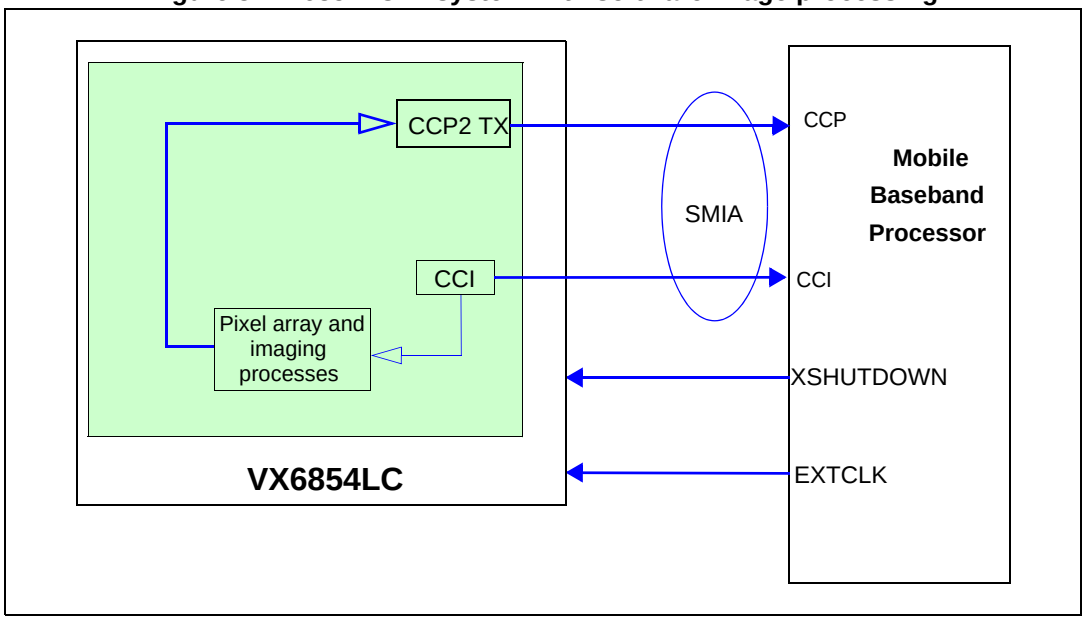
The sensor supplies high speed clock signal to the processor and provides the embedded control sequences which allow the co processor to synchronize with the frame and line level timings. The processor then performs the color processing on the raw image data from the sensor before supplying the final image data to the host.

With the coprocessor system the clock is sent by host to both the VX6854LC and the coprocessor. The high-speed clock for the coprocessor is supplied from the VX6854LC. It is generated using the VX6854LC PLL and is provided as the continuous data qualification clock.

1.2 VX6854LC use in system with software image processing

The VX6854LC image sensor can be directly connected to a baseband or multimedia processor. No dedicated coprocessor is used in this configuration. The image processing is done in software or hardware within the baseband processor.

Figure 3. VX6854LC in system with software image processing



Systems with a CCP 1.0 interface can operate with this device, however they may have a maximum CCP link speed of 208 MHz and therefore will not be able to achieve 20 fps with this device.

1.3 Reference documents

Table 3. Reference documents

Title	Date
MIPI Alliance Standard for Camera Serial Interface 2 (CSI-2) v1.0	Nov 2005
MIPI Alliance D-PHY Specification (v00-90-00)	Oct 2007
SMIA 1.0 Functional Specification	30/06/2004
SMIA 1.0 Characterization Specification Rev A	10/03/2005
SMIA 1.0 CCP2 Specification	30/06/2004
SMIA 1.0 Mechanical Specification	30/06/2004
SMIA 1.0 Functional Specification ECR0001 ver 1	11/02/2005
SMIA 1.0 CCP2 Specification ECR0002 ver 1	11/02/2005

2 Device pinout

Figure 4 shows the module pinout and *Table 4* contains the signal description.

Figure 4. VX6854LC module pinout (viewed from bottom of camera module)

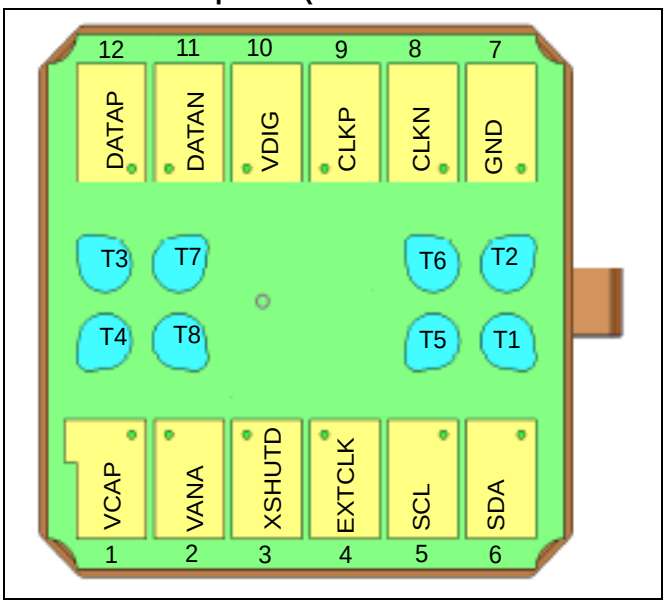


Table 4. Pin description

Pad number	Pad name	I/O type	Description
Power supplies			
1	VCAP	PWR	No connection required(1)
7	GND	PWR	Ground (combined)
2	VANA	PWR	Analog power
10	VDIG	PWR	Digital power
System			
3	XSHUTDOWN	I	Power down control(2)
4	EXTCLK	I	System clock input(3)
Control			
5	SCL	I	Serial communication clock
6	SDA	I/O	Serial communication data
Data			
8	CLK-	SubLVDS output	Output qualifying clock
9	CLK+	SubLVDS output	Output qualifying clock
11	DATA-	SubLVDS output	Serial output data
12	DATA+	SubLVDS output	Serial output data

Table 4. Pin description (continued)

Pad number	Pad name	I/O type	Description
ST test			
T1-T8		ST test pins	Do not connect(4)

1. VCAP is internal to the module. An additional 220nF capacitor may also be connected to this pin.
2. Signal is active low.
3. The EXTCLK pad has a Schmitt trigger input
4. Test pins are not floating.

2.1 ESD protection diodes

The ESD protection diodes can be used to check the connectivity. To test for connectivity, draw 100 uA from the pin and measure the voltage. If the voltage is less than 180 mV or greater than 900 mV the test fails.

Table 5. ESD protection diodes

S854 SMIA65				
Pin name	**Pin number**	**ESD protected**	**Diode to VDIG**	**Diode to GND**
VCAP	1	YES	NO	YES
VANA	2	YES	NO	YES
XSHUTD	3	YES	NO	YES
EXTCLK	4	YES	NO	YES
SCL	5	YES	NO	YES
SDA	6	YES	NO	YES
DGND	7	YES	YES	YES
CLKN	8	YES	Diode to local supply	Diode to GNDE
CLKP	9	YES	Diode to local supply	Diode to GNDE
VDIG	10	YES	NO	YES
DATAN	11	YES	Diode to local supply	YES
DATAP	12	YES	Diode to local supply	YES

3 Functional description

This chapter details the main blocks in the device in the following sections:

- *Section 3.1: Analog video block*
- *Section 3.2: Digital video block*
- *Section 3.4: Power management on page 19*

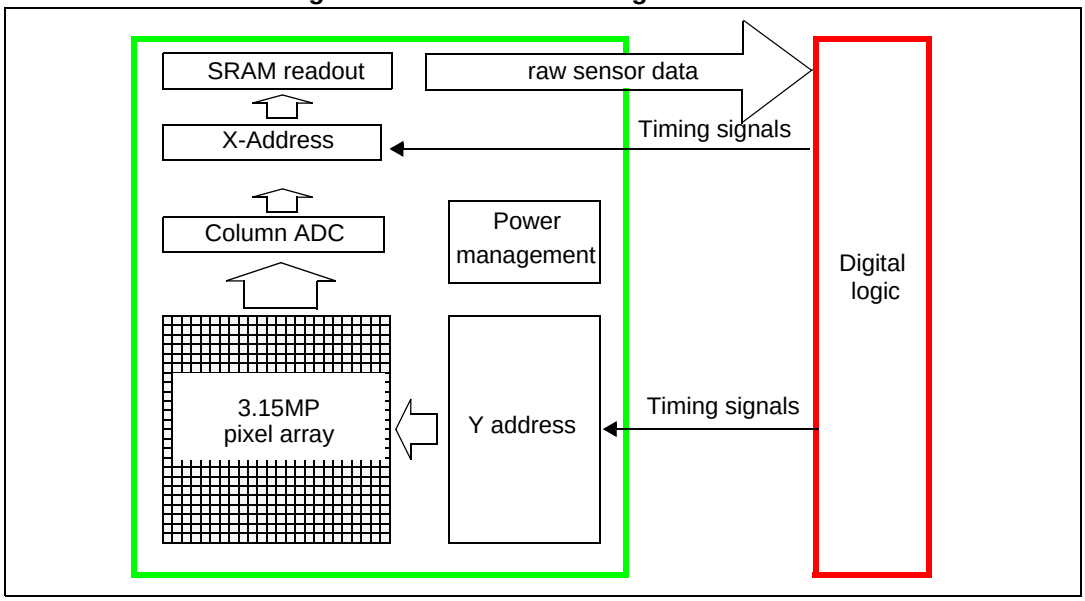
This chapter also describes:

- the device's operating modes, see *Section 3.3 on page 18*
- clock and frame rate control, see *Section 3.5 on page 26*
- control and video interface formats, see *Section 3.6 on page 28*

3.1 Analog video block

The analog video block, shown in *Figure 5*, consists of a 3.15 Mpixel resolution pixel array, power management circuitry. The digital block provides all timing signals to drive the analog block.

Figure 5. Overview of analog video block



Pixel voltage values are read out and digitized using the address decoders and column ADC.

3.2 Digital video block

3.2.1 Features

- Frame rate: 20 frame/s maximum can be reduced down to less than 3 frame/s (3.15 Mpixel) using frame extension
- Automatic dark calibration to ensure consistent video level over varying scenes
- On-chip power-on-reset cell
- Output format: 3.15 Mpixel 2064 x 1552 (maximum)

3.2.2 Dark calibration algorithm

VX6854LC runs a dark calibration algorithm on the raw image data to control the video offsets caused by dark current. This ensures that a high quality image is output over a range of operating conditions. First frame dark level is correctly calibrated, for subsequent frames the adjustment of the dark level is damped by a leaky integrator function to avoid possible frame to frame flicker.

3.3 Device operating modes

Figure 6 shows the various operating modes used by the system. The modes are exaplained in *Table 6*.

Figure 6. System state diagram

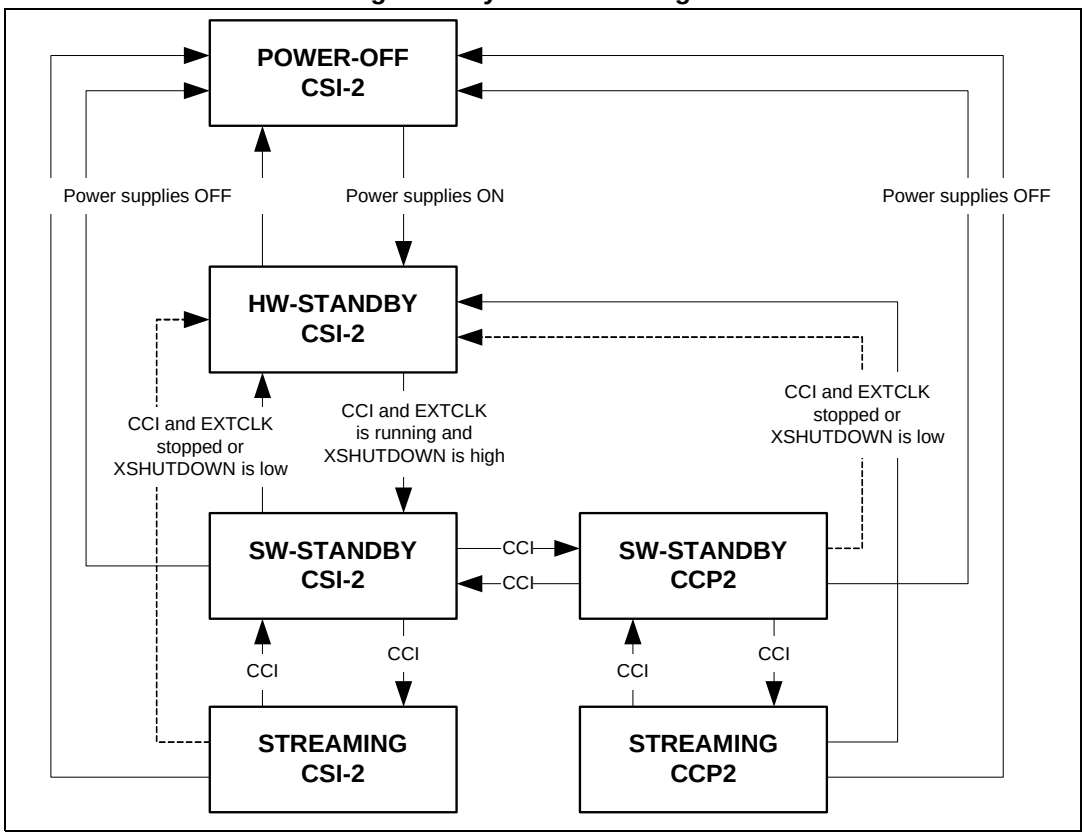


Table 6. Operating modes

Mode	Description
Power off	Power supplies are off.
Hardware standby	This is the lowest power consumption mode. CCI communications are not supported in this mode. The clock input pad, PLL and the video blocks are powered down. This state is entered by pulling the control pin XSHUTDOWN down. All registers are returned to their default values.
Software standby	This mode preserves the contents of the CCI register map. CCI communications are supported in this mode. The software standby mode is selected using a serial interface command. If this state is entered from hardware standby the data pads remain high impedance. If this state is entered from streaming then the data pads go high impedance at the end of the current frame. At this point the video block and PLL power down. The internal video timing is reset to the start of a video frame in preparation for the enabling of active video. The values of the serial interface registers like exposure and gain are preserved. The system clock must remain active when communicating with the sensor. This state is entered by releasing the device from hard reset by: setting XSHUTDOWN high, writing 0x00 to the mode control register (0x0100) or commanding a soft reset by writing 0x01 to the software reset register (0x0103). Note that after a soft reset or the transition of XSHUTDOWN to high, all registers are returned to their default values.
Streaming	The VX6854LC streams live video. This mode is entered by writing 0x01 to the mode control register (0x0100).

3.4 Power management

VX6854LC requires a dual power supply. The analog circuits are powered by a nominal 2.8 V supply while the digital logic and digital I/O are powered by a 1.8 V supply. Different sections of the sensor are powered depending on the system state. See *Table 7* for details.

Table 7. Power management matrix

Mode	Functional block powered down					Video data inhibit
	CCI	Digital	PLL and CLK pins (1)	Output pins	Analog	
Hardware standby	Yes	Yes	Yes	Yes	Yes	Yes
Software standby	No	Yes	Yes	Yes	Yes	Yes
Streaming	No	No	No	No	No	No

1. PLL, CLK+ and CLK- pins

3.4.1 Power-up procedure

The digital and analog supply voltages can be powered up in any order for example, VDIG then VANA or VANA then VDIG. See *Table 8* for timing constraints.

On power-up the on-chip power-on reset cell ensures that the CCI register values are initialized correctly to their default values.

The EXTCLK clock can either be initially low and then enabled during software standby mode or EXTCLK can be a free running clock.

Table 8. Power-up sequence timing constraints for CCP2/CSI2 communications

Symbol	Parameter	Min.	Max.	Units
t0	VANA rising – VDIG rising	VANA and VDIG may rise in any order The rising separation can vary from 0 ns to indefinite		ns
t1	VDIG rising – VANA rising			ms
t2	VANA/VDIG – XSHUTDOWN rising	XSHUTDOWN must rise coincident with, or later than, both power supplies (VDIG and VANA)		us
t3	XSHUTDOWN – first I^2C transaction with free running clock	5(1)	-	ms
t4	Minimum period with EXTCLK present prior to the first I^2C transaction. Gated clock.	5(2)	-	ms
t5	PLL start up/lock time	-	1	ms
t6	Entering streaming mode – first frame start sequence (fixed part)	-	10	ms
t7	Entering streaming mode – first frame start sequence (variable part) = Integration time	fine_integration_time_min	-	ms

1. 5 ms is necessary to upload the NVM data into firmware registers and get the FW ready for sensor initialization through I^2C writes.
2. For gated clock.

Figure 7. VX6854LC power-up sequence for CCP2 mode

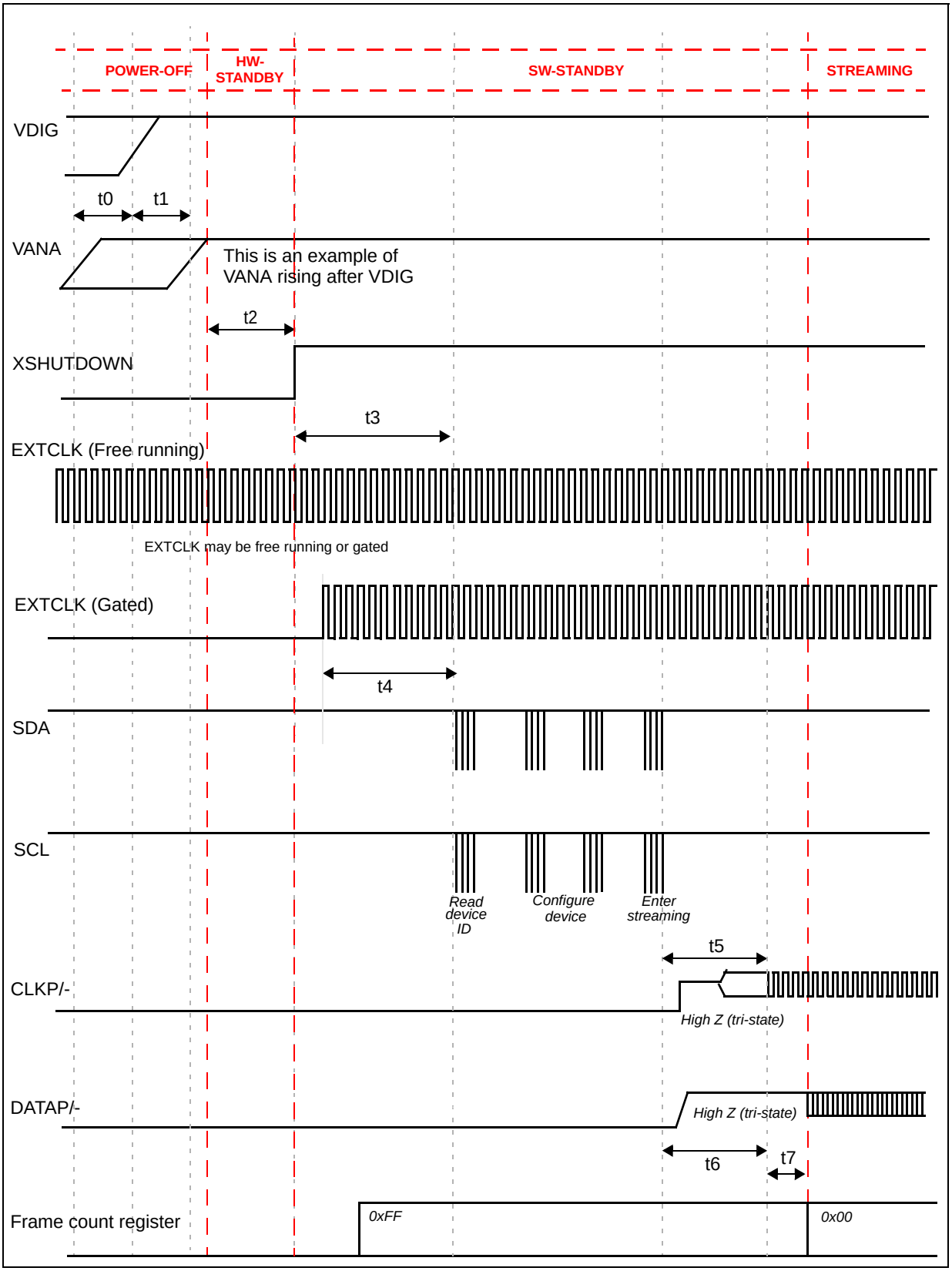
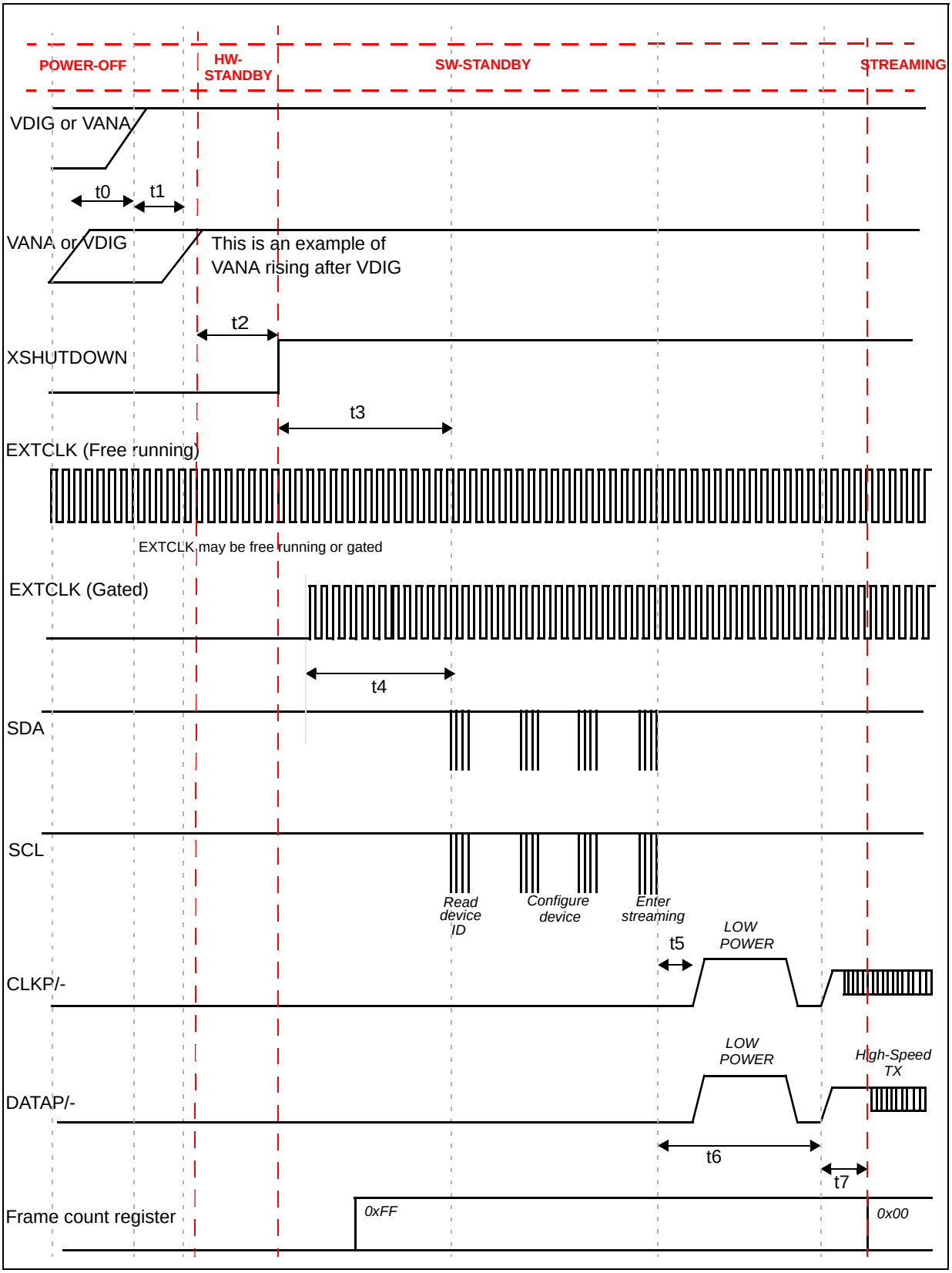


Figure 8. VX6854LC power-up sequence for CSI-2 mode



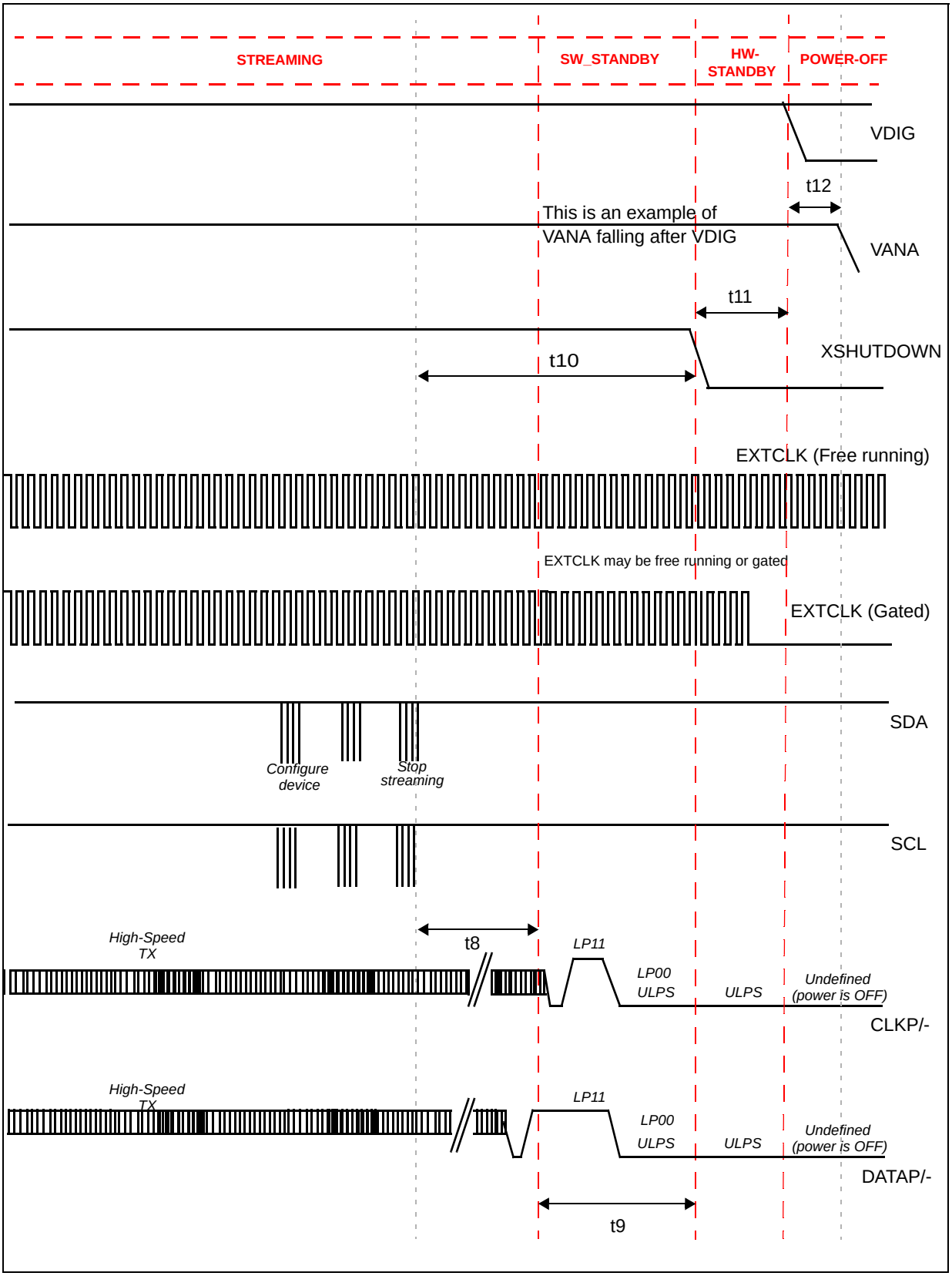
3.4.2 Power-down procedure

Table 9. Power-down sequence timing constraints for CSI2 communications

Symbol	Parameter	Min.	Max.	Units
t8	Last I^2C transaction to MIPI frame end(1)	-	1 frame	
t9	Minimum EXTCLK cycles required after last I^2C transaction or MIPI frame end(2)	512	-	clock cycles
t10	Last I^2C transaction or MIPI frame end to XSHUTDOWN failling(3)	t8+t9	-	
t11	XSHUTDOWN to VANA/VDIG falling	XSHUTDOWN must fall at the same time as, or earlier than, both power supplies (VDIG and VANA)		
t12	VANA to VDIG or VDIG to VANA falling	VANA and VDIG may fall in any order, the rising separation can vary from 0 ns to indefinite		

1. The whole power down sequence is triggered by the CCI power down request, however the power down sequence will only start after the end of the frame when all active data are consumed on CSI-2 DN/DP pins. When this is done, the CSI-2 DN/DP signals enter LP11. The CSI-2 clock will enter LP11 with a delay of 5us (corresponding to Tclk_post + Tclk_trail) compared to DN/DP pins. The device is then SW_STANDBY and will enter LP00 and stay in Ultra Low power mode.
2. After the last frame completion, the gated clock needs to be kept for 512 cycles at least so the system can enter Ultra Low power state. After the system enters ULPS mode, you can keep or stop the EXTCLK.
3. Note: XSHUTDOWN can be asserted at any time. This immediately removes the core-supply, causing the POR to trigger and reset all the digital logic and macros - it does not depend on the presence of the clock. When XSHUTDOWN is asserted, the clock can be running or not - it does not matter.

Figure 9. VX6854LC power-down sequence for CSI-2 mode



3.4.3 Internal power-on reset (POR)

The VX6854LC internally performs a power-on reset (POR) when the 1V2 Vcore digital supply rises through the trigger level, Vtrig_rising. Similarly, if the 1V2 Vcore digital power supply falls through the trigger level, Vtrig_falling, then the power-on reset will also trigger.

Definitions:

Rise threshold voltage (VTRIGR)	This is the supply voltage level that is recognised by the POR as voltage “HIGH”. Only after the supply reaches this level does the output of POR change to high level if it is off, after a specified amount of delay.
Fall threshold voltage (VTRIGF)	This is the supply voltage level that is recognised by the POR as voltage “LOW”. Only after the supply reaches this level does the output of POR change to low (ground) level if it is on.
Burst width (pw)	Burst is the negative pulse riding the supply signal. The burst width is measured as the amount of duration for which the supply signal dropped beyond the threshold levels.
Delay duration (TPOR)	Delay duration is defined as the time duration for which POR stays off before re-powering. Each reset of POR will impart a specified delay duration before POR re-powers.

Figure 10. POR timing

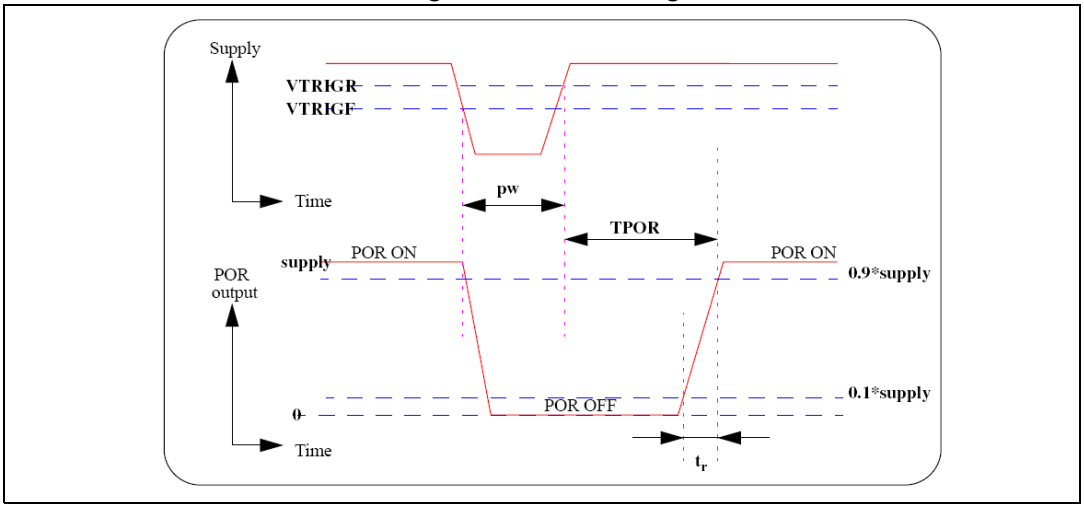


Table 10. POR cell characteristics

Symbol	Constraint	Min	Typ.	Max	Units
VTRIGR	POR Rise Voltage detection	-	-	0.95	V
VTRIGF	POR Fall Voltage detection	0.4	-	-	V
Tburst (pw)	Burst Filter	-	2	8	µs
Tpor	Delay Duration	-	20	45	µs

3.4.4 Failsafe signals

All signals going into the VX6854LC must be either at a low state or high impedance when power is removed from the device. The exceptions to this rule are the EXTCLK, XSHUTDOWN and the CCI signals. These pads have been designed to be high impedance when the VX6854LC is powered-down. This means that the input signal on the specified pads can either be high or low with no leakage problems.

3.5 Clock and frame rate timing

3.5.1 Video frame rate control

The output frame rate of VX6854LC can be reduced by extending either the line length or the frame length. The extension is achieved by adding extra blanking bytes at the end of a line or “blank” video lines to act as timing padding. The frame rate can be reduced from the default 20 frame/s at 3.15 Mpixel resolution to less than 3 frame/s at 3.15 Mpixel resolution.

The advantage of the frame extension approach is that it does not reduce the pixel readout rate or the active frame time and therefore does not introduce unwanted motion distribution effects to the image.

3.5.2 PLL and clock input

The VX6854LC has an embedded PLL block. This block generates all necessary internal clocks from an input range defined in *Table 11*. The input clock pad accepts sine wave or square wave.

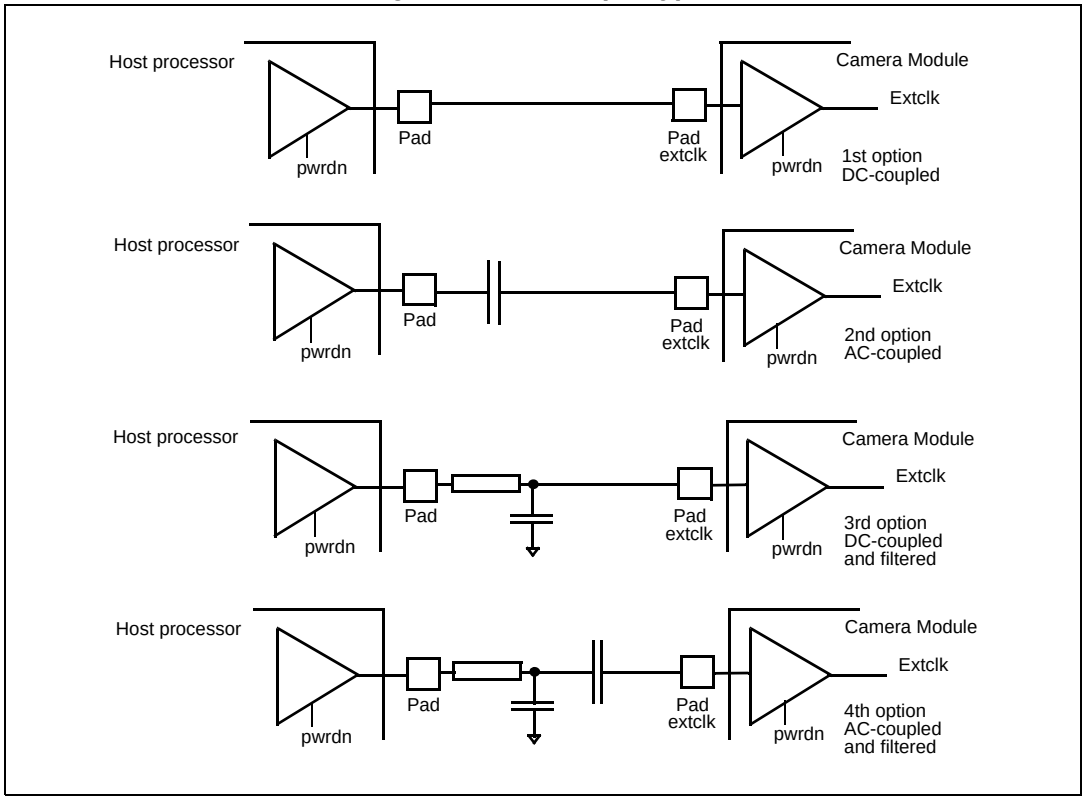
Table 11. System input clock frequency range

Minimum (MHz)	Maximum (MHz)
6	27

3.5.3 Clock input type

As required by the SMIA specification the VX6854LC can receive the clock types shown in *Figure 11*. Note that the EXTCLK pad has a schmitt trigger input.

Figure 11. Clock input types



The clock is fail-safe/high impedance when in either AC or DC coupled and in any mode including the power off state.

3.6 Control and video interface formats

Image data is transferred from the VX6854LC using a high speed subLVDS serial link.The serial control data is transferred to and from the VX6854LC using a CCI bus.

3.6.1 CCP/CSI-2 serial data link

Data signals (DATA+ and DATA-) and clock signals (CLK+ and CLK-) are transferred from VX6854LC using two pairs of balanced 100 Ω impedance transmission lines.

The transmission line pairs and custom transmitters/receivers realize a very low voltage differential (subLVDS) signalling scheme that can transfer information in a potentially noisy environment.

As implemented in VX6854LC, the CCP link supports the transmission of raw bayer data at 3.15 Mpixel resolution up to 20 frame/s at 8-bit or 10-8 bit compressed resolution or 15 frame/s at 10-bit resolution.

As implemented in VX6854LC, the CSI-2 link supports the transmission of raw bayer data at 3.15 Mpixel resolution up to 20 frame/s at 10-bit resolution.

3.6.2 CCI serial control bus

The internal registers in VX6854LC can be configured by a master device using a CCI bus (SDA, SCL). VX6854LC sends and receives commands over this bus at up to 400 Kbit/s.

The CCI bus uses a device address of 0x20 for writes and 0x21 for reads.

4 Register map

4.1 Status registers [0x0000 to 0x000F]

Table 12. Status registers [0x0000 to 0x000F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0000	Hi	model_id	16UI	03.56	RO	Camera model identifcation 0x0356 = 854_{10} (This value is derived from the NVM)
0x0001	Lo					
0x0002		revision_number_major	8UI	02	RO	Revision identifier of the camera for DCC change 00: Unprogrammed 01: ES1.0 02: ES2.0 (This value is derived from the NVM)
0x0003		manufacturer_id	8C	01	RO	Module manufacturer ID: ST (This value is derived from the NVM)
0x0004		smia_version	8C	0A	RO	0x0A: SMIA 1.0
0x0005		frame_count	8UI	FF	RO	Frame count increments by 1 on each frame. Rolls over at 255 to 0. When moving from video to sleep the frame count will be reset to 255. The frame count will also be reset to 255 after a soft reset (register 0x0103).
0x0006		pixel_order	8C	00	RO	Color pixel readout order. Defines the order of the colour pixel readout. Changes with mirror and flip (register 0x0101). 0x00 - GR/BG - normal 0x01 - RG/GB - horizontal mirror 0x02 - BG/GR - vertical flip 0x03 - GB/RG - vertical flip and horizontal mirror
0x0008	Hi	data_pedestal	16UI	00.40	RO	The video data is offset by 64.
0x0009	Lo					
0x000C		pixel_depth	8UI	0A	RO	Pixel data resolution.
0x0010		revision_number_minor	8UI	00	RO	Revision identifier of the camera for minor changes (This value is derived from the NVM)
0x0011		additional_spec_ver	8UI	06	RO	Additional specification identifier
0x0012		module_date_year	8UI	00	RO	Manufacturing year (This value is derived from the NVM)
0x0013		module_date_month	8UI	00	RO	Manufacturing month (This value is derived from the NVM)

Table 12. Status registers [0x0000 to 0x000F] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0014		module_date_day	8UI	00	RO	Manufacturing day (This value is derived from the NVM)
0x0015		module_date_phase	8UI	01	RO	Manufacturing phase identification 00: TS 01: ES 02: CS 03: MP (This value is derived from the NVM)
0x0016	Hi	sensor_model_id	16UI	03.56	RO	Silicon identification 0x0356 = 854_{10}
0x0017	Lo					
0x0018		sensor_revision_number	8UI	30	RO	Bits 3:0 NVM version Bits 7:4 Silicon mask revsion 00: Cut1.0 10: Cut1.1 20: Cut2.0 30: Cut2.1 40: Cut2.2 (The value for bits[3:0] is derived from the NVM)
0x0019		sensor_manufacturer_id	8C	01	RO	Silicon manufacturer ID:ST
0x001A		sensor_firmware_ver	8C	30	RO	Silicon firmware version
0x001C	Hi	serial_number	32UI	00.00 00.00	RO	Serial number (This value is derived from the NVM)
0x001D						
0x001E						
0x001F	Lo					

4.2 Frame format description registers [0x0040 to 0x007F]

For a full description of the frame format description refer to *Chapter 5: Video data interface on page 52*.

Table 13. Frame format description registers [0x0040 to 0x007F]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0040		frame_format_model_type	8C	01	RO	Generic frame format. 0x01: 2-byte data format. (1)
0x0041		frame_format_model_subtype	8C	12	RO	Contains the number of 2-byte data format descriptors used. Upper nibble defines the number of column descriptors i.e 1. The lower nibble defines the number of row descriptors i.e. 2
0x0042	Hi	frame_format_descriptor_0	16C	58.10	RO	Pixel data code: 5 (visible columns) number of pixels : readout dependent (Maximum of 2064)
0x0043	Lo					
0x0044	Hi	frame_format_descriptor_1	16C	10.02	RO	Pixel data code: 1 (embedded data lines) Number of lines: 2
0x0045	Lo					
0x0046	Hi	frame_format_descriptor_2	16C	56.10	RO	Pixel data code: 5(visible lines) Number of lines: readout dependent(Maximum of 1552)
0x0047	Lo					

1. See section 4.5 of SMIA 1.0 functional specification.

4.3 Analogue gain description registers [0x0080 to 0x0097]

These registers are not dynamic but are required to be output on the status line so that it is possible to interpret the meaning of the analogue gain code(s). For a full description of the analogue gain description registers refer to *Section 6.5.1: Analogue gain model on page 67*.

Table 14. Analogue gain description [0x0080 to 0x0097]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0080	Hi	analogue_gain_capability	16B	00.00	RO	Analogue gain capability 0 – single global analogue gain only
0x0081	Lo					
0x0084	Hi	analogue_gain_code_min	16UI	00.00	RO	Minimum recommended analogue gain code that is, 0 (x1 gain)
0x0085	Lo					
0x0086	Hi	analogue_gain_code_max	16UI	00.F0	RO	Maximum recommended analogue gain code that is, 240 (x16 gain)
0x0087	Lo					
0x0088	Hi	analogue_gain_code_step	16UI	00.10	RO	Analogue gain code step size(1)
0x0089	Lo					

Table 14. Analogue gain description [0x0080 to 0x0097] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x008A	Hi	analogue_gain_type	16UI	00.00	RO	Analogue gain type
0x008B	Lo					
0x008C	Hi	analogue_gain_m0	16SI	00.00	RO	Analogue gain m0 constant. m0 = 0
0x008D	Lo					
0x008E	Hi	analogue_gain_c0	16SI	01.00	RO	Analogue gain c0 constant. c0 = 256
0x008F	Lo					
0x0090	Hi	analogue_gain_m1	16SI	FF.FF	RO	Analogue gain m1 constant. m1 =-1
0x0091	Lo					
0x0092	Hi	analogue_gain_c1	16SI	01.00	RO	Analogue gain c1 constant c1 = 256
0x0093	Lo					

1. For above gains of 0xE0, the step size is four. See *Figure 26 on page 68* for gain values. This additional feature of the VX6854LC is outside of the SMIA specification.

4.4 Data format description registers [0x00C0 to 0x00FF]

The data format description registers specify which CCP data formats the SMIA camera module supports. Specifically VX6854LC supports CCP RAW 8, 10-8 compressed and RAW10.

Table 15. Data format description registers [0x00C0 to 0x00FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x00C0		data_format_model_type	8UI	01	RO	2-byte generic data format model. Always 0x01
0x00C1		data_format_model_subtype	8UI	03	RO	Number of descriptors i.e. 3
0x00C2	Hi	data_format_descriptor_0	16UI	08.08	RO	Top 8-bits of internal pixel data transmitted as RAW 8.
0x00C3	Lo					
0x00C4	Hi	data_format_descriptor_1	16UI	0A.0A	RO	Top 10-bits of internal pixel data transmitted as RAW 10.
0x00C5	Lo					
0x00C6	Hi	data_format_descriptor_2	16UI	0A.08	RO	Compress top 10-bits of internal pixel data to 8. Transmitted as RAW 8 mode.
0x00C7	Lo					

4.5 Setup registers [0x0100 to 0x01FF]

Table 16. Setup registers [0x0100 to 0x01FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0100		mode_select	8UI	00	RW	Mode select 0x00 - Software standby 0x01 - Streaming Refer to *Section 3.3: Device operating modes on page 18*
0x0101		image_orientation	8B	00	RW	Image orientation i.e. horizontal mirror and vertical flip. Bit 0: 0 - no mirror, 1 - horizontal mirror enable Bit 1: 0 - no flip, 1 - vertical flip enable
0x0103		software_reset	8UI	00	RW	Software reset. Setting this register to 1 resets the sensor to its power up defaults. The value of this bit is also reset 0x00 - normal 0x01 - soft reset Refer to *Section 3.3: Device operating modes on page 18* A 2.2ms delay is required after issuing the software reset command (6MHz clock)
0x0104		grouped_parameter_hold	8UI	00	RW	The grouped parameter hold register disables the consumption of integration, gain and video timing parameters 0x00 - consume parameters as normal 0x01 - hold parameters Refer to *Section 6.5.3: Integration and gain parameter re-timing on page 69*
0x0105		mask_corrupted_frames	8UI	00	RW	Setting this register to 1 prevents the sensor out-putting frames that have been corrupted by video timing parameter changes. 0x00 - normal 0x01 - mask corrupted frames
0x0110		csi_channel_identifier	8UI	00	RW	The DMA (CCP2) or Virtual (CSI2) channel identifier.
0x0111		csi_signalling_mode	8UI	02	RW	0x00 - CCP2 Data/clock signalling 0x01 - CCP2 Data/strobe signalling 0x02 - CSI-2 This register should not be changed while the device is streaming data.

Table 16. Setup registers [0x0100 to 0x01FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0112	Hi	csi_data_format	16UI	0A.0A	RW	The MSB contains the bit width of the uncompressed pixel data. The LSB contains the bit width of the compressed pixel data. 0A.0A - RAW10 mode 0A.08 - 10-8 compressed mode 08.08 - RAW8 mode
0x0113	Lo					
0x0114		csi_lane_mode	8UI	00	RW	Number of data lanes in use 00 - 1-lane
0x0120		gain_mode	8UI	00	RO	0x00 – Global analogue gain. VX6854LC supports only global gain modes.
0x0136	Hi	ext_clock_freq	8.8UR	06.00	RW	Frequency of external crystal
0x0137	Lo					

4.6 Integration time and gain registers [0x0200 to 0x02FF]

These registers are used to control the image exposure. See *Section 6.5: Exposure and gain control on page 67* for more information.

Table 17. Integration time and gain registers [0x0200 to 0x02FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0200	Hi	fine_integration_time	16UI	01.E5	RW	Fine integration time (pixels).
0x0201	Lo					
0x0202	Hi	coarse_integration_time	16UI	00.00	RW	coarse integration time (lines).
0x0203	Lo					
0x0204	Hi	analogue_gain_code_global	16UI	00.00	RW	Global analogue gain parameter (coded). See *Section 6.5.1: Analogue gain model on page 67* for details of how to use this parameter.
0x0205	Lo					
0x020E	Hi	digital_gain_greenr	16UR	01.00	RW	Gain code for greenr channel
0x020F	Lo					
0x0210	Hi	digital_gain_red	16UR	01.00	RW	Gain code for red channel
0x0211	Lo					
0x0212	Hi	digital_gain_blue	16UR	01.00	RW	Gain code for blue channel
0x0213	Lo					
0x0214	Hi	digital_gain_greenb	16UR	01.00	RW	Gain code for greenb channel
0x0215	Lo					

4.7 Video timing registers [0x0300 to 0x03FF]

For a full description of the video timing registers refer to *Chapter 6: Video timing on page 55*.

Table 18. Video timing registers [0x0300 to 0x03FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0300	Hi	vt_pix_clk_div	16UI	00.0A	RW	Number of system clocks per pixel clock.
0x0301	Lo					
0x0302	Hi	vt_sys_clk_div	16UI	00.01	RW	System clock divider value
0x0303	Lo					
0x0304	Hi	pre_pll_clk_div	16UI	00.01	RW	Pre PLL clock divider value
0x0305	Lo					
0x0306	Hi	pll_multiplier	16UI	00.85	RW	PLL multiplier value Value:133
0x0307	Lo					
0x0308	Hi	op_pix_clk_div	16UI	00.0A	RW	Number of output system clocks per pixel clock.
0x0309	Lo					
0x030A	Hi	op_sys_clk_div	16UI	00.01	RW	Output system clock divider value
0x030B	Lo					
0x0340	Hi	frame_length_lines	16UI	06.40	RW	Frame length Value:1600 Units: Lines
0x0341	Lo					
0x0342	Hi	line_length_pck	16UI	09.C4	RW	Line length Value:2500 Units: Pixel Clocks
0x0343	Lo					
0x0344	Hi	x_addr_start	16UI	00.00	RW	X-address of the top left corner of the visible pixel data Units: Pixels
0x0345	Lo					
0x0346	Hi	y_addr_start	16UI	00.00	RW	Y-address of the top left corner of the visible pixel data(1) Units: Lines
0x0347	Lo					
0x0348	Hi	x_addr_end	16UI	08.0F	RW	X-address of the bottom right corner of the visible pixel data Units: Pixels
0x0349	Lo					
0x034A	Hi	y_addr_end	16UI	06.0F	RW	Y-address of the bottom right corner of the visible pixel data Units: Lines
0x034B	Lo					
0x034C	Hi	x_output_size	16UI	08.10	RW	Width of image data output from the sensor module Units: Pixels
0x034D	Lo					

Table 18. Video timing registers [0x0300 to 0x03FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x034E	Hi	y_output_size	16UI	06.10	RW	Height of image data output from the sensor module Units: Lines
0x034F	Lo					
0x0380	Hi	x_even_inc	16UI	00.01	RW	Increment for even pixels. x_even_inc must = 1 for focus_estimation to operate effectively. Units: Pixels
0x0381	Lo					
0x0382	Hi	x_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0383	Lo					
0x0384	Hi	y_even_inc	16UI	00.01	RW	Increment for even pixels. y_even_inc must = 1 for focus_estimation to operate effectively. VX6854LC only suppports y-even-inc values of 1 and 5 Units: Pixels
0x0385	Lo					
0x0386	Hi	y_odd_inc	16UI	00.01	RW	Increment for odd pixels Units: Pixels
0x0387	Lo					

1. Has to be modulo 4 for correct operation of device

4.8 Image scaling registers [0x0400 to 0x04FF]

Table 19. Image scaling registers [0x0400 to 0x04FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0400	Hi	scaling_mode	16UI	00.00	RW	0 – No scaling 1 – Horizontal scaling. 2 - Full scaling (horizontal and vertical).
0x0401	Lo					
0x0402	Hi	spatial_sampling	16UI	00.00	RW	0 – Bayer sampling 1 – Co-sited sampling
0x0403	Lo					
0x0404	Hi	scale_m	16UI	00.10	RW	Down scale factor M component. (denominator)
0x0405	Lo					
0x0406	Hi	scale_n	16UI	00.10	RO	Down scale factor N component. (numerator, always 16)
0x0407	Lo					

4.9 Image compression registers [0x0500 to 0x05FF]

Table 20. Image compression registers [0x0500 to 0x05FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0500	Hi	compression_mode	16UI	00.01	RO	1 – DPCM/PCM compression (simple predictor)
0x0501	Lo					

4.10 Test pattern registers [0x0600 to 0x06FF]

Table 21. Test pattern registers [0x0600 to 0x06FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0600	Hi	test_pattern_mode	16C	00.00	RW	0 – Normal operation (default) 1 – solid colour bars(1) 2 – 100% colour bars(1) 3 – fade to grey' color bars(1) 4 – PN9(2) 5 to 255 - reserved
0x0601	Lo					
0x0602	Hi	test_data_red	16UI	00.00	RW	The test data used to replace red pixel data. Range 0 to 1023.(3)
0x0603	Lo					
0x0604	Hi	test_data_greenR	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have red pixels. Valid range 0 to 1023.(1)
0x0605	Lo					
0x0606	Hi	test_data_blue	16UI	00.00	RW	The test data used to replace blue pixel data. Range 0 to 1023(1)
0x0607	Lo					
0x0608	Hi	test_data_greenB	16UI	00.00	RW	The test data used to replace green pixel data on rows that also have blue pixels. Range 0 to 1023(1).
0x0609	Lo					
0x060A	Hi	horizontal_cursor_width	16UI	00.00	RW	Defines the width of the horizontal cursor (in pixels).
0x060B	Lo					
0x060C	Hi	horizontal_cursor_position	16UI	00.00	RW	Defines the top edge of the horizontal cursor.
0x060D	Lo					
0x060E	Hi	vertical_cursor_width	16UI	00.00	RW	Defines the width of the vertical cursor (in pixels).
0x060F	Lo					
0x0610	Hi	vertical_cursor_position	16UI	00.00	RW	Defines the left hand edge of the vertical cursor. A value of 0x0FFF switches the vertical cursor into automatic mode where it automatically advances every frame.
0x0611	Lo					

1. On cut2.x silicon, the pedestal value of 64d will be added to the pixel value. To disable the pedestal, set 0x31D0= 00, 0x31E8=0, 0x3120=0x00. (The lens shading block must also be disabled).
2. This mode must be entered and exited via software standby. The embedded data lines will also be output.
3. Some clipping of these values may occur to prevent false sync codes being generated

4.11 Fifo water mark registers [0x0700 to 0x0701]

Table 22. Fifo water mark registers [0x0700 to 0x0701]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0700	Hi	fifo_water_mark_pixels	16UI	00.28	RW	The level at which data starts to be transmitted out of the FIFO (default = 40)
0x0701	Lo					

4.12 DPHY registers [0x0810 to 0x0811]

Table 23. DPHY registers [0x0810 to 0x0811]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0820	Hi	dphy_channel_mbps_for_ui	32UI	00.00	RW	CSI-2 DPHY channel in Mbps (16.16 fixed point) This is used by the DPHY to calculate UI(Unit Interval) value. It does not control the sensor clock set-up, but should normally correspond to those settings. 0: Sensor automatically calculates UI from the op_sys_clk_freq_mhz value. 80-800: Sensor calculates UI from this value.
0x0821	3rd					
0x0822	2nd					
0x0823	Lo					

4.13 Binning registers [0x0900 to 0x0902]

Table 24. Binning registers [0x0900 to 0x0902]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0900		binning_mode	8UI	00	RW	Binning Mode 0 - Disabled 1 - Enabled
0x0901		binning_type	8UI	00	RW	High-nibble - column binning factor Low-nibble - row binning factor
0x0902		binning_weighting	8UI	00	RW	bit0: Averaged (1-enable) bit2: Bayer corrected (1-enable)

4.14 Data transfer registers [0x0A00 to 0x0A02]

Table 25. Data transfer registers [0x0A00 to 0x0A02]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0A00		if1_ctrl	8UI	00	RW	Bit0: 0 - IF1 transfer disabled 1 - IF1 transfer enabled Bit1: 0 - IF1 read enabled 1 - IF1 write enabled Bit2: 0 - Normal operation 1 - Clear error bits on IF1
0x0A01		if1_status	8UI	00	RW	Bit0: Read interface ready Bit1: Write interface ready Bit2: Data corrupt Bit3: Improper interface uage
0x0A02		if1_page_sel	8UI	00	RW	Select page for IF1: Page 00: NVM: 0xFC00 - 0xFC3F Page 01: NVM: 0xFC40 - 0xFC7F Page 02: NVM: 0xFC80 - 0xFCBF Page 03: NVM: 0xFCC0 - 0xFCFF Page 04: NVM: 0xFD00 - 0xFD3F Page 05: NVM: 0xFD40 - 0xFD7F Page 06: NVM: 0xFD80 - 0xFDBF Page 07: NVM: 0xFDC0 - 0xFDFF

4.15 Shading correction registers [0x0B00 to 0x0B00]

Table 26. Shading correction registers [0x0B00 to 0x0B00]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B00		shading_correction_enable	8UI	01	RW	Shading correction 0 - Disable 1 - Enable

4.16 Defect correction registers [0x0B05 to 0x0B09]

Table 27. Defect correction registers [0x0B05 to 0x0B09]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B05		mapped_couplet_correct_enable	8UI	01	RW	Mapped couplet correction 0 - Disable 1 - Enable
0x0B06		single_defect_correct_enable	8UI	01	RW	Single defect correction 0 - Disable 1 - Enable
0x0B07		single_defect_correct_weight	8UI	40	RW	Single defect correction weight 1-127 manual mode Bit[7]=1 auto, weight varies with analog gain
0x0B08		dynamic_couplet_correct_enable	8UI	00	RW	Dynamic couplet correction 0 - Disable 1 - Enable (Note: If enabled, the single defect correction will also be enabled).
0x0B09		dynamic_couplet_correct_weight	8UI	00	RW	Not used in VX6854LC

4.17 EDoF registers [0x0B80 to 0x0B8A]

Table 28. EDoF registers [0x0B80 to 0x0B8A]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B80		edof_mode	8UI	00	RW	EDoF control 0 - EDoF disabled (power saving) 1 - EDoF application (Capture) 2 - EDoF estimation (Preview)
0x0B81		edof_est_depth_of_field	8UI	00	RO	Not used in VX6854LC
0x0B82		edof_est_focus_distance	8UI	32	RO	The estimated focus point (cm)
0x0B83		edof_sharpness	8UI	00	RW	EDoF sharpness control 1-127 - manual mode 128-255 - signed offset added to internal default value.
0x0B84		edof_denoising	8UI	00	RW	EDoF denoising control 1-127 - manual mode 128-255 - signed offset added to internal default value.

Table 28. EDoF registers [0x0B80 to 0x0B8A] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B85		edof_module_specific	8UI	00	RW	EDoF noise vs. details control 1-127 - manual mode 128-255 - signed offset added to internal default value.
0x0B88	Hi	edof_focus_distance	16UI	00.32	RW	Value supplied by the host which is used by VX6854LC for focus distance. (in cm) 0x0000 to 0x7FFF - manual mode 0x8000 to 0xFFFF - auto mode
0x0B89	Lo					
0x0B8A		edof_estimation_control	8UI	00	RW	EDoF estimator control 0 - uniform 1 - uniform 2 - centre weight 4 - large spot 8 - narrow spot

4.18 Color feedback registers [0x0B8C to 0x0B95]

Table 29. Color feedback registers [0x0B8C to 0x0B95]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B8C	Hi	colour_temperature	16SR	00.00	RW	Not supported by VX6854LC
0x0B8D	Lo					
0x0B8E	Hi	host_WB_stats_green_red	16UR	01.00	RW	White balance gains to be applied by the host. These stats are used by the EDOF and the adaptive AV to estimate the color temperature of the scene.
0x0B8F	Lo					
0x0B90	Hi	host_WB_stats_red	16UR	01.00	RW	
0x0B91	Lo					
0x0B92	Hi	host_WB_stats_blue	16UR	01.00	RW	
0x0B93	Lo					
0x0B94	Hi	host_WB_stats_green_blue	16UR	01.00	RW	
0x0B95	Lo					

4.19 Integration time and gain parameter limit registers [0x1000 to 0x10FF]

These registers are used to define exposure limits for the integration control registers (0x200 to 0x203). See *Section 6.5: Exposure and gain control on page 67* for more information.

Table 30. Integration time and gain parameter limit registers [0x1000 to 0x10FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1000	Hi	integration_time_capability	16UI	00.01	RO	0x0001 – coarse and smooth (1 pixel) fine integration.
0x1001	Lo					
0x1004	Hi	coarse_integration_time_min	16UI	00.00	RO	Minimum coarse integration time. Line periods.
0x1005	Lo					
0x1006	Hi	coarse_integration_time_max_margin	16UI	00.09	RO	Current frame length – current max coarse exposure. Line periods.
0x1007	Lo					
0x1008	Hi	fine_integration_time_min	16UI	01.E5	RO	Minimum fine integration time. Pixel periods.
0x1009	Lo					
0x100A	Hi	fine_integration_time_max_margin	16UI	07.73	RO	Current line length – current max fine exposure. Pixel periods.
0x100B	Lo					
0x1080	Hi	digital_gain_capability	16UI	00.01	RO	0x01 – supports digital gain.
0x1081	Lo					
0x1084	Hi	digital_gain_min	16UR	00.08	RO	1.00000 minimum
0x1085	Lo					
0x1086	Hi	digital_gain_max	16UR	01.F8	RO	1.96875 maximum
0x1087	Lo					
0x1088	Hi	digital_gain_step_size	16UR	00.08	RO	0.03125 step size
0x1089	Lo					

4.20 Video timing parameter limit registers [0x1100 to 0x11FF]

For a full description of the video timing parameter limit registers refer to *Chapter 6: Video timing on page 55*.

Table 31. Video timing parameter limit registers [0x1100 to 0x11FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1100	Hi	min_ext_clk_freq_mhz	32SF	40.C0 00.00	RO	Minimum external clock frequency Units: MHz Value: 6.0
0x1101	3rd					
0x1102	2nd					
0x1103	Lo					
0x1104	Hi	max_ext_clk_freq_mhz	32SF	41.D8 00.00	RO	Maximum external clock frequency Units: MHz Value: 27.0
0x1105	3rd					
0x1106	2nd					
0x1107	Lo					
0x1108	Hi	min_pre_pll_clk_div	16UI	00.01	RO	Minimum Pre PLL divider value Value: 1
0x1109	Lo					
0x110A	Hi	max_pre_pll_clk_div	16UI	00.04	RO	Maximum Pre PLL divider value Value: 4
0x110B	Lo					
0x110C	Hi	min_pll_ip_freq_mhz	32SF	40.C0 00.00	RO	Minimum PLL input clock frequency Units: MHz Value: 6.0
0x110D	3rd					
0x110E	2nd					
0x110F	Lo					
0x1110	Hi	max_pll_ip_freq_mhz	32SF	41.40 00.00	RO	Maximum PLL input clock frequency Units: MHz Value: 12.0
0x1111	3rd					
0x1112	2nd					
0x1113	Lo					
0x1114	Hi	min_pll_multiplier	16UI	00.25	RO	Minimum PLL multiplier Value: 37
0x1115	Lo					
0x1116	Hi	max_pll_multiplier	16UI	00.86	RO	Maximum PLL multiplier Value: 134
0x1117	Lo					
0x1118	Hi	min_pll_op_freq_mhz	32SF	43.E1 00.00	RO	Minimum PLL output clock frequency Units: MHz Value: 450.0
0x1119	3rd					
0x111A	2nd					
0x111B	Lo					

Table 31. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x111C	Hi	max_pll_op_freq_mhz	32SF	44.7A 00.00	RO	Maximum PLL output clock frequency Units: MHz Value: 1000.0 Note: This value should be 800MHz
0x111D	3rd					
0x111E	2nd					
0x111F	Lo					
0x1120	Hi	min_vt_sys_clk_div	16UI	00.01	RO	Minimum video-timing system clock divider value Value: 1
0x1121	Lo					
0x1122	Hi	max_vt_sys_clk_div	16UI	00.04	RO	Maximum video-timing system clock divider value Value: 4 This value should be 2.
0x1123	Lo					
0x1124	Hi	min_vt_sys_clk_freq_mhz	32SF	42.F4 00.00	RO	Minimum video-timing system clock frequency Units: MHz Value: 122.0
0x1125	3rd					
0x1126	2nd					
0x1127	Lo					
0x1128	Hi	max_vt_sys_clk_freq_mhz	32SF	44.48 00.00	RO	Maximum video-timing system clock frequency Units: MHz Value: 800.0
0x1129	3rd					
0x112A	2nd					
0x112B	Lo					
0x112C	Hi	min_vt_pix_clk_freq_mhz	32SF	42.18 00.00	RO	Minimum video-timing pixel clock frequency Units: MHz Value: 38.0
0x112D	3rd					
0x112E	2nd					
0x112F	Lo					
0x1130	Hi	max_vt_pix_clk_freq_mhz	32SF	42.A0 00.00	RO	Maximum video-timing pixel clock frequency Units: MHz Value: 80.0
0x1131	3rd					
0x1132	2nd					
0x1133	Lo					
0x1134	Hi	min_vt_pix_clk_div	16UI	00.04	RO	Minimum video-timing pixel clock divider Value: 4
0x1135	Lo					
0x1136	Hi	max_vt_pix_clk_div	16UI	00.0A	RO	Maximum video-timing pixel clock divider Value: 10
0x1137	Lo					
0x1140	Hi	min_frame_length_lines	16UI	00.2A	RO	Minimum Frame Length allowed. Value = 42 lines
0x1141	Lo					

Table 31. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1142	Hi	max_frame_length_lines	16UI	FF.FF	RO	Maximum possible number of lines per Frame. Value = 65535 Units: Lines
0x1143	Lo					
0x1144	Hi	min_line_length_pck	16UI	09.C4	RO	Minimum Line Length allowed. Value = 2500 Units: Pixel Clocks
0x1145	Lo					
0x1146	Hi	max_line_length_pck	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line. Value = 16383 Units: Pixel Clocks
0x1147	Lo					
0x1148	Hi	min_line_blanking_pck	16UI	01.A8	RO	Minimum line blanking time in pixel clocks Value = 424 Units: Pixel Clocks
0x1149	Lo					
0x114A	Hi	min_frame_blanking_lines	16UI	00.24	RO	Minimum frame blanking in video lines = 36
0x114B	Lo					
0x1160	Hi	min_op_sys_clk_div	16UI	00.01	RO	Minimum output system clock divider. Value = 1
0x1161	Lo					
0x1162	Hi	max_op_sys_clk_div	16UI	00.42	RO	Maximum output system clock divider Value = 66
0x1163	Lo					
0x1164	Hi	min_op_sys_clk_freq_mhz	32SF	40.F2 6C.9B	RO	Minimum output system clock frequency Units: MHz Value: 7.57 Note that this value is 80MHz in CSI2 mode.
0x1165						
0x1166						
0x1167	Lo					
0x1168	Hi	max_op_sys_clk_freq_mhz	32SF	44.48 00.00	RO	Maximum output system clock frequency Units: MHz Value: 800.0
0x1169						
0x116A						
0x116B	Lo					
0x116C	Hi	min_op_pix_clk_div	16UI	00.08	RO	Minimum output pixel clock divider. Value = 8
0x116D	Lo					
0x116E	Hi	max_op_pix_clk_div	16UI	00.0A	RO	Maximum output pixel clock divider Value = 10
0x116F	Lo					
0x1170	Hi	min_op_pix_clk_freq_mhz	32SF	3F.41 F0.7C	RO	Minimum output pixel clock frequency Units: MHz Value: 0.757 (757 kHz)
0x1171						
0x1172						
0x1173	Lo					

Table 31. Video timing parameter limit registers [0x1100 to 0x11FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x1174	Hi	max_op_pix_clk_freq_mhz	32SF	42.A0 00.00	RO	Maximum output pixel clock frequency Units: MHz Value: 80.0
0x1175						
0x1176						
0x1177	Lo					
0x1180	Hi	x_addr_min	16UI	00.00	RO	Minimum X-address of the addressable pixel array Value: Always 0
0x1181	Lo					
0x1182	Hi	y_addr_min	16UI	00.00	RO	Minimum Y-address of the addressable pixel array Value: Always 0
0x1183	Lo					
0x1184	Hi	x_addr_max	16UI	08.0F	RO	Maximum X-address of the addressable pixel array Value = 2063
0x1185	Lo					
0x1186	Hi	y_addr_max	16UI	06.0F	RO	Maximum Y-address of the addressable pixel array Value = 1551
0x1187	Lo					
0x1188	Hi	min_x_output_size	16UI	01.00	RO	Minimum x output size in pixels. Value: 256
0x1189	Lo					
0x118A	Hi	min_y_output_size	16UI	00.04	RO	Minimum y output size in pixels. Value: 4
0x118B	Lo					
0x118C	Hi	max_x_output_size	16UI	08.10	RO	Maximum x output size in pixels. Value: 2064
0x118D	Lo					
0x118E	Hi	max_y_output_size	16UI	06.10	RO	Maximum y output size in pixels: Value: 1552
0x118F	Lo					
0x11C0	Hi	min_even_inc	16UI	00.01	RO	Minimum Increment for even pixels
0x11C1	Lo					
0x11C2	Hi	max_even_inc	16UI	00.07	RO	Maximum increment for even pixels. even_inc must = 1 for focus_estimation to operate effectively. VX6854LC only suppports y-even-inc values of 1 and 5
0x11C3	Lo					
0x11C4	Hi	min_odd_inc	16UI	00.01	RO	Minimum Increment for odd pixels
0x11C5	Lo					
0x11C6	Hi	max_odd_inc	16UI	00.07	RO	Maximum Increment for odd pixels
0x11C7	Lo					

4.21 Image scaling parameter limit registers [0x1200 to 0x12FF]

Table 32. Image scaling parameter limit registers [0x1200 to 0x12FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1200	Hi	scaling_capablility	16UI	00.02	RO	VX6854LC supports Full (horizontal & vertical) scaling.
0x1201	Lo					
0x1204	Hi	scale_m_min	16UI	00.10	RO	Down scale factor: Minimum M value = 16
0x1205	Lo					
0x1206	Hi	scale_m_max	16UI	00.81	RO	Down scale factor: Maximum M value = 129
0x1207	Lo					
0x1208	Hi	scale_n_min	16UI	00.10	RO	Down scale factor: Minimum N value = 16
0x1209	Lo					
0x120A	Hi	scale_n_max	16UI	00.10	RO	Down scale factor: Maximum N value = 16
0x120B	Lo					

4.22 Image compression parameter registers [0x1300 to 0x13FF]

Table 33. Image compression parameter limit registers [0x1300 to 0x13FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1300	Hi	compression_capablility	16UI	00.01	RO	VX6854LC supports DPCM/PCM compression
0x1301	Lo					

4.23 Color matrix registers [0x1400 to 0x14FF]

Table 34. Color matrix registers [0x1400 to 0x14FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1400	Hi	matrix_element_RedInRed	16SR	01.00	RO	Color matrix parameter for Red in Red
0x1401	Lo					
0x1402	Hi	matrix_element_GreenInRed	16SR	00.00	RO	Color matrix parameter for Green in Red
0x1403	Lo					
0x1404	Hi	matrix_element_BlueInRed	16SR	00.00	RO	Color matrix parameter for Blue in Red
0x1405	Lo					
0x1406	Hi	matrix_element_RedInGreen	16SR	00.00	RO	Color matrix parameter for Red in Green
0x1407	Lo					
0x1408	Hi	matrix_element_GreenInGreen	16SR	01.00	RO	Color matrix parameter for Green in Green
0x1409	Lo					

Table 34. Color matrix registers [0x1400 to 0x14FF] (continued)

Index	Byte	Register name	Data type	Default	Type	Comment
0x140A	Hi	matrix_element_BlueInGreen	16SR	00.00	RO	Color matrix parameter for Blue in Green
0x140B	Lo					
0x140C	Hi	matrix_element_RedInBlue	16SR	00.00	RO	Color matrix parameter for Red in Blue
0x140D	Lo					
0x140E	Hi	matrix_element_GreenInBlue	16SR	00.00	RO	Color matrix parameter for Green in Blue
0x140F	Lo					
0x1410	Hi	matrix_element_BlueInBlue	16SR	01.00	RO	Color matrix parameter for Blue in Blue
0x1411	Lo					

4.24 FIFO capability registers [0x1500 to 0x15FF]

Table 35. Fifo capability registers [0x1500 to 0x15FF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1500	Hi	fifo_size_pixels	16UI	07.00	RO	VX6854LC has a fifo of 1792 pixels Note: This value should be 1023 pixels
0x1501	Lo					

4.25 CSI lane mode capability registers [0x1600 to 0x1602]

Table 36. CSI lLane mode capability registers [0x1600 to 0x1602]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1600		ui_and_manual_dphy_ctrl_capability	8UI	03	RO	CSI2 DPHY Control capability bit0: Automatic DPHY control supported bit1:UI-based DPHY control supported
0x1601		csi_lane_capability	8UI	01	RO	One CSI-2 data lane supported
0x1602		csi_signallingmode_capability	8UI	07	RO	VX6854LC supports: bit0: CCP2 data/clock bit1: CCP2 data/strobe bit2: CSI-2

4.26 Binning capability registers [0x1700 to 0x1719]

Table 37. Binning capability registers [0x1700 to 0x1719]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1700		binning_capability	8UI	01	RO	VX6854LC supports binning
0x1701		binning_sub_type	8UI	02	RO	VX6854LC supports two binning types
0x1702		binning_type_1	8UI	22	RO	Binning type is 2x2 (col x row)
0x170B		binning_weighting_capability	8UI	05	RO	VX6854LC supports averaged and bayer corrected weighting
0x170C	Hi	min_frame_length_lines_bin	16UI	00.19	RO	Minimum Frame Length allowed in binning mode. Units: Lines
0x170D	Lo					
0x170E	Hi	max_frame_length_lines_bin	16UI	FF.FF	RO	Maximum possible number of lines per Frame allowed in binning mode. Units: Lines
0x170F	Lo					
0x1710	Hi	min_line_length_pck_bin	16UI	09.C4	RO	Minimum Line Length allowed in binning mode. Units: Pixel Clocks
0x1711	Lo					
0x1712	Hi	max_line_length_pck_bin	16UI	3F.FF	RO	Maximum possible number of pixel clocks per line. allowed in binning mode Units: Pixel Clocks
0x1713	Lo					
0x1714	Hi	min_line_blanking_pck_bin	16UI	05.A6	RO	Minimum line blanking time in pixel clocks allowed in binning mode Units: Pixel Clocks
0x1715	Lo					
0x1716	Hi	fine_integration_time_min_bin	16UI	03.86	RO	Minimum fine integration time. Pixel periods allowed in binning mode. Value should be 0x0197 for 2x2
0x1717	Lo					
0x1718	Hi	fine_integration_time_max_ margin_bin	16UI	06.3E	RO	Current line length – current max fine exposure allowed in binning mode. Pixel periods. Value should be 0x080F for 2x2
0x1719	Lo					

4.27 Data transfer capability registers [0x1800 to 0x1800]

Table 38. Data transfer capability registers [0x1800 to 0x1800]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1800		data_xfer_if_capability	8UI	0D	RO	VX6854LC supports interface 1 and requires polling for both read and write.

4.28 Shading correction capability registers [0x1900 to 0x1900]

Table 39. Shading correction capability registers [0x1900 to 0x1900]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1900		shading_correction_capability	8UI	01	RO	VX6854LC supports shading correction

4.29 Defect correction capability registers [0x1903 to 0x1903]

Table 40. Defect correction capability registers [0x1903 to 0x1903]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1903		defect_correction_capability	8UI	0F	RO	VX6854LC supports the following defect correction: bit0: Mapped couplet correction bit1: Dynamic couplet correction bit2: Single pixel defect correction bit3: Single pixel defect correction weight adjustment

4.30 EDoF capability registers [0x1980 to 0x19C0]

Table 41. EDoF capability registers [0x1980 to 0x19C0]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1980		edof_capability	8UI	01	RO	VX6854LC supports EDoF
0x1981		edof_estimation_frames	8UI	01	RO	One estimation frame is required before EDoF is applied
0x1982		edof_supports_sharpness_adj	8UI	03	RO	VX6854LC supports sharpness adjustment
0x1983		edof_supports_denoising_adj	8UI	03	RO	VX6854LC supports denoising adjustment
0x1984		edof_supports_module_specific_adj	8UI	03	RO	VX6854LC supports noise vs details adjustment
0x1985		edof_supports_depth_of_field_adj	8UI	00	RO	VX6854LC does not support depth of field adjustment
0x1986		edof_supports_focus_distance_adj	8UI	03	RO	VX6854LC supports focus distance adjustment
0x1988		edof_supports_ab_2x2	8UI	02	RO	VX6854LC does not support binning 2x2 with EDoF
0x19C0		edof_estimation_mode_capability	8UI	0F	RO	EDoF supports following types: bit 0: uniform bit 1: centre weight bit2: large spot bit3: narrow spot

4.31 Color feedback capability registers [0x1987 to 0x1987]

Table 42. Color feedback capability registers [0x1987 to 0x1987]

Index	Byte	Register name	Data type	Default	Type	Comment
0x1987		colour_feedback_capability	8UI	02	RO	VX6854LC requires AWB gain feedback

4.32 Manufacturer specific registers [0x3000 to 0x3FFF]

Table 43. Manufacturer specific registers [0x3000 to 0x3FFF]

Index	Byte	Register name	Data type	Default	Type	Comment
0x3050		dark_setup	8B	05	RW	Bit_0: 0 : Do not apply any offset. 1 : Apply an offset.
0x3516	Hi	pll_mod_period	16UI	00.00	RW	SSCG config input to set modulation period and depth (13bit)
0x3517	Lo					
0x3518	Hi	pll_inc_step	16UI	00.00	RW	SSCG config input to set modulation depth (15bit)
0x3519	Lo					
0x5024		sscg_static_ctrl	8B	00	RW (1)	Bit0: 0 - SSCG deactivated 1 - SSCG activated Bit1: 0 - SSCG - center spread 1 - SSCG - down spread

1. In order to read this register, the non-SMIA address range must be enabled by writing 0x3640=0.

5 Video data interface

The video stream which is output from the VX6854LC using the compact camera port (CCP) or camera serial interface (CSI) contains both video data and other auxiliary information. This chapter describes the frame formats.

The VX6854LC is SMIA version 1.0 and MIPI CSI-2 version 1.00 and D-PHY 0.90 compliant.

The selection of the video data format is controlled using the following register: CSI_SIGNALLING_MODE (0x0111)

0 - CCP2 Data/Clock

1 - CCP2 Data/strobe

2 - CSI-2 (default)

Changing the video data format must be performed when the sensor is in software standby.

- The VX6854LC has one CSI-2 data lane capable of transmitting at 800 Mbps.
- The CSI-2 data lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MUYN function
- The CSI-2 clock lane transmitter supports:
  - unidirectional master
  - HS-TX
  - LP-TX (ULPS)
  - CIL-MCNN function

5.1 Frame format

The frame format for the VX6854LC is described by the frame format description registers, see *Table 13 on page 31*. For CCP this results in a frame as shown in *Figure 12* and for CSI it results in a frame as shown in *Figure 13.*

Figure 12. VX6854LC CCP frame format

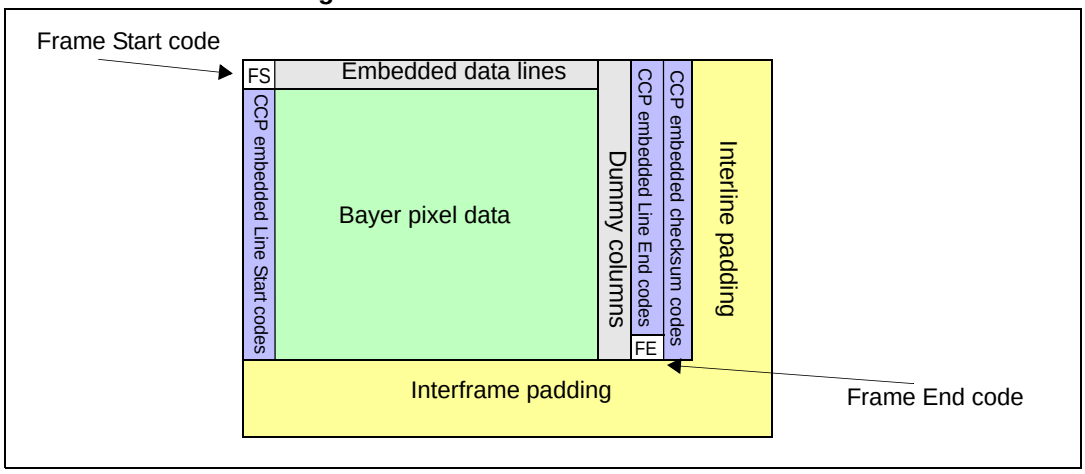
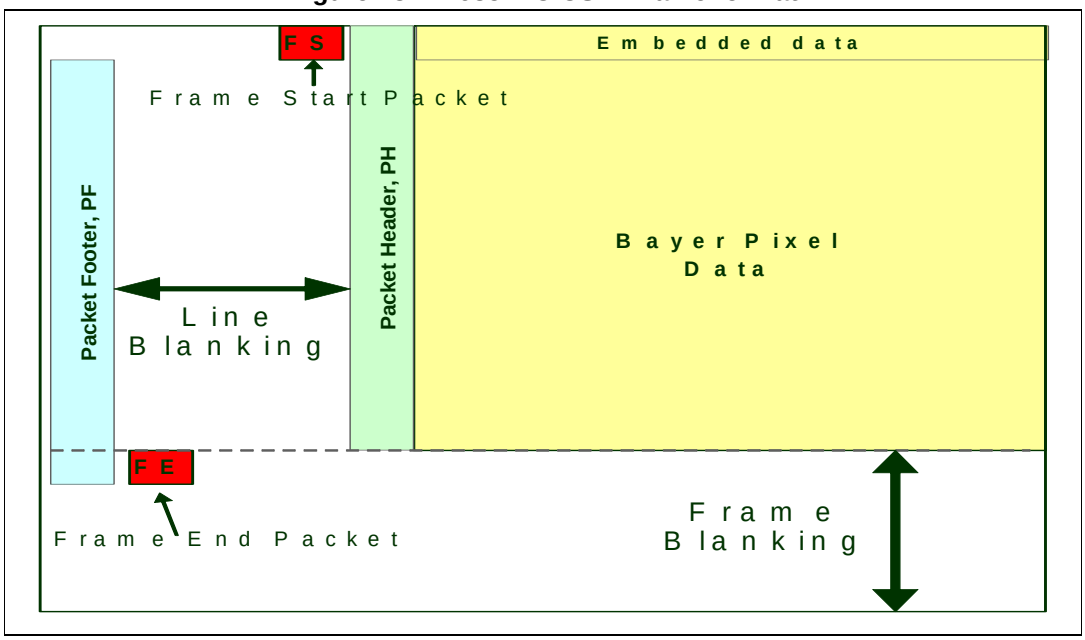


Figure 13. VX6854LC CSI-2 frame format



Embedded data lines

The embedded data lines provide a mechanism to embed non-image data such as sensor configuration details and image statistics values with a frame of data.

VX6854LC has two embedded data lines at the start of the frame.

Dummy columns

The VX6854LC has 0 dummy columns.

Visible pixel data

The visible pixels contain valid image data.The correct integration time and analogue gain for the visible pixels is specified in the embedded data lines at the start of the frame. The number of visible pixels can be varied.

Black pixel data (zero integration time)

The VX6854LC has 0 black pixels.

Dark pixel data (light shielded pixels)

The VX6854LC has 0 dark pixels.

Manufacturer specific pixel data

The VX6854LC has 0 manufacturer specific pixels.

Interline padding/line blanking

During interline padding all bits in the data stream in a CCP frame are set to 1.

In a CSI-2 frame there is no concept of line blanking being transmitted, the sensor will simply spend a longer time in the LP state between active line data.

Interframe padding / frame blanking

During interframe padding all bits in the data stream in a CCP frame are set to 1.

In a CSI-2 frame there is no concept of frame blanking being transmitted, the sensor will simply spend a longer time in the LP state at the end of the active data for a frame.

6 Video timing

6.1 Output size

The VX6854LC has the following methods available to achieve the required output size, these can be used independently or in conjunction with any other:

- programmable addressable region of the pixel array
- programmable width and height for output image data
- scaling
- subsampling

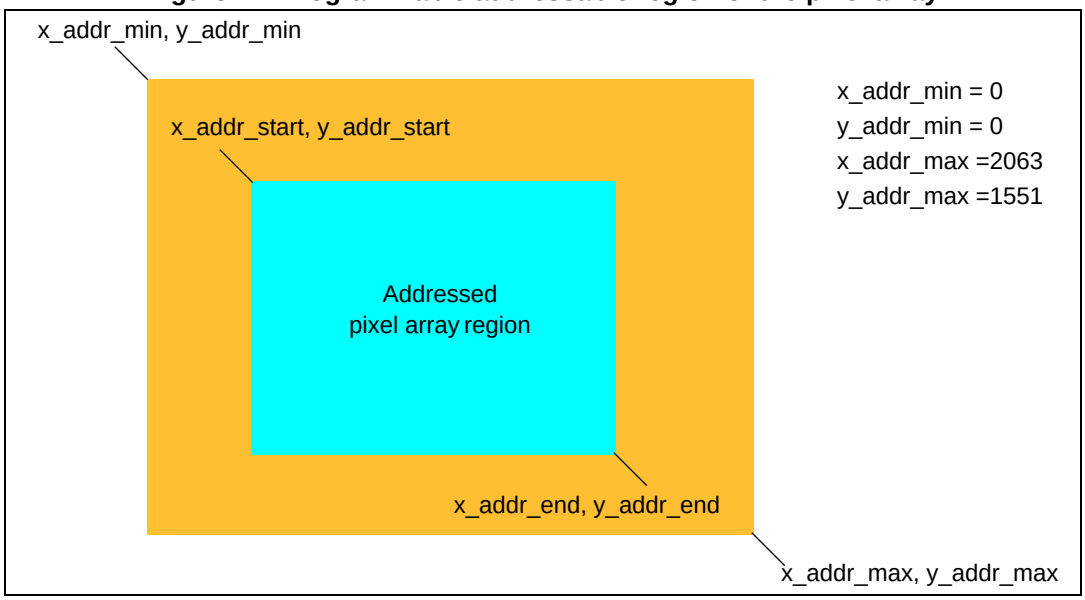
The programmable image size and output size are independent functions. It is the responsibility of the host to ensure that these functions are programmed correctly for the intended application. These functions also reduce the amount of data and therefore reduce the peak data rate of CCP2/CSI-2.

6.1.1 Programmable addressable region of the pixel array

The native size for the VX6854LC is 2048 x 1536, the maximum addressable array is 2064 x 1552 which gives border (outer 8 rows and 8 columns) pixels for the color reconstruction algorithms to use at the edges of the array.

By programming the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers it is possible to use the full size of the array as you would do for a native size output or you can select a “window of interest”. The addressed region of the array is used in any subsequent sub-sampling or scaling.

Figure 14. Programmable addressable region of the pixel array



The host must ensure the following rules are kept:

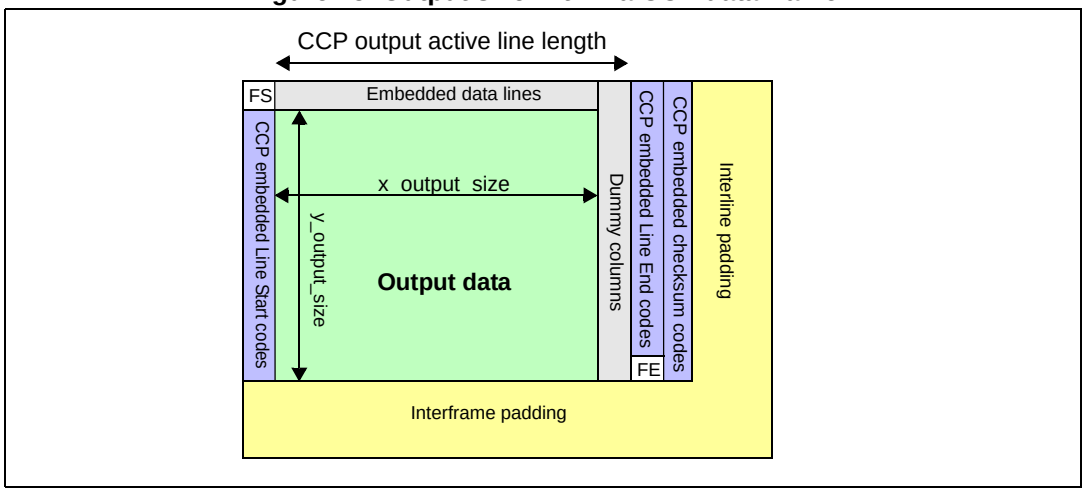
- the end address must be greater than the start address
- the x and y start addresses are restricted to even numbers only, and the x and y end addresses are restricted to odd numbers only, to ensure that there is always a even number of pixels readout

6.1.2 Programmable width and height for output image data

The x_output_size and y_output_size registers are not intended as the primary cropping controls.

They are intended to define the position of the LE/FE codes in the CCP data frame so that the sensor does not need to calculate this based on region of interest or sub-sampling settings. It should be expected that the host will set the output sizes to exactly enclose the output image data. If the host should not do this, the VX6854LC will treat the output sizes as being calculated from the top left hand corner of the output array. So in the case where output sizes are smaller than the output data, the data shall be cropped from its right hand and lower limits. In the case where larger than the output data, the lines shall be padded out to the defined output size with undefined data.

Figure 15. Output size within a CCP data frame



Note: CCP2 requires that the number of pixels between the line start and line end sync codes for:

- *RAW8 is a multiple of 4 pixels*
- *RAW10 is a multiple of 16 pixels*

The host must control the x_output_size to ensure that the above criteria is met.

6.1.3 Scaling

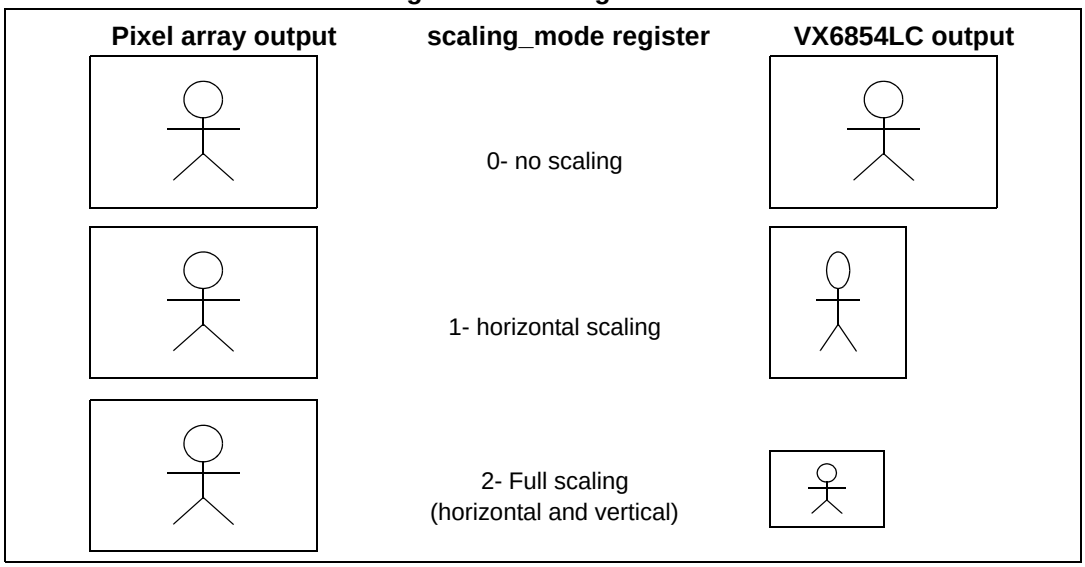
The VX6854LC module is compliant with the “Profile Level 2 - Full (Horizontal & Vertical)” level of image scaling.

The image scaling function within the sensor module provides a flexible way of generating lower resolution full field of view image data, at a reduced data rates, for viewfinder and video applications.

The scaler is able to scale the full resolution of the sensor module down to within 10% of a the target image size (the smallest output size is 256x192). This flexibility means that the VX6854LC module can support a wide range of LCD viewfinder sizes and different codec resolutions.

The VX6854LC has three scaling modes which are controlled by the scaling_mode register as shown in *Figure 16*.

Figure 16. Scaling modes



Scaler quality

The scaler supports two options for the spatial sampling of the scaled image data (see *Figure 17*):

- Bayer sampled scaled image data

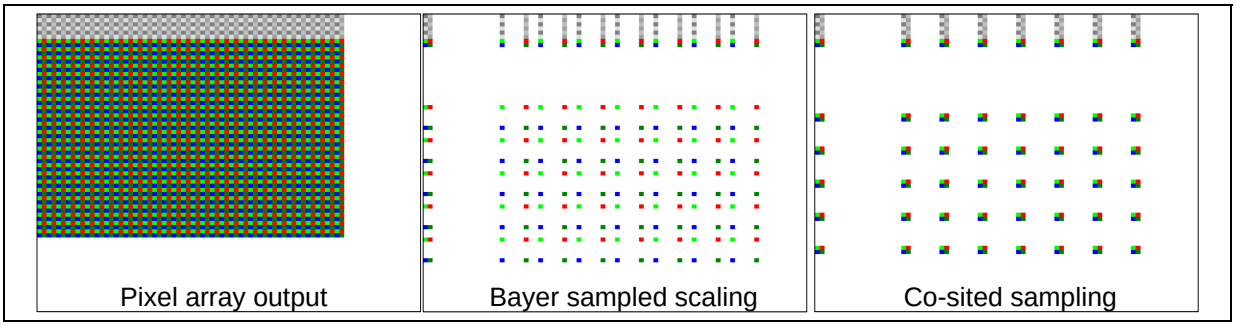
  The sampling point for the scaler for the output Gr value appears to be in the centre of the Gr pixel (that is, between the first and second pixels and between the first and second rows of the original input Bayer pixel data). The R (or B) sampling points are similarly in the centre of the R pixel (or B pixel).

- Co-sited scaled image data

  The sampling point for the Gr, R. Gb and B vales in each output ‘quad’ are functions of the same colour input array pixels such that the spatial sampling point for all four appears to be in the centre of the ‘quad’, that is, between the second and third pixels and between the first and second rows.

The spatial sampling mode is controlled by the spatial_sampling register.

Figure 17. Scaler quality



Down scaler factor

The down scaler factor is controlled by an M/N ratio, scale_m is >= 16 and scale_n is fixed at 16. scale_m is in the range 16 to 129.

$$\text{down\_scale\_factor} = \frac{\text{scale\_m}}{\text{scale\_n}} = \frac{\text{scale\_m}}{16}$$

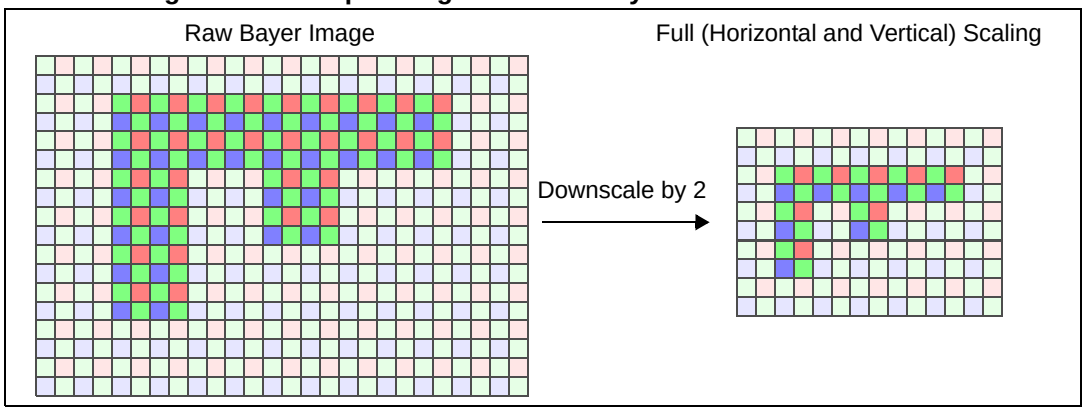
This single down scale factor is used by both the horizontal and vertical scalers.

The scaler acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

If the down scale factor is greater than 1.0, then the derating factor must also be set greater than 1.0. Refer to *Section 6.2.4: Derating on page 63* for details.

Note: The derating can be set to a minimum value, for example if op_pix_clk_div=10, setting vt_pix_clk_div=9 would meet this requirement.

Figure 18. Example image full scaled by a downscale factor of 2



6.1.4 Subsampling

Subsampling is achieved by programming the x _odd_inc, y_odd_inc, x_even_inc and y_even_inc registers.

If the pixel being readout has an even address then the address is incremented by the even increment value either x_even_inc or y_even_inc. If the pixel being readout has an odd address then the address is incremented by the odd increment value either x _odd_inc or y_odd_inc.

The sub_sampled readout is disabled by setting the odd and even increment values to 1.

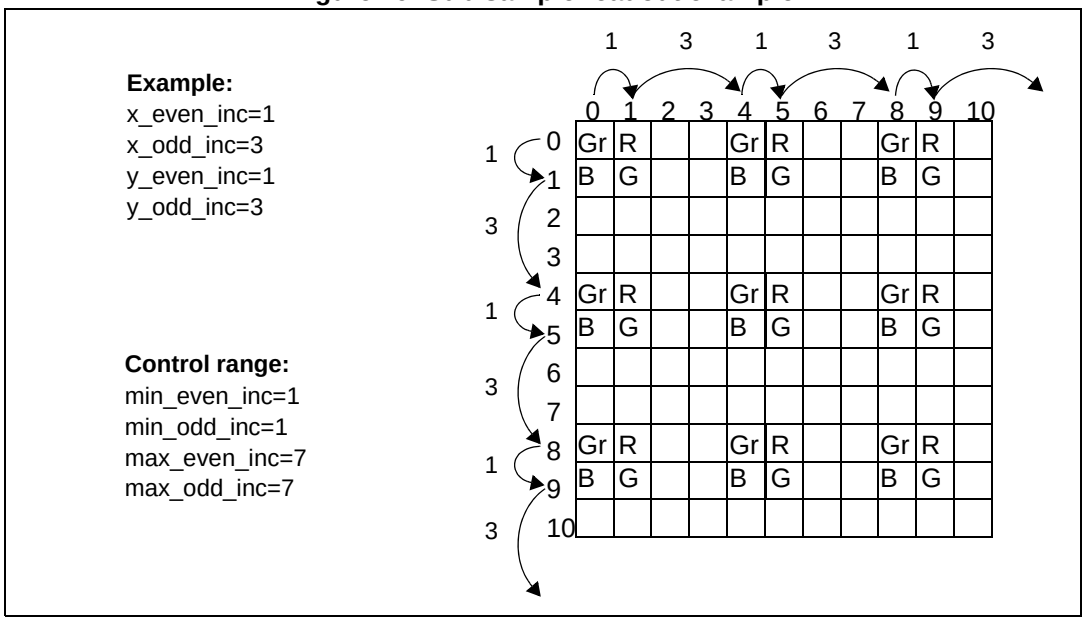
Sub-sampling acts upon the addressed region of the array which is determined by the x_addr_start, y_addr_start, x_addr_end and y_addr_end registers.

For the EDOF focus estimation to operate effectively, the x_even_inc and y_even_inc registers must be 1.

The equation for the sub-sampling factor is given below:

$$\text{sub\_sampling\_factor} = \frac{\text{even\_inc} + \text{odd\_inc}}{2}$$

Figure 19. Sub-sample readout example



6.1.5 Binning

The VX6854LC also has a binning mode, that offers a reduced size full field of view image. The binning mode averages row and column pixel data.

The binning mode results in a reduced number of lines and so can be used to give a higher image frame rate. Compared to sub-sampling, binning makes use of the light gathered from the whole pixel array and it results in higher image quality.

The binning mode will scale by 2x2 in the X and Y direction.

For cut 1 silicon, entering and exiting binning mode must be performed when the sensor is in software standby. (This is not a requirement for cut 2.x silicon).

Table 44 summarizes the register settings for each of the binning modes. Refer to the personality file for additional settings to optimise the image quality performance.

Table 44. Binning register settings

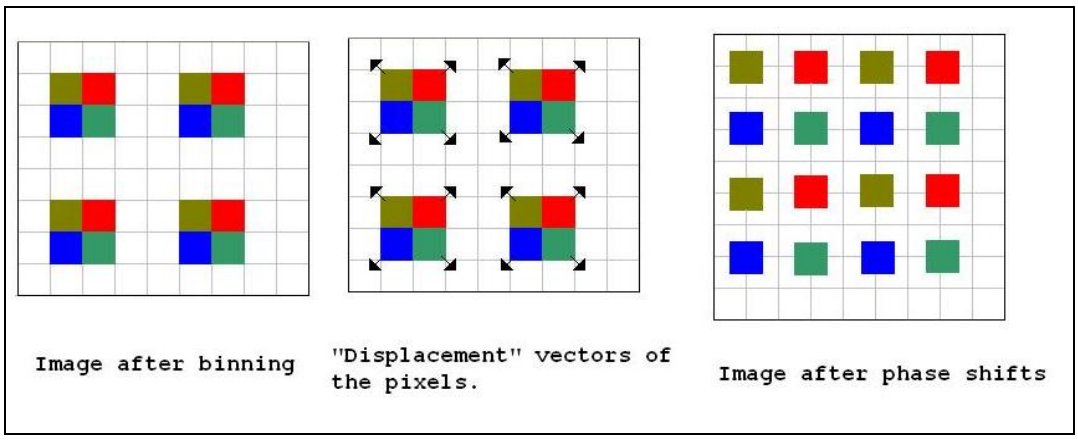
Register	Address	Normal	2x2
binning_mode	0x0900	0x00	0x01
binning_type	0x0901	N/A	0x22
binning_weighting	0x0902	N/A	0x04
x_odd_inc	0x0383	0x01	0x03
y_odd_inc	0x0387	0x01	0x03

Binning repair

Binning can introduce some phases errors from the image perspective as it clusters the output of each color channel. Gr, R, B and Gb binned pixels are located around the same intersection point on the output lattice.

To reduce this error, a binning IP is integrated into the imaging data path. The IP moves each binned color channel by 1/8th of an inter-pixel distance. Therefore the top-left Gr pixel moves into the top-left corner, the R pixel in the top-right moves in the top-right direction. This is shown in *Figure 20*.

Figure 20. Binning repair



6.2 Video timing

This section specifies the timing for the image data that is readout from the pixel array and the output image data. These are not necessarily the same size.

The application of all of the video timing read/write parameters must be re-timed to the start of frame boundary to ensure that the parameters are consistent within a frame.

The video stream which is output from the VX6854LC contains both video data and other auxiliary information. The VX6854LC output coding conforms to the CCP Raw8 and Raw10 data format (see SMIA 1.0 Part 2:CCP2 Specification) including line checksums.

Reference SMIA 1.0 Specification section 5 for detailed description of video timing.

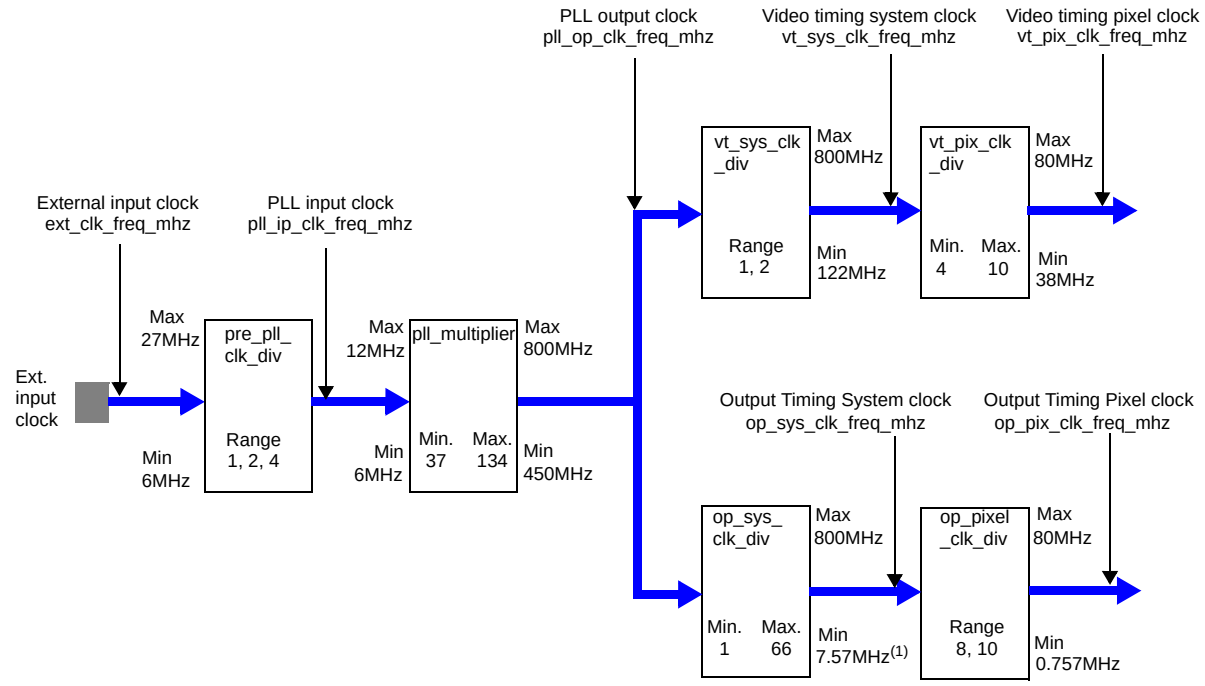
6.2.1 PLL block

The VX6854LC contains a PLL (phase locked loop) block, which generates all the necessary internal clocks from the external clock input. Changes to the PLL settings on the VX6854LC will only be consumed on the software standby to streaming mode transition.

Figure 21 shows the internal functional blocks, which define the relationship between the external input clock frequency and the pixel clock frequency.

The majority of the logic within the device is clocked by vt_sys_clk however the CCI block is clocked by the External input clock.

Figure 21. VX6854LC clock relationships



1. Note that the minimum op_sys_clk_freq_mhz is 80MHz in CSI2 mode.

The equation relating the input clock frequency to pixel clock frequencies are given below:

$$vt\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times vt\_sys\_clk\_div \times vt\_pix\_clk\_div}$$

$$op\_pix\_clk\_freq\_mhz = \frac{ext\_clk\_freq\_mhz \times pll\_multiplier}{pre\_pll\_clk\_div \times op\_sys\_clk\_div \times op\_pix\_clk\_div}$$

6.2.2 Spread spectrum clock generator

The PLL contains a spread spectrum clock generator block (SSCG) for the purposes of EMI reduction. This feature is off by default and is intended for use if channel blocking becomes an issue on the baseband platform. A primary source of EMI is the high speed CCP serial data link. The modulation period and depth are fully programmable. The spread mode is selectable between center spread (default) or down spread. The SSCG registers can only be reprogrammed with new values when the sensor is in software standby mode.

6.2.3 Framerate

The framerate of the array readout and therefore the output framerate is governed by the line length, frame length and the video timing pixel clock frequency.

- Line length is specified as a number of pixel clocks, line_length_pck.
- Frame length is specified as a number of lines, frame_length_lines.
- Video timing pixel clock is specified in MHz, vt_pix_clk_freq_mhz.

The equation relating the framerate to the Line length, frame length and the video timing pixel clock frequency is given below:

$$Framerate = \frac{vt\_pix\_clk\_freq\_mhz}{line\_length\_pck \times frame\_length\_lines}$$

Table 45 provides examples of frame timing for Raw10 mode for 20 fps for a variety of external clock frequencies.

Table 45. External clock frequency examples, 3.15 Mpixel Raw10 20 fps (CSI-2 only)

Ext Clk Freq	Pre-PLL Clk Div	PLL multiplier	VT Sys Clk Div	VT pixel Clk Div	Video timing pixel clock	Line length		Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Pixel Clks	µs	Lines (Dec)
9.60	1	83	1	10	79.680	2500	31.37	1594
12.00	2	133	1	10	79.800	2500	31.32	1596
13.00	2	123	1	10	79.950	2500	31.27	1599

Table 46 provides examples of frame timing for Raw10 mode for 15 fps for a variety of external clock frequencies.

Table 46. External clock frequency examples, 3.15 Mpixel Raw10 15 fps (CSI-2 or CCP)

Ext Clk Freq	Pre-PLL Clk Div	PLL multi-plier	VT Sys Clk Div	VT pixel Clk Div	Video timing pixel clock	Line length		Frame length
MHz	Integer	Integer (Dec)	Integer	Integer	MHz	Pixel Clks	µs	Lines (Dec)
9.60	1	66	1	10	63.360	2500	39.46	1690
12.00	2	106	1	10	63.600	2500	39.31	1696
13.00	2	98	1	10	63.700	2500	39.25	1699

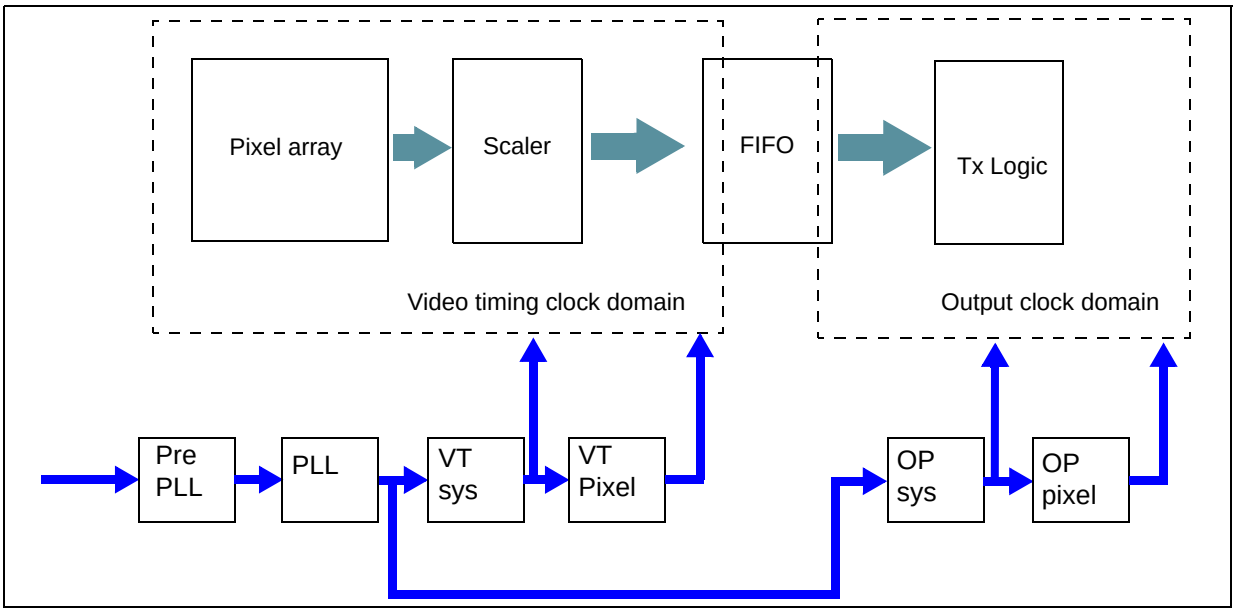
Note: op_sys_clk_div should equal vt_sys_clk_div and op_pix_clk_div should equal vt_pix_clk_div for these examples.

6.2.4 Derating

To provide a wide range of data rate reduction options the full image scaler is able to reduce the data and therefore data rates in both the horizontal and vertical directions. In the VX6854LC this is achieved by the use of a FIFO between video timing and output clock domains.

It is therefore necessary for the host to configure the OP clock domain to ensure that the FIFO neither over flows or under flows

Figure 22. Timing block diagram



Derating shows the difference between the video timing domain and the output clock domain.

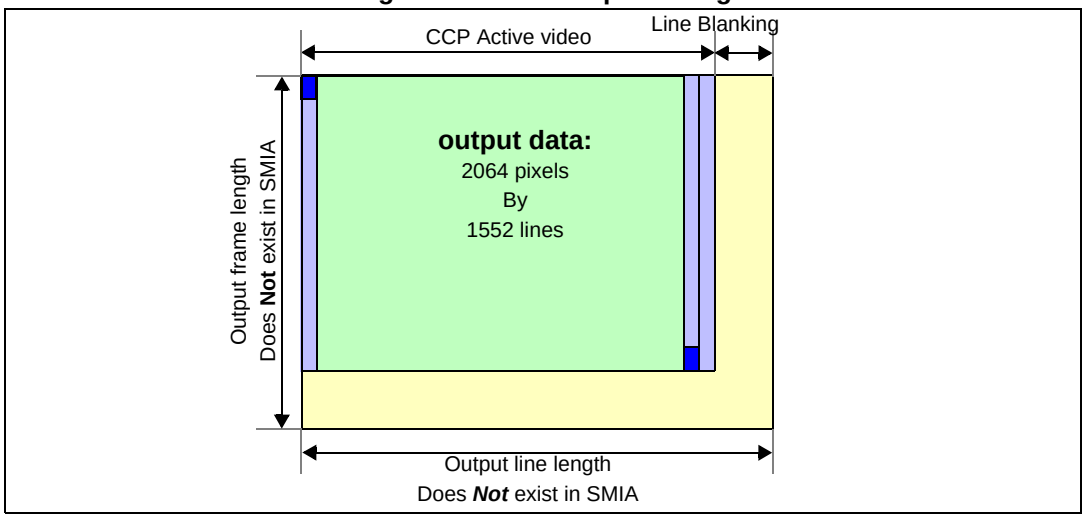
$$\text{derating} = \frac{\text{op\_sys\_clk\_div} * \text{op\_pix\_clk\_div}}{\text{vt\_sys\_clk\_div} * \text{vt\_pix\_clk\_div}}$$

FIFO

The FIFO is used to implement the data rate reduction required for profile 1 and 2 operation.

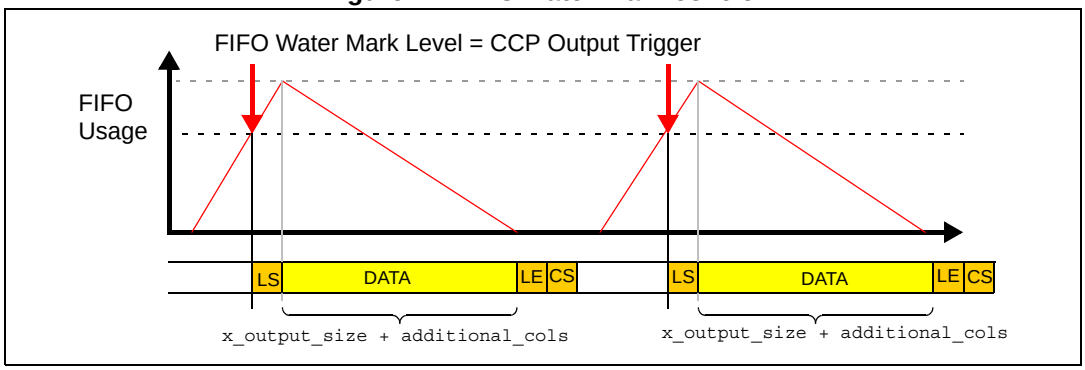
The concept of an output frame length and a line length for the output timing domain does not exist for SMIA devices such as the VX6854LC. This is a result of the FIFO input data patterns being different depending on scaling factor and if the data is co-sited or bayer sampled, which results in variable interframe and interline blanking time between lines and between frames.

Figure 23. SMIA output timing



When the FIFO reaches a certain level of usage the CCP transmitter starts outputting a line containing x_output_size pixels. This then naturally tracks any variation in the input data rate, if the water mark is set correctly underflow is not possible.

Figure 24. FIFO water mark control



If the derating factor >= downscale factor then the average input rate of a burst of a line of scaler output data into the FIFO is always faster than the output data rate, in this case the

fifo_water_mark_pixels can be set to 40 as the FIFO input data rate is always faster than the FIFO output data rate.

If the derating factor < downscale factor then the average input rate of a burst of a line of scaler output data into the FIFO is slower than the output data rate, in this case the fifo_water_mark_pixels must be set to avoid underflow.

Calculate the floating point value of the fifo_water_mark_pixels

$$\text{fifo\_water\_mark\_pixels(flt)} = \frac{\text{scale\_factor - derating}}{\text{scale\_factor}} * \text{x\_output\_size}$$

Then round up this value;

fifo_water_mark_pixels = fifo_water_mark_pixels(flt) + 40

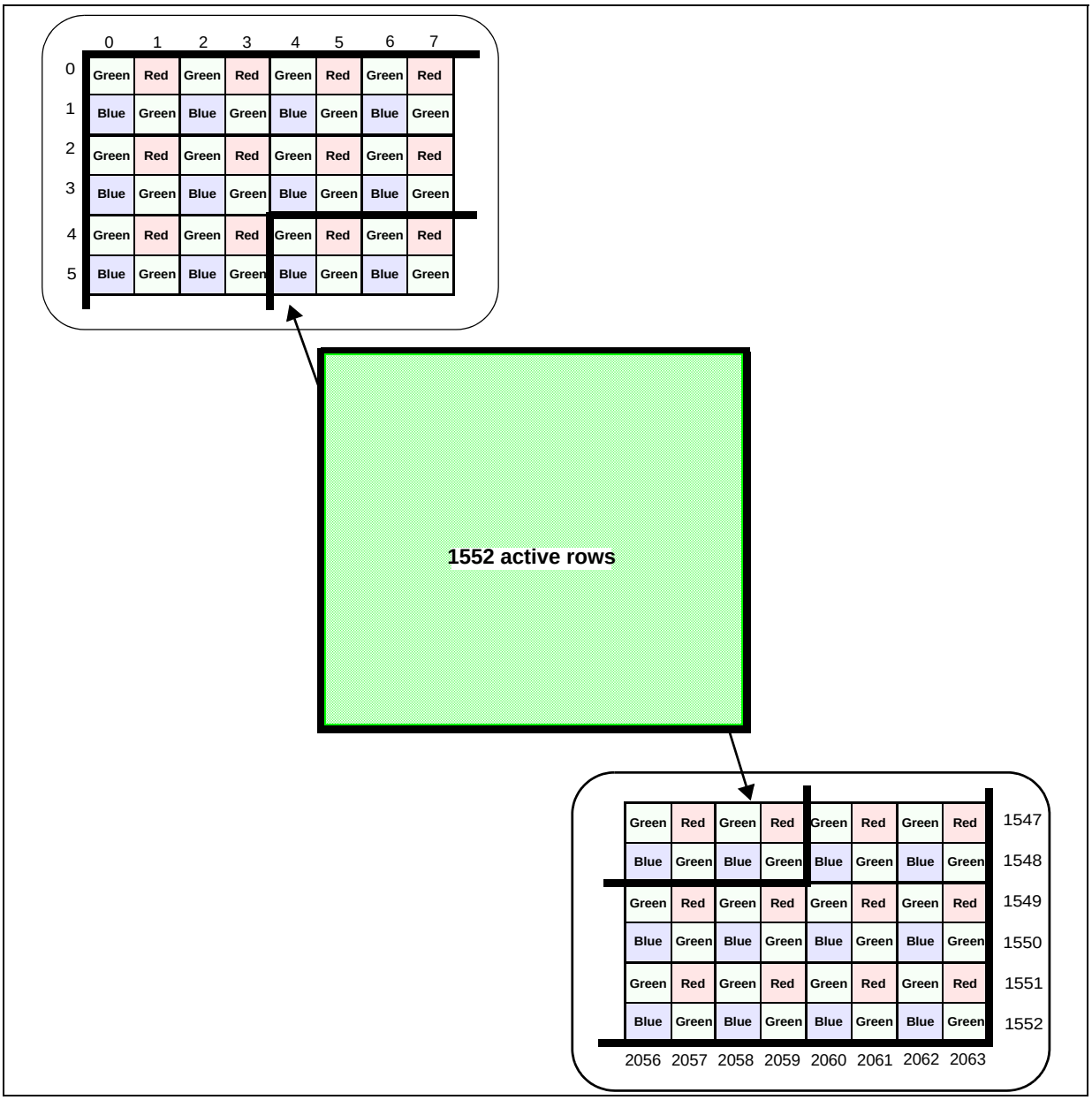
6.3 Bayer pattern

The three color (Red, Green, Blue) filters are arranged over the pixel array in a repeated 2x2 arrangement known as the Bayer Pattern. When the sensor array is read, the output order of red, green, blue depends on the settings of vertical flip and horizontal mirror.

See *Figure 25* for read-out order for the default settings of vertical flip and horizontal mirror both turned off. Vertical flip will change the first line to be output from a green/red line to a blue/green line and horizontal mirror will change the sequence within a line, say, green/red to red/green.

As shown in *Figure 25*, the first pixel to be readout from the imaging array will be green followed by red.

Figure 25. Bayer pattern



6.4 Image compression

The objective of the image compression is to reduce the required bandwidth in transmission between the sensor and the host.

The key features of the DPCM/PCM compression algorithm are:

- visually lossless
- low cost implementation (no line memories are required)
- fixed rate compression

The 10-bit to 8-bit DPCM/PCM image compression algorithm is supported by VX6854LC. 10-bit to 8-bit compression has the additional advantage that one pixel value equals 1 byte of data.

The level of compression is controlled via the CSI_data_format register. The same register is also used to enable and disable compression.

The compression_mode register is used to select which compression algorithm is used. Currently only the DPCM/PCM technique is supported. Therefore the value of this register is always 0x01.

The compression_capability register tells the host whether a sensor module does or does not have compression and if it has compression then what is the compression technique. Again currently only the DPCM/PCM technique is supported.

Please also refer to section 10 of the SMIA1.0 specification document.

6.5 Exposure and gain control

VX6854LC does not contain any form of automatic exposure control. To produce a correctly exposed image the integration period and analogue gain for the pixels must be calculated by an exposure control algorithm implemented externally. The parameters are written to the VX6854LC using the CCI interface.

The exposure control parameters available on VX6854LC are:

- fine integration time
- coarse integration time
- analogue gain
- digital gain

The exposure control parameter registers are defined in *Chapter 4: Register map on page 29*.

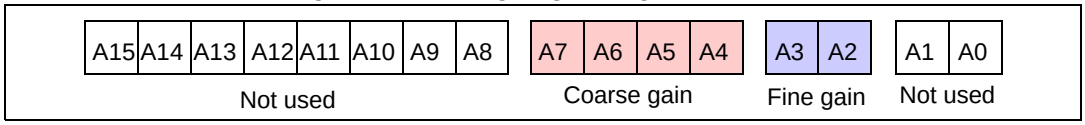
Integration time and analogue gain capability registers should be used to determine the exposure control parameter limits for a given video timing configuration. See Section 6.7 of the SMIA 1.0 part 1 specification for more information on how to interpret the integration and gain capability registers and how to calculate exposure and gain limits.

6.5.1 Analogue gain model

VX6854LC only supports the single global analogue gain mode. VX6854LC has a 16-bit register (0x0204 and 0x0205) to control analogue gain. However, only 4 bits are supported by the SMIA1.0 description. Two extra bits can be used for fine gain between values 8 and 16 but their description is not currently supported by SMIA1.0 specification.

Figure 26 shows the way the analogue gain bits are used for VX6854LC. **Use only Coarse Gain bits for standard 1/x functionality**.

Figure 26. Analogue gain register format



The following generic equation describes VX6854LC coarse gain behavior specified by the analogue gain description registers 0x008A to 0x0093:

$$gain = c0/(m1 \cdot x + c1)$$

where:

- m1 = -1
- c0 = 256
- c1 = 256

Table 47 specifies the valid analogue gain values for VX6854LC. Also refer to section 6.3 of the SMIA1.0 specification document.

Table 47. Analogue gain control

Gain value (0x0204/0x0205)	Coarse gain code [A7:A4]	Coarse analogue gain	Fine gain code [A3:A2]	Fine analogue gain
0x0000	0000	0.0 dB (x1.00)	00	N/A
0x0010	0001	0.6 dB (x 1.07)	00	N/A
0x0020	0010	1.2 dB (x1.1)	00	N/A
0x0030	0011	1.8 dB (x1.2)	00	N/A
0x0040	0100	2.5 dB (x1.3)	00	N/A
0x0050	0101	3.3 dB (x1.5)	00	N/A
0x0060	0110	4.1 dB (x1.6)	00	N/A
0x0070	0111	5.0 dB (x1.8)	00	N/A
0x0080	1000	6.0 dB(x2.0)	00	N/A
0x0090	1001	7.2 dB (x2.3)	00	N/A
0x00A0	1010	8.5 dB (x2.7)	00	N/A
0x00B0	1011	10.1 dB (x3.2)	00	N/A
0x00C0	1100	12.0 dB (x4.0)	00	N/A
0x00D0	1101	14.5 dB (x5.3)	00	N/A
0x00E0	1110	18.1 dB (x8.0)	00	N/A
0x00E4	1110	fine ctrl	01	19.2 dB (x9.1)
0x00E8	1110	fine ctrl	10	20.6 dB (x10.7)
0x00EC	1110	fine ctrl	11	22.1 dB (x12.8)
0x00F0	1111	24.1 dB (x16.0)	00	N/A

6.5.2 Digital gain

To help compensate for the relatively coarse analogue gain steps, VX6854LC contains a digital multiplier to “fill” in the missing steps. By mixing analogue and digital gain it is possible to implement 3% gain steps across the full 1x to 16x gain range

The details of the digital gain implementation are:

- four individual 16-bit digital channel gains (one per Bayer channel)
  - digital_gain_greenR (0x020E and 0x020F)
  - digital_gain_red (0x0210 and 0x0211)
  - digital_gain_blue (0x0212 and 0x0213)
  - digital_gain_greenB (0x0214 and 0x0215)
- the digital gain range for each channel is 1.000 to 1.96875 in steps of 0.03125 (1/32), that is, 5 fractional bits
  - digital_gain_min {0x1084:0x1085} = 0x0100 (1.00)
  - digital_gain_max {0x1086:0x1087} = 0x01F8 (1.96875)
  - digital_gain_step {0x1088:0x1089} = 0x0008 (0.03125)

6.5.3 Integration and gain parameter re-timing

The modification of exposure parameter (coarse, fine, clock division or gain) register values does not take effect immediately.

The exact time at which changes to certain parameters take effect is controlled both to ensure that each frame of image data produced has consistent settings and that changes in groups of related parameters are synchronized.

To eliminate the possibility of the sensor array seeing only part of the new exposure and gain setting, if the serial interface communications extends over a frame boundary, the internal re-timing of exposure and gain data is disabled while writing data to the serial interface register map. Thus if the 5 bytes of exposure and gain data is sent as an auto-increment CCI sequence, it is not possible for the sensor to consume only part of the new exposure and gain data.

However if it is not possible for the host to use auto-increment CCI register accesses and only discrete register accesses are possible then the VX6854LC has a mechanism to temporarily suspend the automatic application of updated exposure register values.

A group of parameter changes is marked by the host using a dedicated Boolean control parameter, grouped_parameter_hold (register 0x0104). Any changes made to “retimed” parameters while the grouped_parameter_hold signal is in the “hold” state will be considered part of the same group. Only when the grouped_parameter_hold control signal is moved back to the default “no-hold” state should the group of changes be executed.

7 Electrical characteristics

Refer to SMIA Characterization Specification - Revision 1, SMIA CCP2 Specification ECR0002 - Revision 1 and SMIA CCP2 Specification - Revision 1 (see *Table 3: Reference documents on page 14*). Typical values quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified.

7.1 Operating conditions

Table 48. Operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Voltage					
VDIG	Digital power supply	1.68	1.8	1.92	V
VANA	Analog power supply	2.3	2.8	2.9	V
VIP(DIG)	Digital input voltage(1)	0	-	1.92	V
Temperature					
T_{AS}	Temperature (storage(2))	-40	-	+85	°C
T_{AF}	Temperature (functional operating(3))	-30		+70	°C
T_{AN}	Temperature (normal operating(4))	-25		+55	°C
T_{AO}	Temperature (optimal operating(5))	+5		+40	°C
T_{AT}	Temperature (test(6))	+21		+25	°C

1. Digital input: EXTCLK, XSHUTDOWN, SCL, SDA
2. Camera has no permanent degradation.
3. Camera is electrically functional.
4. Camera produces “acceptable” images.
5. Camera produces optimal optical performance.
6. 100% tested parameters are measured at this temperature.

7.2 Absolute maximum ratings

Table 49. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DIGMAX}	Digital power supply	-0.3	2.2	V
V_{ANAMAX}	Analog power supply	-0.3	3.2	V
V_{IHMAX}	EXTCLK, XSHUTDOWN, SCL, SDA	-0.3	VDIG + 0.5	V
V_{CAP}	VCAP analogue voltage	-0.3	4.2	V
T_{STO}	Storage temperature	-40	+ 85(1)	°C
V_{ESD}	Electrostatic discharge model Human body model (2) Charge device model(3)	 -2.0 -500	 2.0 500	 kV V

1. This is a maximum long term standard storage temperature, see soldering profile for short term high temperature tolerance.
2. HBM tests are performed in compliance with JESD22-A114F
3. CDM tests are performed in compliance with JESD22-C101D

Caution: Stresses above those listed under “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.3 Power supply

7.3.1 Power supply - VDIG, VANA

Table 50. Power supplies VDIG, VANA

Parameter	Digital		Analogue		Unit
	Typ.	Max.	Typ.	Max.	
Hardware standby	10	30	10	40	µA
Software standby: Ext. clock not switching Ext. clock = 9.6MHz(1)	 7 10	 20 25	 0.6 0.6	 1.0 1.0	 mA mA
Streaming: Preview(2) Capture Still(3)	 60 65	 85 95	 40 40	 65 65	 mA mA

1. The digital current scales linearly with the external clock frequency used.
2. Profile 0, 30fps, 10-10 data, CSI-2, binning 2x2 image, EDoF estimation mode
3. Profile 0, 15fps, 10-10 data, CSI-2, full resolution image, EDoF application mode

7.3.2 Power supply (peak current) - VDIG, VANA

The peak current (in-rush) consumption of the sensor module is defined as any current pulse >=10µs. The duty cycle of the peak to the low part of the current profile is 33% with a worst-case period of 500 µs.

Table 51. In-rush current VDIG, VANA for CCP2 interface

Parameter	Digital		Analog		Unit
	Typical	Maximum	Typical	Maximum	
Boot clock peak current(1)	70	100	190	200	mA
Start streaming current(2)	60	85	190	200	mA
Stop streaming current(3)	150	160	80	90	mA
In streaming mode while changing sensor settings	150	190	90	90	mA

1. This corresponds to the transient current when XSHUTDOWN is powered up and the sensor is being set SW_Standby mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
2. When the sensor is changed from Software standby to Streaming mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
3. When the sensor is changed from streaming to Software standby. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.

Table 52. In-rush current VDIG, VANA for CSI-2 interface

Parameter	Digital		Analog		Unit
	Typical	Maximum	Typical	Maximum	
Boot clock peak current(1)	110	135	210	220	mA
Start streaming current(2)	150	230	135	160	mA
Stop streaming current(3)	160	190	140	140	mA
In streaming mode while changing sensor settings	190	230	140	140	mA

1. This corresponds to the transient current when XSHUTDOWN is powered up and the sensor is being set SW_Standby mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
2. When the sensor is changed from Software standby to Streaming mode. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.
3. When the sensor is changed from streaming to Software standby. Max value is given for Max VDD and 70c temperature. Typical value is for 25C and VDD is set to nominal value.

7.3.3 Power supply ripple requirement

It is recommended that the application meets the following requirements on the power supply signal in 10 kHz to 1.4 MHz.

Table 53. Ripple requirement

Symbol	Parameter	Max.	Unit
Ripple_VANA	Peak to peak max ripple on analogue power supply (10 kHz to 1.4 MHz)	6	mV
Ripple_VDIG	Peak to peak max ripple on digital power supply	50	mV

7.4 System clock - EXTCLK

Table 54. System clock - EXTCLK

Symbol	Parameter	Min.	Max.	Unit
	Leakage current	4(1)	30(2)	µA
V_{CL}	DC coupled square wave low level	0	0.3 * VDIG	V
V_{CH}	DC coupled square wave high level	0.7 VDIG	VDIG+0.5V	V
V_{CAC}	AC coupled sine wave	0.5	1.2	V
f_{EXTCLK}	Clock frequency input	6.0 - 1%(3)	27 + 1%(3)	MHz
Duty cycles	Clock frequency duty cycles	40	60	%
Input jitter	EXTCLK input jitter	-	Refer to Jitter application note(4)	ps

1. With DC coupled square wave clock.
2. With DC VDIG applied.
3. Nominal frequencies are 6.0 to 27 MHz with a 1% centre frequency tolerance. Tested at characterization only.
4. STMicroelectronics will provide upon request an application note detailing the EXTCLK input jitter requirements.

7.5 Power down control - XSHUTDOWN

Table 55. Power down control - XSHUTDOWN

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	Low level input voltage	0	-	0.3 * VDIG	V
V_{IH}	High level input voltage	0.7 * VDIG	-	VANA	V
I_L	Input leakage current(1)	-15		15	µA

1. With VGND ≤ $V_{XSHUTDOWN}$ ≤ VDIG

7.6 CCI interface - SDA, SCL

7.6.1 CCI interface - DC specifications

Table 56. CCI interface

Symbol	Parameter	Min.	Max.	Unit
V_{IL}	Low level input voltage	0	0.3 * VDIG	V
V_{IH}	High level input voltage (VDIG > 1.7V)	0.7 * VDIG	VDIG+0.5V	V
	High level input voltage (VDIG < 1.3V)	0.77	VDIG+0.5V	V
V_{OL}	Low level output voltage(1)	0	0.2 * VDIG	V
I_{IL}	Low level input leakage	-	-15	µA
I_{IH}	High level input leakage	-	15	µA

1. V_{OH} not valid for CCI. 3 mA drive strength

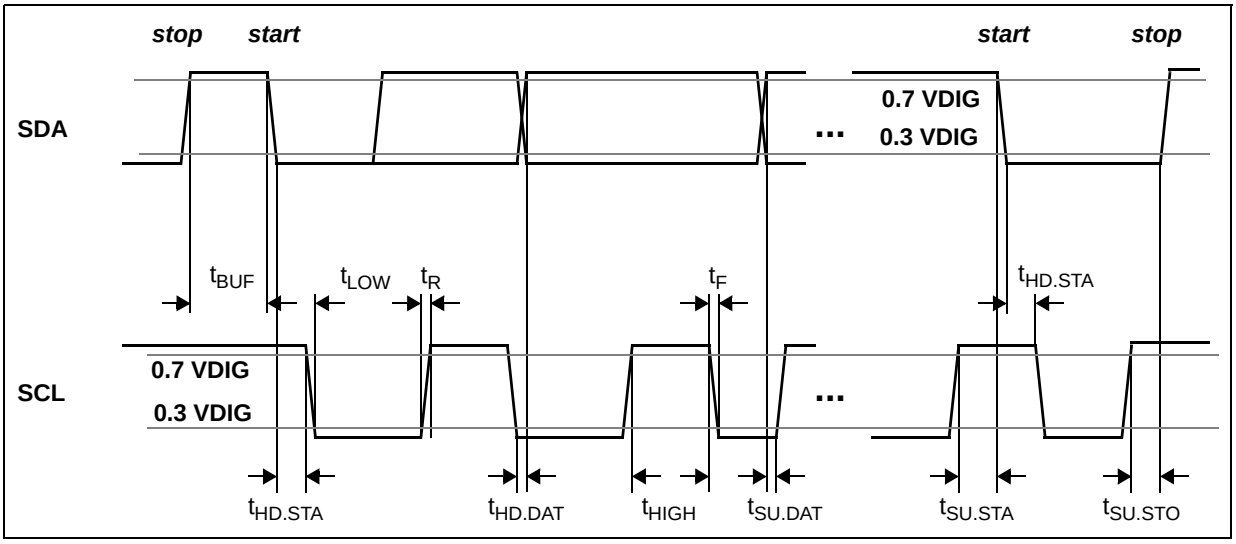
7.6.2 CCI interface - timing characteristics

Table 57. CCI interface - timing characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{SCL}	SCL clock frequency	0	-	400	kHz
t_{LOW}	Clock pulse width low	1.3	-	-	µs
t_{HIGH}	Clock pulse width high	0.6	-	-	µs
t_{SP}	Pulse width of spikes which are suppressed by the input filter	0	-	50	ns
t_{BUF}	Bus free time between transmissions	1.3	-	-	µs
$t_{HD.STA}$	Start hold time	0.6	-	-	µs
$t_{SU.STA}$	Start set-up time	0.6	-	-	µs
$t_{HD.DAT}$	Data in hold time	0	-	0.9	µs
$t_{SU.DAT}$	Data in set-up time	100	-	-	ns
t_R	SCL/SDA rise time	20+0.1 Cb(1)	-	300	ns
t_F	SCL/SDA fall time	20+0.1 Cb(1)	-	300	ns
$t_{SU.STO}$	Stop set-up time	0.6	-	-	µs
Ci/o	Input / Output capacitance (SDA)	-	-	8	pF
Cin	Input capacitance (SCL)	-	-	6	pF

1. Cb = total capacitance of one bus line in pF

Figure 27. CCI AC characteristics



All timings are measured from either 0.3 VDIG or 0.7 VDIG. For further information on the CCI interface please refer to the specification document: SMIA 1.0 part 2: CCP Specification.

7.7 CCP interface

7.7.1 CCP interface - DC specifications

Table 58. CCP interface - DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OD}	Differential voltage swing(1)	100	150	200	mV
V_{CM}	Common mode voltage (self biasing)	0.8	0.9	1.0	V
R_O	Output Impedance	40		140	Ω
I_{DR}	Drive current range (internally set by bias circuit)	0.5	1.5	2	mA
PSRR(2)	0 - 100MHz	-	-	30	dB
	100 - 1000MHz	-	-	10	dB

1. Measured over a 100 Ω load
2. Nominal value for the interference at V_{CM} voltage through digital supply relative to the interference at digital supply over the 0-1 GHz operating range. PSRR = 20*log10 (V_{DIG} interference (peak-to-peak) / V_{CM} interference (peak-to-peak))

Note: For further information on the subLVDS refer to the following specification document: SMIA 1.0 Part 2: CCP2 Specification

7.7.2 CCP interface - timing characteristics

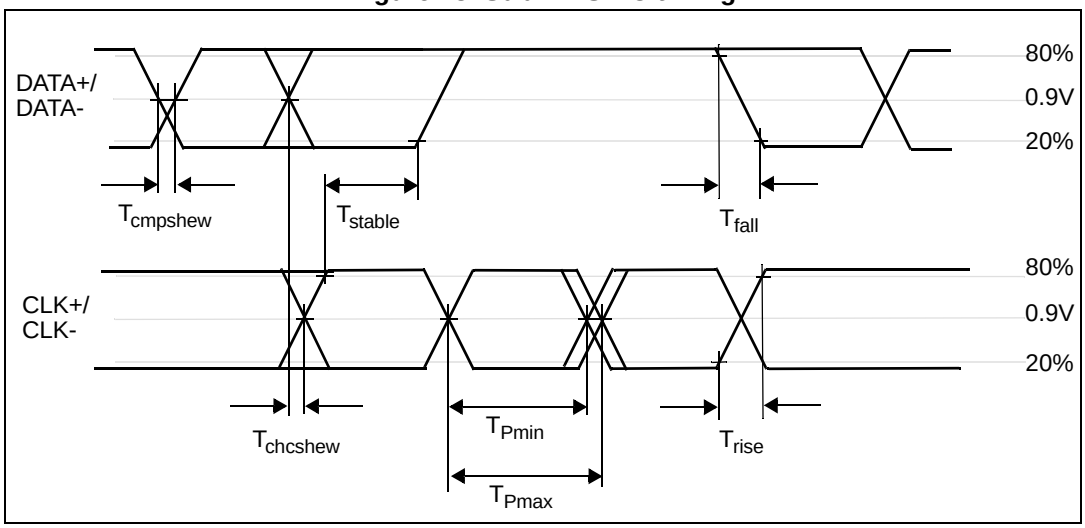
The parameters in *Table 59* are measured across a terminated 100Ω transmission line. CCP2_signalling_mode register is set to 1, data/strobe mode.

Table 59. CCP interface - timing characteristics

Symbol	Parameter	Min.	Max.	Unit
F_p	Average data frequency	-	640	Mbits/s
T_p	Average data period	1.56	-	ns
T_{jitter}(1)	Data period Jitter	-	200	ps
t_{stable}	Both data and clock at the stable level	780	-	ps
T_{rise}	Rise time of DATA+/DATA- ,CLK+/CLK-	300	400	ps
T_{fall}	Fall time of DATA+/DATA-, CLK+/CLK-	300	400	ps
T_{shew}(2)	Total skew between signals	-	225	ps
t_{PWR}	Power up/down time	-	20	µs

1. T_{Pmax}-T_{Pmin}
2. T_{shew} =$T_{cmpshew}$ + $T_{chcshew}$

Figure 28. SubLVDS AC timing



For further information on the CCP refer to the specification document: SMIA 1.0 Part 2: CCP2 Specification 30-6-04.

7.8 CSI-2 interface

7.8.1 CSI-2 interface - DC specifications

Table 60. CSI-2 interface - high speed mode - DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage(1)	140	200	270	mV
V_{OHHS}	HS output high voltage (1)			360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω

1. Value when driving into load impedance anywhere in the Z_{ID} range (80-125Ω).

Table 61. CSI-2 interface - low power mode - DC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	-50		50	mV
Z_{OLP}	Output impedance of LP transmitter	110			Ω

Note: When quoting the MIPI specification, the following rules must be followed:

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7.8.2 CSI-2 interface - AC specifications

Table 62. CSI-2 interface - high speed mode - AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Data rate	80	-	800	Mbits/s
t_{clkp}	Average data period	1.25		-	ns
t_r and t_f	20% - 80% rise time and fall time	150		0.3UI(1)	ps
t_{skew}	Data to Clock Skew	-0.15UI	-	0.15UI	ps

1. UI is equal to 1/(2*fh) where fh is the fundamental frequency of the transmission for a certain bit rate. e.g. for 600Mbps fh is 300MHz.

Table 63. CSI-2 interface - low power mode - AC specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_r and t_f	15% - 85% rise time and fall time			25	ns

For further information on the subLVDS refer to the specification document: MIPI Alliance Standard for D_PHY version 0.90.

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8 Optical specification

8.1 Lens characteristics

Table 64. Lens design characteristics for first source lens supplier

Parameter	Value					
4-element plastic lens	-					
F/number	2.8					
Effective focal length	3.26mm (primary wavelength 587.56 nm used)					
Horizontal FOV	57.8°					
Closest focusing distance	<300 mm with DAF					
Distortion	TV: -0.3 (typ)% Absolute: <|1.0%| across whole field (by design)					
Relative Illumination (lens only)	46% at 1.0 field.					
Maximum illumination decrease over 10% of image height. (lens only)	12%					
Spectral weighting: Wavlength (nm) Weight	656.28 151	587.56 318	546.07 312	486.13 157	435.84 49	404.66 13
Lateral chromatic aberration from blue (λ=435nm) to red (λ=656nm)	< |1.8 um|					
Coating reflectance - All surfaces are coated. At least 50% of all surfaces must fulfil this specification.	< 400nm 400 - 670nm >670nm		No limitation ≤ 1.0% absolute, 0.35% avg Straight line with a slope of < 3% / 100nm			
Maximum chief ray angle	28.2°					

Note: The module IR filter cut-off wavelength is 650 nm.

8.2 Text, 1D and 2D code reading

The VX6854LC camera module features a Supermacro mode dedicated to business card and text reading as well as barcode and 2D QR code reading using a monochrome image.

Figure 29. Examples of barcode and QR code

Barcode

QR code

Table 65: QR code (2D) resolution reading capability

Performances	Working distances (cm)
QR code 0.339 mm	25-28cm
QR code 0.4 mm	20-30cm
QR code 0.5 mm	15-30cm
QR code 0.6 mm	15-30cm
QR code 0.7 mm	15-30cm

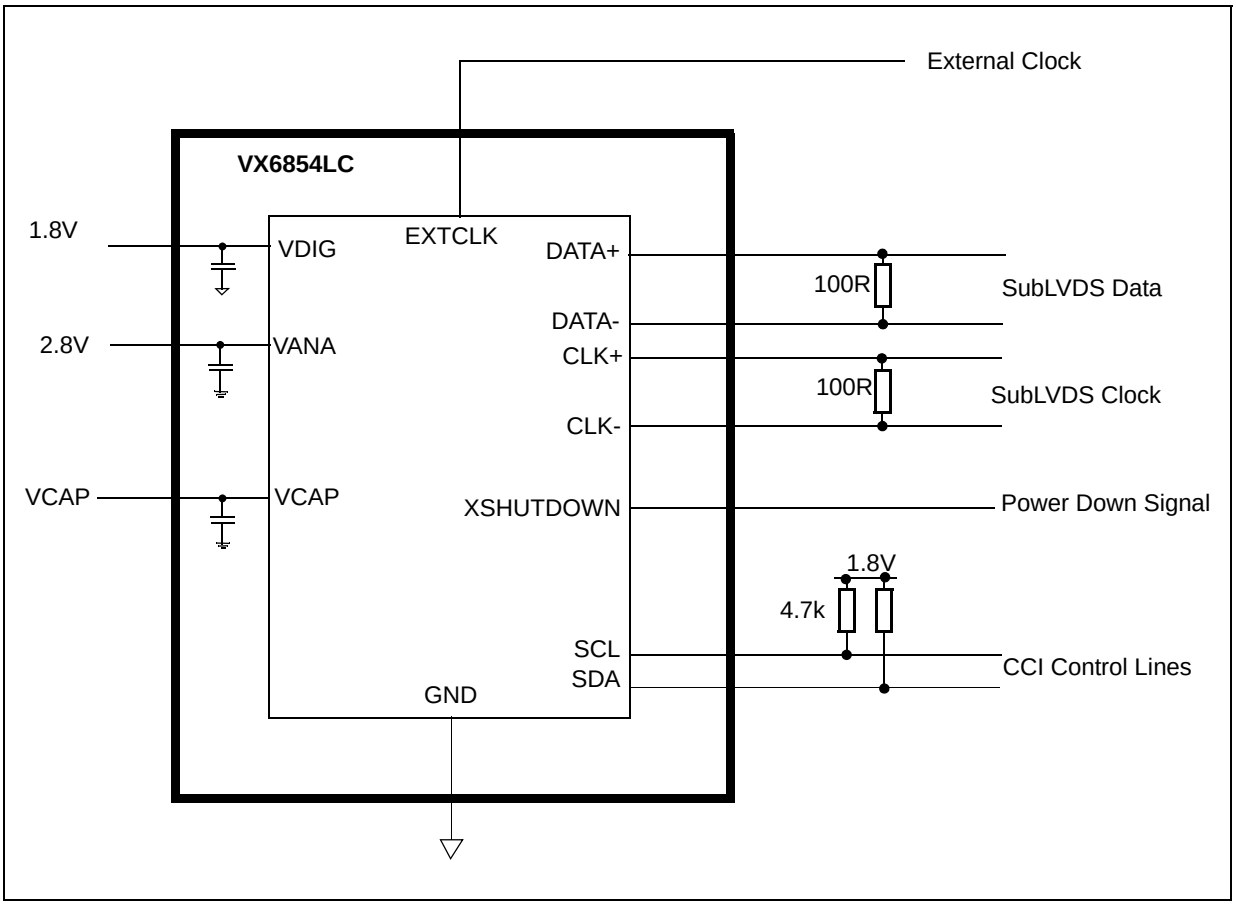
Note: The above performances were achieved on VX6854LC in Supermacro mode through ST's image processing pipe and with standard mobile phone application QR decoder software.

Refer to the "EDoF application note" for recommendations on Host processing pipe tuning for QR/Barcode reading.

9 Application

9.1 Schematic

Figure 30. Mobile camera application



1. CCP 100R termination may be internal to subLVDS receiver (for example, STV0986).
2. No external supply decoupling capacitors are required as the necessary components are integrated into the module.

9.2 Personality file

The personality file as specified in SMIA 1.0 Part 3.1:Software and application specification is detailed below:

```
smia_personality_file_id : 2.9
date : 2010-Oct-15
manufacturer_id : 1
model_id : 854
revision_number : Silicon Cut2.1

setting : register_override
Matrix optimisation 7Aug2009 (D65)

matrix_element_RedInRed =  1.934
matrix_element_GrnInRed = -0.586
matrix_element_BluInRed = -0.348

matrix_element_RedInGrn = -0.401
matrix_element_GrnInGrn =  1.582
matrix_element_BluInGrn = -0.181

matrix_element_RedInBlu = -0.052
matrix_element_GrnInBlu = -0.635
matrix_element_BluInBlu =  1.687

0x1122 = 0x0002    // max_vt_sys_clk_div
0x111C = 0x44480000 // max_pll_op_freq = 800MHz
0x1500 = 0x0400    // fifo_capability = 1023 pixels

setting : register_reprogram_once
// Require to load the following files:
// VX6854LC_Cut2_Patch06.txt - fixes the GPH, dark cal and HFPN
bugs. Also sets the analog MSRs.

0x0B06 = 0x00 // single_defect_correct = disable -> This enables the
RingCorrect
0x0B07 = 0x80 // single_defect_correct_weight = auto
0x0B08 = 0x01 // couplet_correct = enable
0x0B09 = 0x4F   // couplet_correct_weight
0x0b83 = 0x00    // EDOF Sharpness
0x0b84 = 0x20    // EDOF Denoising
0x0b85 = 0x20    // EDOF Noise vs. details
0x0B88 = 0x8000  // edof_focus_distance = automatic from preview

0x317E = 0x11   // IQ av_r2_shift
0x317F = 0x09   // IQ av_slant_shift

//Additional settings if Binning disabled
N/A

//Additional settings for Binning 2x2
0x0383 = 0x03   // X-Odd Inc
```

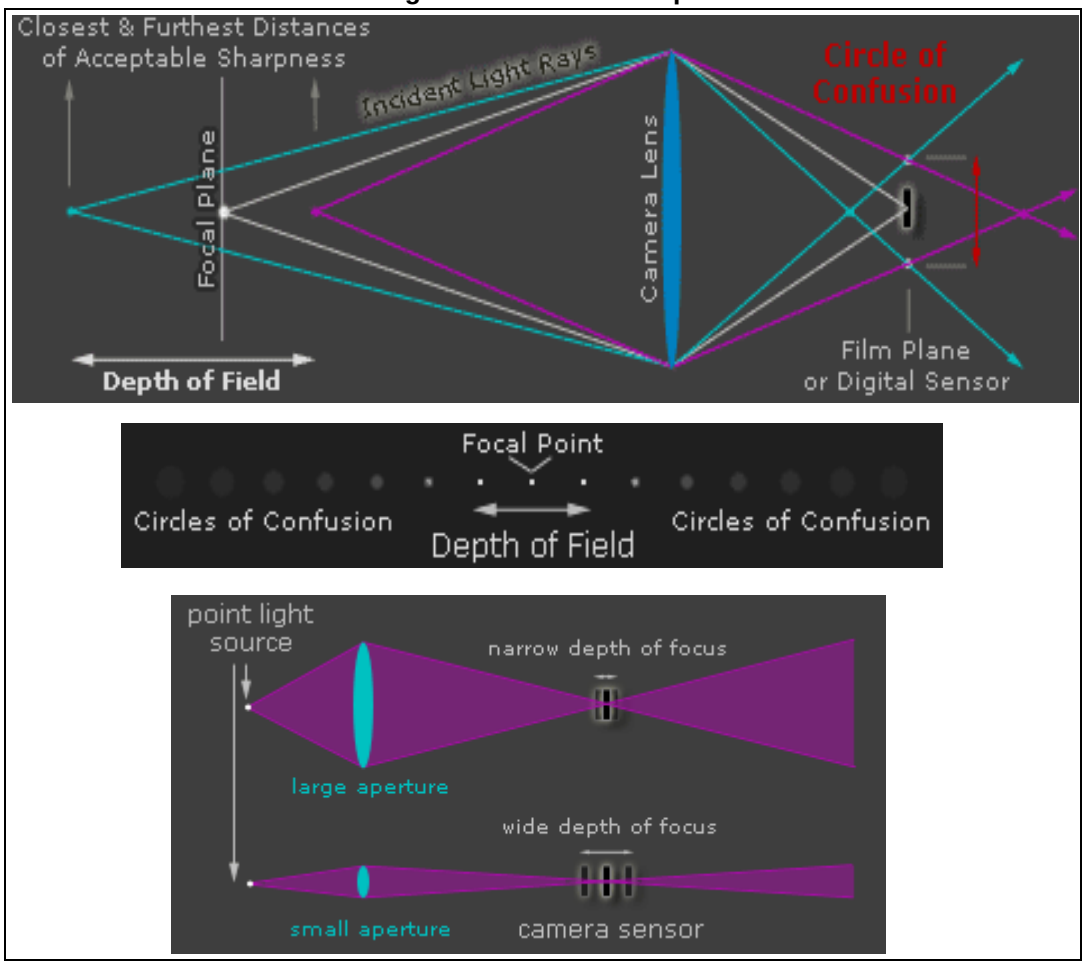
```
0x0387 = 0x03 // Y-Odd Inc
0x0900 = 0x01 // Enable Binning Mode
0x0901 = 0x22 // Binning Type
0x0902 = 0x04 // Binning Weighting
0x1716 = 0x0197// fine_integration_time_min_bin
0x1718 = 0x080F// fine_integration_time_max_margin_bin
//
// set Ext clk freq (default =6MHz)
0x0136 0xXXXX    // NOTE This should be set before loading the patch

setting : register_reprogram_every
// The white balance gains must be written to the sensor every time
the white balance gains change.
//END
```

10 EDoF control

The VX6854LC module uses a fixed focused lens with optical aberrations that the EDoF reconstruction engine is designed to recover the resolution and increase the depth of field in the range of 20 cm to infinity. The focus is tuned for far distances > 2 m but for closer distances where a standard fixed focus camera would show a blur image, the EDoF correction is capable of significantly recovering the resolution.

Figure 31. What is sharp?



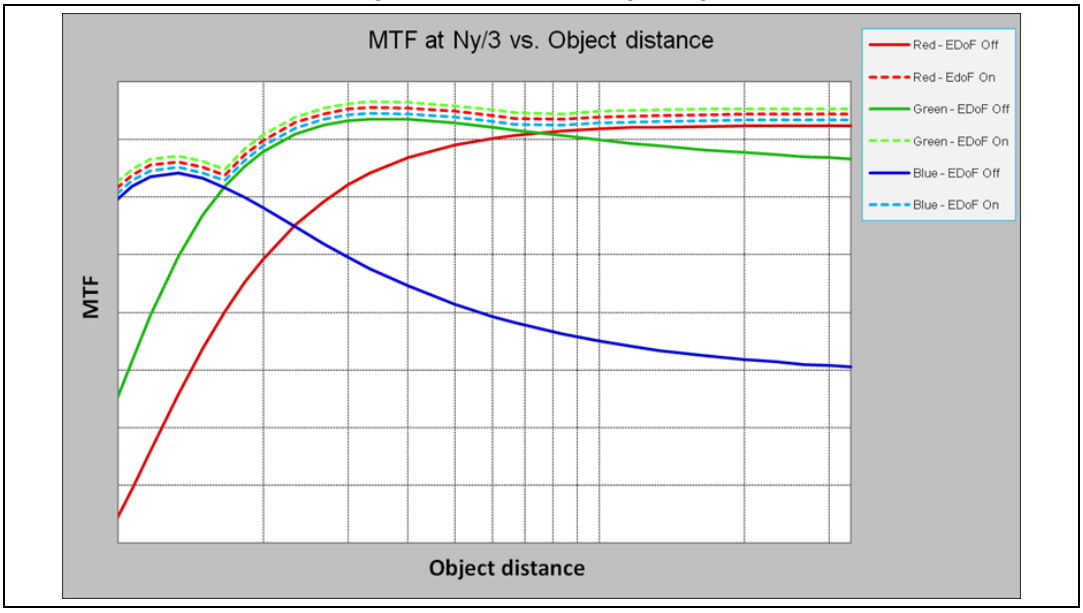
Facts about optics

- The depth of focus narrows with reduction in object distance or with aperture increase.
- If the lens is focussed at the hyper-focal distance, the sharpness will be the same from hyperfocal/2 to infinity.
- The depth of field is defined by the range of scene distances that appears acceptably sharp in the image.
- The size of a pixel (1.75 um) can be defined as a blurred spot. A blurred spot smaller than 1.75 um is registered as sharp. Above that value the spot will look blurred (refer to circle of confusion graph).

Considering the above points, EDoF aims to make the blur spot invariant (or change its reference) over a range of objects distances, thus defeating the obvious geometric optical effects to enhance the Depth of Field.

The plot below shows the EDoF main principle:

Figure 32. EDoF main principle



10.1 EDoF capabilities

The EDoF reconstruction engine is applied to the image after defect correction. It has denoising, sharpening, deconvolution algorithms among others that allow recovering the resolution.

It is advised that the end user does not use the EDoF IP as a sharpness block. EDoF has a depth of field recovery role. Oversharpening the image using EDoF before the HOST image processing might alter the final image quality.

The EDoF reconstruction engine can improve the depth of field for a colored image in the range of 30 cm to infinity and for a monochrome image below 30 cm.

The EDoF block works with ranges of distances in four modes for which the correction applied will be different:

- Super macro mode: < 30 cm
- Macro mode: 30 to 49 cm
- Portrait: 50 to 119 cm
- Landscape: 120 cm to infinity

The distance estimation analyzes gradients and relative sharpness among channels.

It first returns a measure of the sharpest channel in the image giving a macro “vote” when the sharpest channel is the blue one, portrait when it’s the green and landscape when it’s the red.

The relative sharpness among channel varies with the object distance but also in the field of the image (field curvature), so the votes are then weighted by calibration data in order to obtain the most appropriate mode or distance at the output.

Note: The aim of the distance estimation is not to obtain a precise distance but to select the best parameterization for the correction to be applied in capture, therefore the returned distance or specified distances range is indicative only.

Like an auto-focus module:

- The algorithm has failure cases, but the correction is constrained in order to always have acceptable image quality even if not optimal.
- For a single image several modes are often possible and giving same level of image quality.
  - For overlap distances (between macro and portrait modes, or between portrait and landscape modes), two of the channels may have the same level of sharpness, so any of the two corresponding distances could be returned, depending on scene content and field curvature of the module.
  - For scenes with objects at different distances, any of the three distances could be returned depending on content of the scene, field curvature of the module and spatial weights used for estimation (edof_estimation_control).

Supermacro mode is used for bar code and business card reading. Supermacro mode uses a monochrome image. Below 30 cm distance, the MTF is lost and there is too little green and red pixel information to build a colorized image. However, the blue pixel has enough MTF to reconstruct a monochrome image.

10.2 Control interface

The modules have a 100 kHz/400 kHz I^2C compatible 2-wire control interface. It uses the SMIA 16-bit index, 8-bit data message format. The CCI interfaces allows the programming of the EDoF control registers.

10.3 EDOF control registers [0x0B80 to 0x0B8A]

Table 66 lists the different registers that the end user can configure to tune the EDoF block.

Table 66. EDOF registers [0x0B80 to 0x0B8A]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B80		edof_mode	8UI	00	RW	EDOF control 0 - EDOF disabled (power saving) 1 - EDOF application (Capture) 2 - EDOF estimation (Preview)
0x0B82		edof_est_focus_distance	8UI	32	RO	The estimated focus point (cm)
0x0B83		edof_sharpness	8UI	00	RW	EDOF sharpness control 0 - 127: Manual mode
0x0B84		edof_denoising	8UI	00	RW	EDOF denoising control 0 - 127: Manual mode
0x0B85		edof_module_specific	8UI	00	RW	EDOF noise vs. details control 0 - 127: Manual mode
0x0B88	Hi	edof_focus_distance	16UI	00.32	RW	Value supplied by the host which is used by module for focus distance (in cm). 0x0000 to 0x7FFF - manual mode 0x8000 to 0xFFFF - auto mode
0x0B89	Lo					
0x0B8A		edof_estimation_control	8UI	00	RW	EDOF estimator control 0/1 - uniform 2 - centre weight 4 - large spot 8 - narrow spot

10.3.1 EDoF_Mode (0xB80)

The EDoF block can be disabled or enabled. The interest of disabling this block would be to save some power consumption. When enabling EDoF, two modes are available:

- **Estimation mode**

  This mode is dedicated to image preview (Viewfinder) only. EDoF correction is not being applied but statistics are gathered for distance estimation. Estimation mode can be full resolution or subsampled or binned image up to a maximum of x4 in both directions. If too much subsampling is performed the image out of the sensor becomes sharp and focus distance estimation is not possible.

- **Application mode**

  This is used for capture (or snapshot). The EDoF distance calculated during estimation is applied to the image. The application mode can only be enabled after the estimation mode has been selected, otherwise the EDoF correction will not be applied. EDoF cannot be applied to subsampled or binned images as it is not necessary to correct images when they are subsampled as the image blur introduced by the lens does not

need to be corrected when images are downscaled. No focus distance estimates are performed in application mode, even in multi-shot mode.

For preview mode, set the 0x0b80 register in estimation mode

```
0x0b80 = 0x02; // EDOF enabled for estimation mode
```

For capture mode, set the 0x0b80 register in application mode

```
0x0b80 = 0x01; // EDOF enabled for application mode
```

Note: Before enabling application mode, estimation mode has to be applied for a minimum of one frame so as to estimate the EDoF focus distance. This information is used in application mode when the image data is corrected. If estimation mode is not enabled prior to application mode, no correction will be applied to the snapshot image.

10.3.2 EDoF_est_focus_distance (0x0B82)

The edof_est_focus_distance register (0x0B82) is READ ONLY. This register tells the user the estimated focus point (cm) that the EDoF function has calculated.

10.3.3 EDoF tuning sliders (0xB83 to 0x0B85)

The three key registers for the end user tuning are the sharpness, denoising and noise versus detail registers.

- **edof_sharpness (0x0B83)**

  Value ranges from 0 to 127. The higher the value the more sharpening is applied. Higher values result in high contrasted edges being more sharpened but the noise level in uniform areas will not suffer.

Figure 33. Example images with different settings for sharpness slider

Sharpness=0x00 Sharpness=0x40 Sharpness=0x60

- **edof_denoising (0x0B84)**

  Value ranges from 0 to 127. The higher the value the stronger the denoising to be applied. Higher values results in reduced noise in uniform areas.

Figure 34. Example images with different settings for denoising slider

Denoising=0x00 Denoising=0x40 Denoising=0x60

- **edof_module_specific (noise vs. details) (0x0B85)**

  Value ranges from 0 to 127. Defines the weight of the sharpening versus the denoising weight. The higher the value the more weight is given to sharpness (that is, lower denoising weight). The lower the value, the more denoising weight is being applied. If sharpness (0x0B83) and denoising (0x0B84) registers are set to 0, then whatever this register value is, it will make no difference.

Figure 35. Example images with different settings for noise vs. details slider

NoiseVsDetails=0x00 NoiseVsDetails=0x40 NoiseVsDetails=0x60

Note: 1 Even with the above three registers values set to 0, a correction is being applied and will show a significant improvement versus no correction at all.

2 The tuning sliders do not operate in SuperMacro mode.

Recommended settings

For recommended settings for the EDoF sliders (0x0B83 to 0x0B85) refer to the relevant personality file.

10.3.4 EDoF focus distance (0x0B88)

For automatic mode, the value range is 0x8000 to 0xFFFF. Whatever value is selected within this range, automatic distance estimation will be enabled. ST recommend setting the EDoF estimation mode to automatic mode. In this mode, when the user selects application mode, the EDoF processing will automatically use the last estimate of the focus distance obtained in estimation mode.

For manual mode, the value to be set in the register is the value of the distance in cm. The range is 0x0000 to 0x7FFF. If you want to use one of the following modes, apply the following values:

- Super macro mode: 0 to 29 cm
- Macro mode: 30 to 49 cm
- Portrait: 50 to 119 cm
- Landscape: 120 to 32767 cm

Whatever value is selected within a particular range will produce the same result. For example, applying any value between 0 and 29 selects Super macro mode and produces the same result in the final image.

Super macro mode only works in manual mode. Refer to *Section 10.4: Super macro mode* for more detailed information.

Procedure to test distance estimation

Reference test scene: black and white chart (for example SFR chart or ISO12233), under D65 illuminant, minimal analog gain.

Ensure that the streaming frames are correctly exposed and that the white balance gains are written to the sensor.

Place the sensor at the minimum distance (that is, lower macro range distance) and then move the module gradually away from the scene

The estimated distance should change according to the distances quoted below:

- Macro mode: 30 cm
- Portrait: 50 cm
- Landscape: 120 cm

Note: 1 There is always an overlap between two consecutive modes, it might therefore be possible that the mode switch may not be exactly done at the given boundary.

2 The distances quoted above are given for D65, results may vary slightly for other illuminants. For instance, if the switch is 50 cm in Daylight, it is closer to 40 cm for tungsten illuminants.

3 It's not always possible to shoot charts at landscape distances. In this particular case, shoot an outdoor image with objects at infinity: the estimated distance should be landscape.

10.3.5 EDoF estimation control (0x0B8A)

This register selects the region of interest (ROI) on which to apply the distance estimation processing. Four different ROIs are available:

0 or 1: uniform

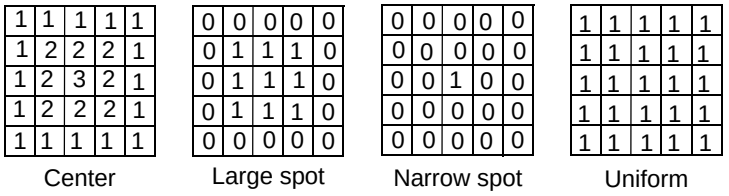
2: center-weighted

4: spot- large

8: spot narrow

Considering the above order, with increasing values, the estimation will increasingly focus on objects in the centre of the image. The processing time is identical for all cases.

Figure 36. Focus strategy weightings



The image is arranged as 5x5 regions for the weightings.

10.4 Super macro mode

Unlike the other modes (macro, portrait and landscape), super macro mode cannot be managed by the automated distance range estimator. The reason is that at distances below 30 cm, there is very little information in green and red channels though there is a significant energy in the blue channel. The distance estimator needs the four color channel information to estimate the distance. Below 30 cm, unless the distance is manually programmed using register 0x0B88, the EDoF correction will not be accurate.

For text or bar code reading, a monochromatic image can be used. EDoF super macro mode can be used for that purpose as the EDoF reconstruction engine would use the blue channel information to calculate the suitable sharpness and denoising.

To enable super macro mode, the user has to program manually the register 0x0B88 to set a value for distances below 30 cm. The register value being the value of the distance in cm.

It is important to note that as the super macro mode uses one color channel, the HOST has to consider using only the blue channel information to build a monochromatic image and the following features need to be disabled or restricted:

- lens shading correction: only apply blue channel correction
- disable white balance correction in the host: the white balance gains must still be calculated and written to the sensor
- no demosaicing
- disable any 4 channel gain dependant block in the HOST
- apply black and white matrix, rather than color matrix. (0 1 0, 0 1 0, 0 1 0)

10.5 EDoF and white balance

The EDoF reconstruction engine requires the white balance gains to be programmed by the HOST (by I^2C writes) to the color feedback register (0x0B8E to 0x0B95) of the sensor. These gains are also used for the sensor adaptive lens shading correction if enabled. The gains must be written to the sensor every time that the white balance gains change.

The white balance gains are required in both estimation and application modes.

The four HOST white balance gains to be programmed are listed in *Table 67*.

Table 67. Color feedback registers [0x0B8C - 0x0B95]

Index	Byte	Register name	Data type	Default	Type	Comment
0x0B8E	Hi	host_WB_stats_green_red	16UR	01.00	RW	White balance gains to be applied by the host. These are used by the EDOF and the adaptive AV to estimate the color temperature of the scene.
0x0B8F	Lo					
0x0B90	Hi	host_WB_stats_red	16UR	01.00	RW	
0x0B91	Lo					
0x0B92	Hi	host_WB_stats_blue	16UR	01.00	RW	
0x0B93	Lo					
0x0B94	Hi	host_WB_stats_green_blue	16UR	01.00	RW	
0x0B95	Lo					

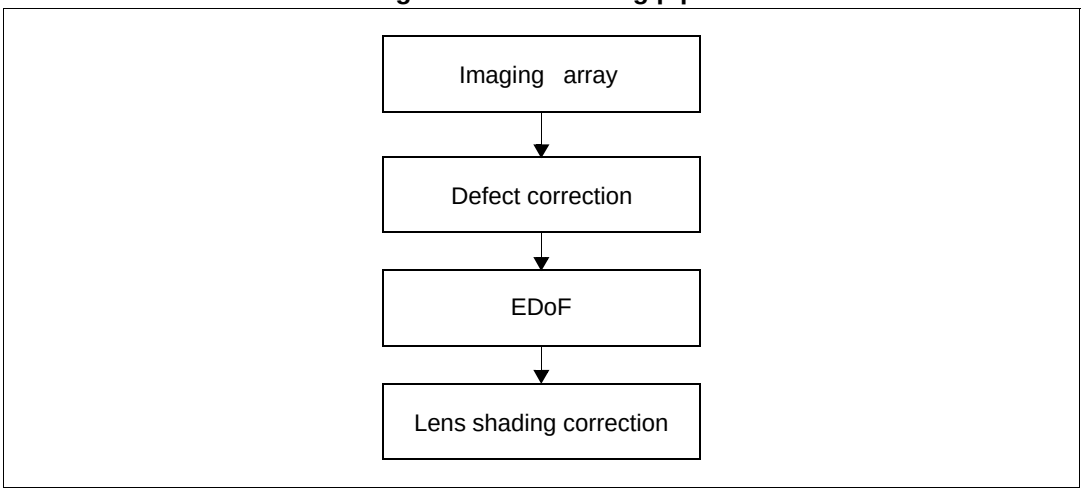
11 Image optimization

The sensor has the following image optimizations on the sensor:

- mapped couplet correction
- dynamic couplet and singlet correction
- lens shading correction

Figure 37 shows the processing pipe. Note that defect correction must be enabled as it occurs before the EDoF processing.

Figure 37. Processing pipe

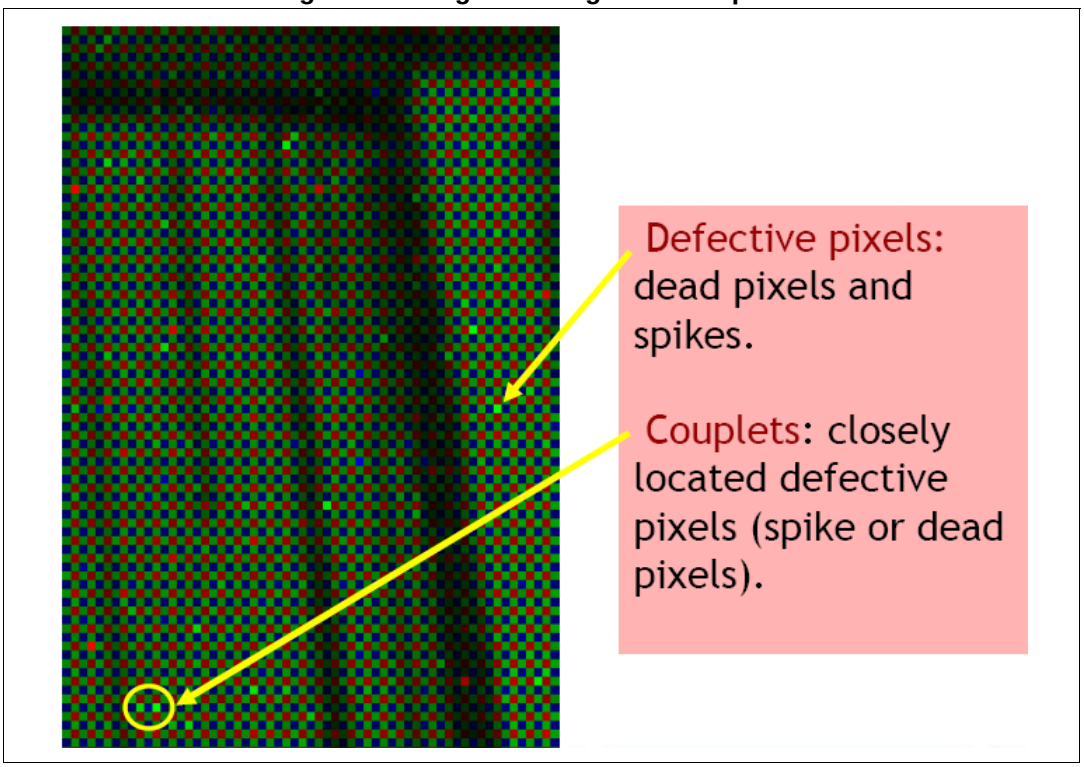


11.1 Defect correction

The defect correction algorithm dynamically detects and corrects single and couplet defective pixels in the imaging array. The weight of both correction filters can be adjusted. For recommended settings refer to the personality file.

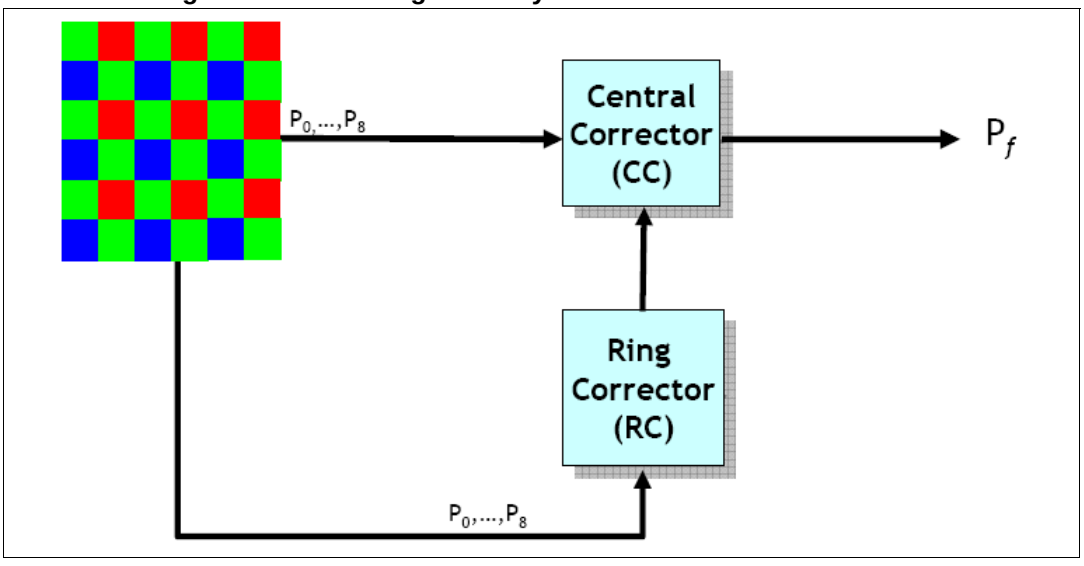
An image showing an example of defective pixels is shown in *Figure 38*.

Figure 38. Image showing defective pixels



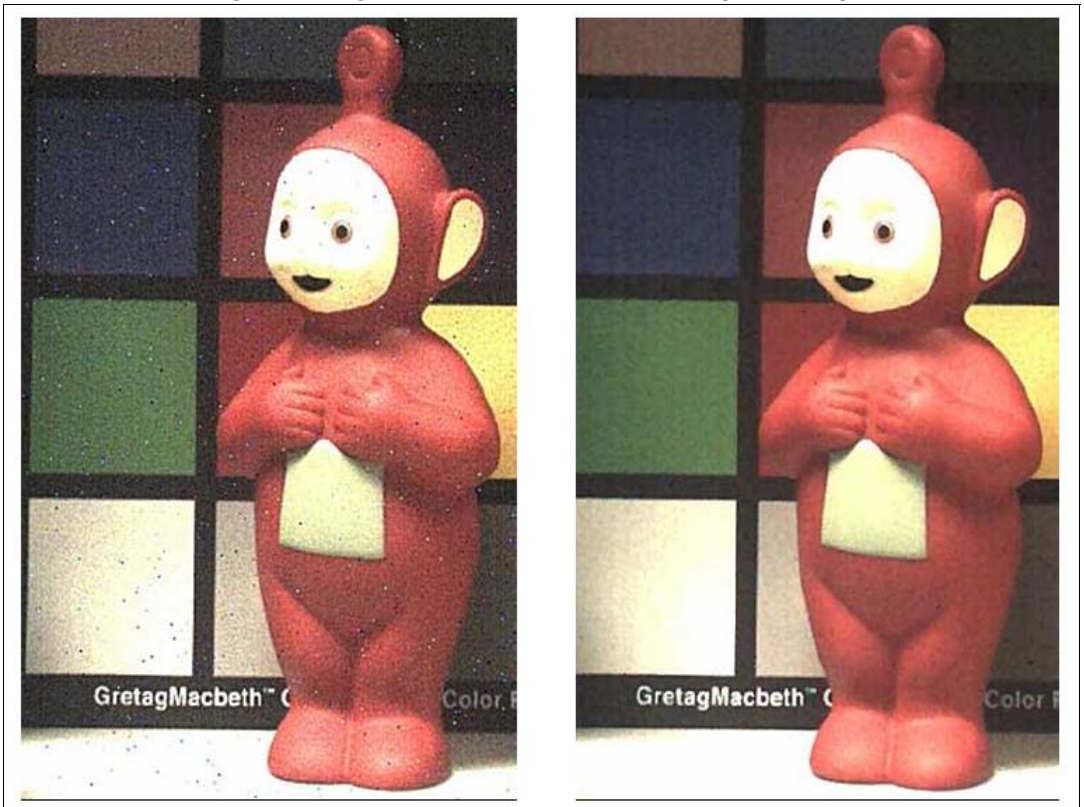
A simplified block diagram of the defective correction block is shown in *Figure 39*.

Figure 39. Block diagram of dynamic defect correction block



An example of an image before and after correction is shown in *Figure 40*.

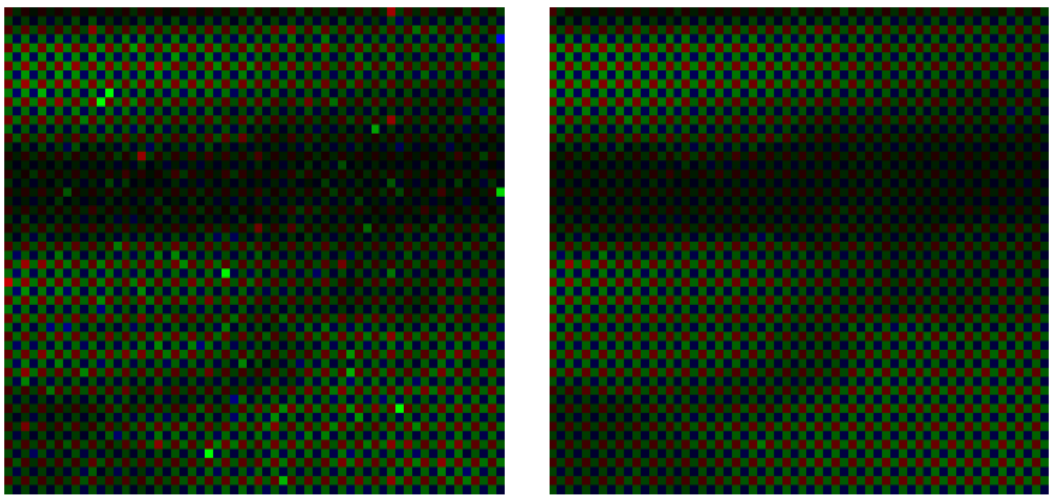
Figure 40. Dynamic defect correction output example



Original image Corrected image

An example of a corrected Bayer pattern is shown in *Figure 41*.

Figure 41. Corrected Bayer pattern



Colorized original Bayer Colorized corrected Bayer

11.2 Mapped couplet correction (Bruce)

The mapped couplet defect correction filter is designed to intelligently correct the first defect in a couplet thereby changing a couplet into a single pixel defect. Single pixel defects can then be corrected using the dynamic defect correction filter.

The mapped couplet correction filter requires exact coordinate information for each of the couplets to be repaired. The couplet coordinates are stored in non-volatile-memory (NVM) during production test. The mapped couplet correction filter does not operate in binning mode or in sub sample mode and is automatically disabled.

The mapped couplet correction is controlled by register 0x0B05:

0 - Disable

1 - Enable

11.3 Lens shading correction

The sensor has an adaptive (four color temperature) lens shading correction function which can be used to reduce the effect of roll off in the optical system. Correction is carried out individually for all four color planes, each gain is calculated based on the distance from the image centre to the pixel in question using a two factor polynomial (R2 and R4).

In order to optimize the adaptive lens shading algorithm, the coefficients for each device are calculated under D65 lighting conditions and programmed in the NVM memory at production test.

Settings for three other color temperatures (Cool White, U30, and Horizon) are calculated from characterization data and these are stored in the NVM memory. The calculation of the color temperature is performed by the sensor using the color feedback registers. Therefore it is necessary for the host to supply the sensor with the white balance gains.

The lens shading function can be used with the profile1 and profile 2 scaler and with crop and sub-sampling.

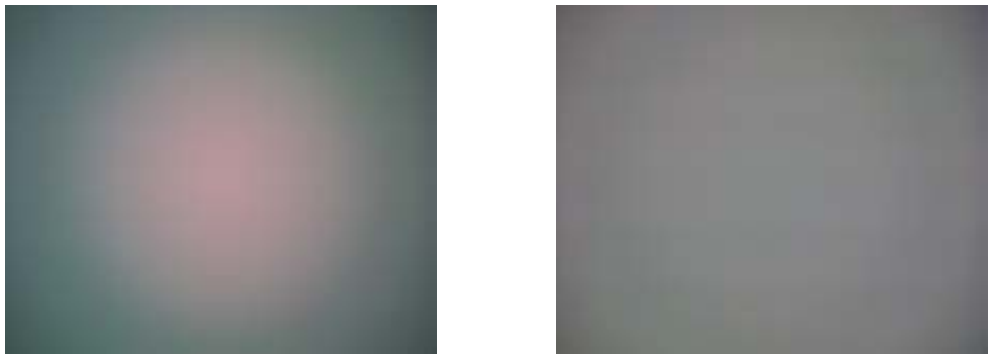
The lens shading correction is controlled by register 0x0B00:

0 - Disable

1 - Enable

The correction applied is 75%.

Figure 42. Lens shading images



Original image Corrected image

12 NVM contents

The sensor has the following contents in the NVM:

- revision and traceability data
- defect data (used on-chip, described in *Section 11.2*)
- lens shading 4 channel radial corrector data (used on-chip, described in *Section 11.3*)
- sensitivity data (to be used by the host)

12.1 Sensitivity data

This data is not used by the sensor but can be used by the host to calibrate the AWB system.

The sensitivity data is measured at FMT for each device for one color temperature D65 (Fluorescent Phillips Graphica Pro 965). Each of the four color channel values are recorded. The 10-bit average of the central 10% of the image (10% of image width, 10% of image height) is recorded, the pedestal is included in the value. The on board lens shading correction is disabled. The analog gain is set to x1.

12.2 NVM map

The sensor must be in software standby to read the NVM.

In order to read the NVM the following registers must be programmed.

0x3E04 = 1 - Power-up the NVM

0x3640 = 0 - Access NVM register space

The registers should be reset after reading the NVM to the following:

0x3E04 = 0 - Power-down the NVM

0x3640 = 1 - Disable access to NVM register space

Table 68. NVM map

Index	Data transfer page & page value	Segment	Bit number								Comments
			7	6	5	4	3	2	1	0	
0xFC00	0,0		0x00								Not used
0xFC01	0,1		0x00								
0xFC02	0,2		0x00								
0xFC03	0,3		0x00								

Table 68. NVM map (continued)

Index	Data transfer page & page value	Segment	Bit number 7	6	5	4	3	2	1	0	Comments
0xFC04	0,4	ST Payload - Module Data	0x03								Module Model ID: 0x0356 (854d)
0xFC05	0,5		0x56								
0xFC06	0,6		ModuleRevMajor[7:0]								00: Unprogrammed 01: ES1.0 02: ES2.0
0xFC07	0,7		00								ModuleRevMinor
0xFC08	0,8		01								ModuleManufID (ST)
0xFC09	0,9		Year				Month				
0xFC0A	0,10		Day				ModuleDatePhase				ModuleDatePhase[2:0] 00: TS 01: ES 02: CS 03: MP
0xFC0B	0,11		SerialNumber[31:24]								Serial numbering, [31:24]: tester code [23:0]: seconds since midnight
0xFC0C	0,12		SerialNumber[23:16]								
0xFC0D	0,13		SerialNumber[15:8]								
0xFC0E	0,14		SerialNumber[7:0]								
0xFC0F	0,15		0	0	0	0	00				SensorRevNo[3:0]
0xFC10	0,16	ST Payload - Defect correction	DefectCount[15:8]								Number of defects
0xFC11	0,17		DefectCount[7:0]								
0xFC12	0,18		CoupletXCoord[11:4]								Coordinates of first defect
0xFC13	0,19		CoupletXCoord[3:0]				0	CoupletYCoord[10:8]			
0xFC14	0,20		CoupletYCoord[7:0]								
			Variable amount of bytes depending on the number of defects programmed.								
		Gap	Gap so that AV data starts on a word boundary. This is programmable depending on the number of couplets stored.								

Table 68. NVM map (continued)

Index	Data transfer page & page value	Segment	Bit number								Comments
			7	6	5	4	3	2	1	0	
AV_Start_Addr		ST Payload - Adaptive AV coefficients for Cast3 (D65)	AV_R^2_Red_Cast3[7:0]								
AV_Start_Addr+1			AV_R^2_GreenRed_Cast3[7:0]								
AV_Start_Addr+2			AV_R^2_GreenBlue_Cast3[7:0]								
AV_Start_Addr+3			AV_R^2_Blue_Cast3[7:0]								
AV_Start_Addr+4			AV_R^4_Red_Cast3[7:0]								
AV_Start_Addr+5			AV_R^4_GreenRed_Cast3[7:0]								
AV_Start_Addr+6			AV_R^4_GreenBlue_Cast3[7:0]								
AV_Start_Addr+7			AV_R^4_Blue_Cast3[7:0]								
AV_Start_Addr+8			AV_Horiz_Slant_Coeff_Red_Cast3[7:0]								
AV_Start_Addr+9			AV_Horiz_Slant_Coeff_GreenRed_Cast3[7:0]								
AV_Start_Addr+10			AV_Horiz_Slant_Coeff_GreenBlue_Cast3[7:0]								
AV_Start_Addr+11			AV_Horiz_Slant_Coeff_Blue_Cast3[7:0]								
AV_Start_Addr+12			AV_Ver_Slant_Coeff_Red_Cast3[7:0]								
AV_Start_Addr+13			AV_Ver_Slant_Coeff_GreenRed_Cast3[7:0]								
AV_Start_Addr+14			AV_Ver_Slant_Coeff_GreenBlue_Cast3[7:0]								
AV_Start_Addr+15			AV_Ver_Slant_Coeff_Blue_Cast3[7:0]								
AV_Start_Addr+16			AV_DC_Coeff_Red_Cast3[7:0]								
AV_Start_Addr+17			AV_DC_Coeff_GreenRed_Cast3[7:0]								
AV_Start_Addr+18			AV_DC_Coeff_GreenBlue_Cast3[7:0]								
AV_Start_Addr+19			AV_DC_Coeff_Blue_Cast3[7:0]								

Table 68. NVM map (continued)

Index	Data transfer page & page value	Segment	Bit number								Comments
			7	6	5	4	3	2	1	0	
AV_Start_Addr+20		ST Payload - Adaptive AV coefficients for Cast2	AV_R^2_Red_Cast2[7:0]								
AV_Start_Addr+21			AV_R^2_GreenRed_Cast2[7:0]								
AV_Start_Addr+22			AV_R^2_GreenBlue_Cast2[7:0]								
AV_Start_Addr+23			AV_R^2_Blue_Cast2[7:0]								
AV_Start_Addr+24			AV_R^4_Red_Cast2[7:0]								
AV_Start_Addr+25			AV_R^4_GreenRed_Cast2[7:0]								
AV_Start_Addr+26			AV_R^4_GreenBlue_Cast2[7:0]								
AV_Start_Addr+27			AV_R^4_Blue_Cast2[7:0]								
AV_Start_Addr+28		ST Payload - Adaptive AV coefficients for Cast1	AV_R^2_Red_Cast1[7:0]								
AV_Start_Addr+29			AV_R^2_GreenRed_Cast1[7:0]								
AV_Start_Addr+30			AV_R^2_GreenBlue_Cast1[7:0]								
AV_Start_Addr+31			AV_R^2_Blue_Cast1[7:0]								
AV_Start_Addr+32			AV_R^4_Red_Cast1[7:0]								
AV_Start_Addr+33			AV_R^4_GreenRed_Cast1[7:0]								
AV_Start_Addr+34			AV_R^4_GreenBlue_Cast1[7:0]								
AV_Start_Addr+35			AV_R^4_Blue_Cast1[7:0]								

Table 68. NVM map (continued)

Index	Data transfer page & page value	Segment	Bit number								Comments
			7	6	5	4	3	2	1	0	
AV_Start_Addr+36		ST Payload - Adaptive AV coefficients for Cast0	AV_R^2_Red_Cast0[7:0]								
AV_Start_Addr+37			AV_R^2_GreenRed_Cast0[7:0]								
AV_Start_Addr+38			AV_R^2_GreenBlue_Cast0[7:0]								
AV_Start_Addr+39			AV_R^2_Blue_Cast0[7:0]								
AV_Start_Addr+40			AV_R^4_Red_Cast0[7:0]								
AV_Start_Addr+41			AV_R^4_GreenRed_Cast0[7:0]								
AV_Start_Addr+42			AV_R^4_GreenBlue_Cast0[7:0]								
AV_Start_Addr+43			AV_R^4_Blue_Cast0[7:0]								
AV_Start_Addr+44		ST Payload - Adaptive AV nRed Gain Casts	Normalised_Red_Gain_Cast3[15:8]								
AV_Start_Addr+45			Normalised_Red_Gain_Cast3[7:0]								
AV_Start_Addr+46			Normalised_Red_Gain_Cast2[15:8]								
AV_Start_Addr+47			Normalised_Red_Gain_Cast2[7:0]								
AV_Start_Addr+48			Normalised_Red_Gain_Cast1[15:8]								
AV_Start_Addr+49			Normalised_Red_Gain_Cast1[7:0]								
AV_Start_Addr+50			Normalised_Red_Gain_Cast0[15:8]								
AV_Start_Addr+51			Normalised_Red_Gain_Cast0[7:0]								

Table 68. NVM map (continued)

Index	Data transfer page & page value	Segment	Bit number								Comments
			7	6	5	4	3	2	1	0	
0xFDF4	7,52								Sensitivity_Red[9:8]		The measured light level is recorded per Bayer Color channel for diffuse D65 illumination, AV off, ROI = central 10% of image height and width, including pedestal. These values can be used as input into the ISP AWB algorithm to normalise the sensor response to match that of the 'golden' sensor used to set-up the AWB tilts. Not used by VX6854LC
0xFDF5	7,53		Sensitivity_Red[7:0]								
0xFDF6	7,54								Sensitivity_GreenRed[9:8]		
0xFDF7	7,55		Sensitivity_GreenRed[7:0]								
0xFDF8	7,56								Sensitivity_GreenBlue[9:8]		
0xFDF9	7,57		Sensitivity_GreenBlue[7:0]								
0xFDFA	7,58								Sensitivity_Blue[9:8]		
0xFDFB	7,59		Sensitivity_Blue[7:0]								
0xFDFC	7,60		MapVersion[7:0]								
0xFDFD	7,61		TestProgramRevMaj[7:0]								
0xFDFE	7,62		TestProgramRevMin[7:0]								
0xFDFF	7,63										

13 Defect categorization

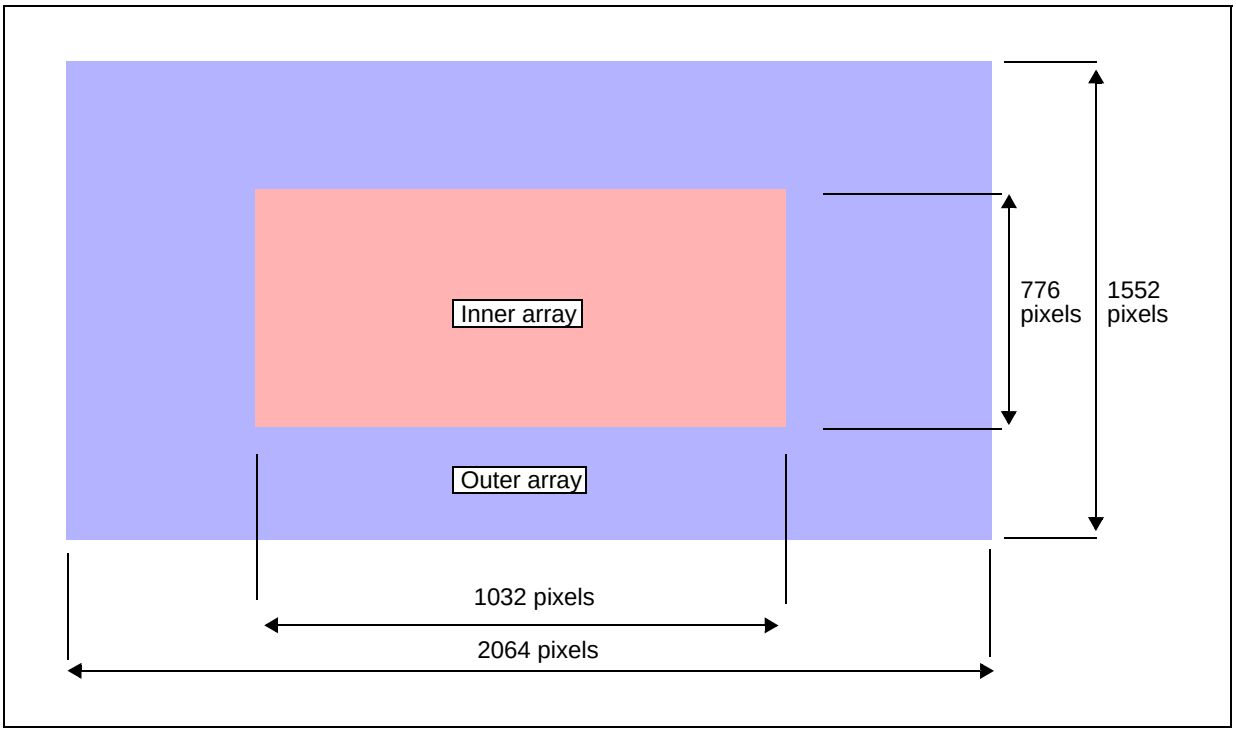
13.1 Pixel defects

Illuminated defects are tested with a flat field illumination and a pass-fail criteria that is a percentage deviation from a local mean. In order that the sensor can be effectively tested in a reasonable test time, it is necessary to put the limits of gain error above the normal noise distribution of photon shot noise and sensor noise otherwise false single pixel fails will be detected. A typical defect criteria for single-pixel gain errors is ± 9%. In fact, any element in the array outside ±9% is a “minor” fail, and outside of ± 25% is a “major” fail. Note that the defect detection method is applied to raw bayer images.

13.2 Sensor array area definition

For specific aspects of pixel defect testing the image sensor array is subdivided into two regions as illustrated in *Figure 43*.

Figure 43. VX6854LC pixel defect test area



The inner array in *Figure 43* is centre justified, in the x and y axis, with respect to the outer array. The inner array is 50% of the full width and 50% of the full height of the larger outer array, therefore the inner array is one quarter of the area of the outer array.

13.3 Pixel fault numbering convention

The pixel notation is described in *Figure 44*. For the purposes of the test the 3x3 array describes nine bayer pixels of a common color, that is, **all the pixels will either be Red, Green (the Green pixels are split over 2 common channels, Green1 and Green2) or Blue.** The pixel under test is **X**. If a pixel under test is on the edge, the array is reduce to its existing neighbor pixels (that is, the first pixel uses only a 2x2 array).

Figure 44. Pixel numbering notation

[0]	[1]	[2]
[7]	X	[3]
[6]	[5]	[4]

13.4 Single pixel faults

STMicroelectronics defines a single pixel fail as a failing pixel with no adjacent failing same color neighbours. A single pixel fail can be a stuck at white where the output of the pixel is permanently saturated regardless of the level of incident light and exposure level, a stuck at black where the pixel output is zero regardless of the level of incident light and exposure level (major fail) or simply a pixel that differs from it's immediate neighbours by more than the test threshold (minor fail).

The example in *Figure 45* assumes that pixel **X** is a fail. For this pixel to be a single pixel fail the pixels at positions [0],[1],[2],[3],[4],[5],[6] and [7] must be "good" pixels that pass final test. The implemented test program will pass a sensor with up to the defined limit of single pixel faults per color channel. Defect correction algorithms will correct the pixel faults in the final image.

Figure 45. Single pixel fault

[0]	[1]	[2]
[7]	X	[3]
[6]	[5]	[4]

13.5 Couplet definition

A failing pixel at **X** with a failing pixel at position [0], [1], [2], [3], [4], [5], [6] or [7] such that there is a maximum of two failing pixels from the group of nine pixels illustrated in *Figure 46*. The example shown in *Figure 46* has the centre pixel and the pixel at position [7] failing the test criteria.

Figure 46. General couplet example

[0]	[1]	[2]
[**X**]	X	[3]
[6]	[5]	[4]

The basic couplet definition is further subdivided into minor and major couplets. With respect to the example in *Figure 46*, a minor couplet is defined as a defect pixel pair where one pixel can be an extreme fail, that is a stuck at black or stuck at white, but the second pixel in the pair must differ from the local pixel average by less than 25% of that average value. If the second pixel in the couplet differs by more than 25% of the local pixel average value then this would be defined as a major couplet.

In addition, couplets will be classified as being in the inner or outer area.

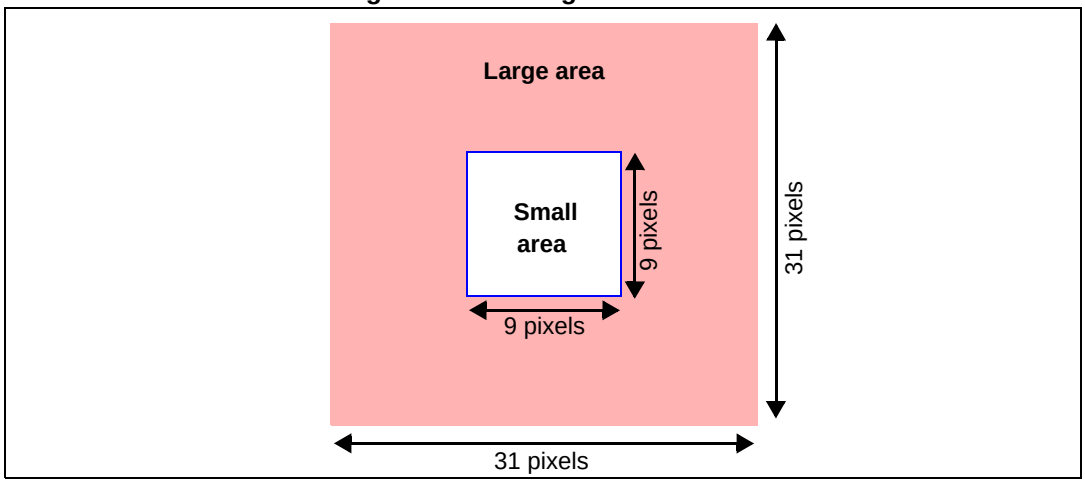
13.6 Physical aberrations

A specific test algorithm is also applied in production to identify and reject samples that display defocused artefacts often referred to as blemishes or shapes. These artefacts are caused by scratches or contamination in the optical path away from the focal plane for example, on the IR glass or lens.

The test requires two regions to be defined:

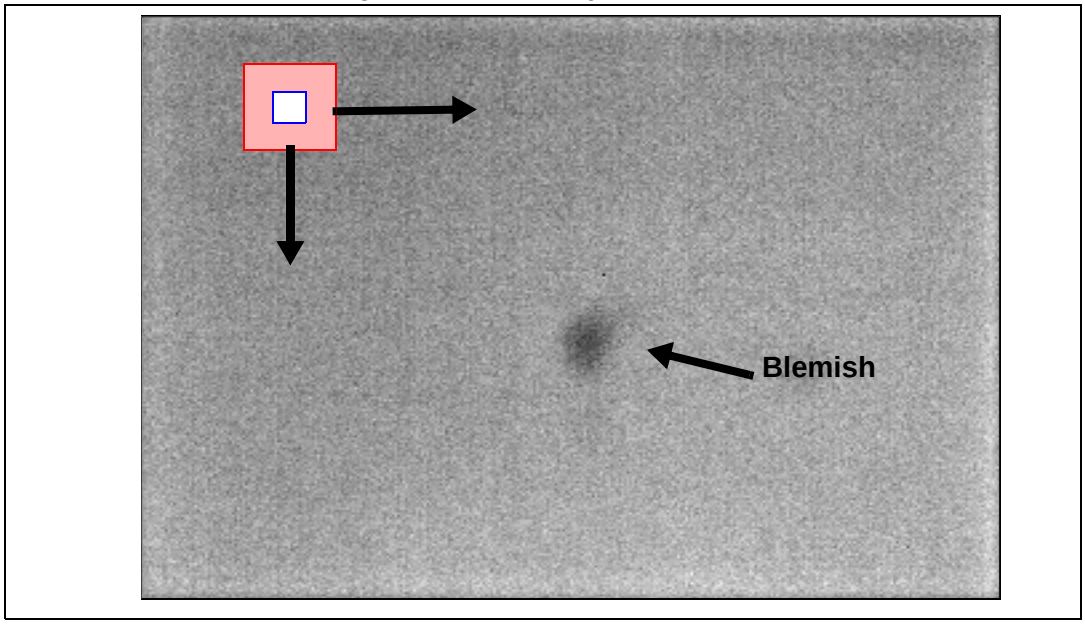
- a small area: 9 by 9 pixels with the pixel under test at the centre of this area (shaded blue in *Figure 47*)
- a large region, 31 by 31 pixels (shaded red in *Figure 47*)

Figure 47. Test region definition



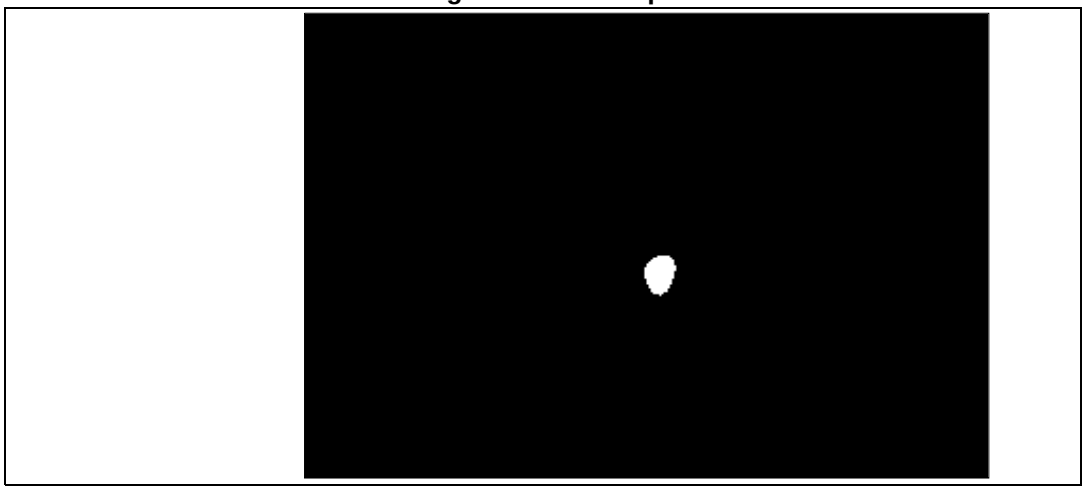
An average value is calculated for both the “small” and “large” areas. The areas are then scanned across each color channel separately.

Figure 48. Scan array for blemish



The next stage of the test is the creation of a pixel map for each color channel with the coordinates of the failing pixels. See *Figure 49*.

Figure 49. Fail map



A pixel location is identified as a fail in the map if it satisfies the following criteria:

Small_average < Large_average - (1.2% of Large_average)

or

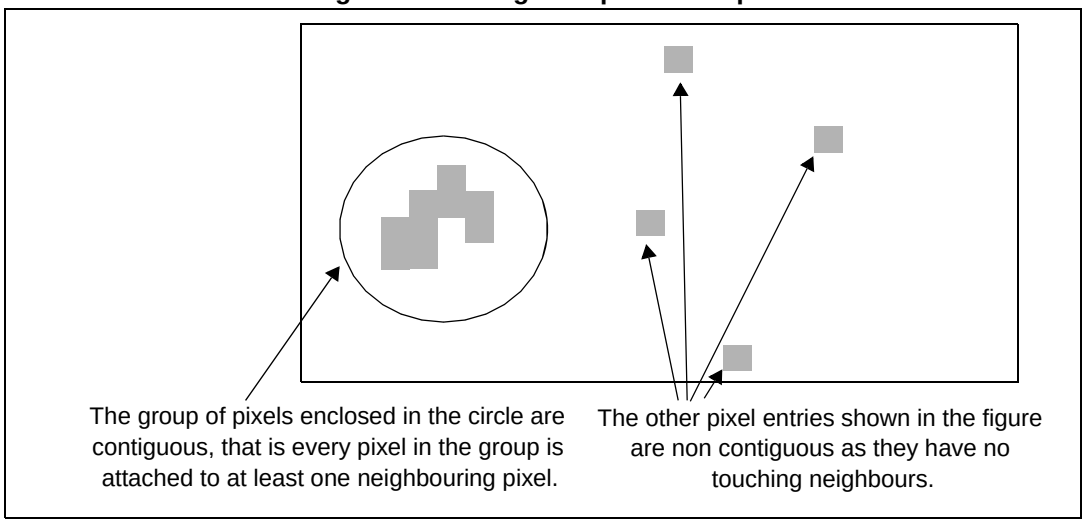
Small_average > Large_average + (1.2% of Large_average)

The contents of the fail map determine whether the sensor fails the physical aberration test. The module fail criteria is:

Pass if: <= 82 contiguous pixel entries in the failure map for each color channel.

An example of contiguous pixels entries is given in *Figure 50*.

Figure 50. Contiguous pixel example



14 Mechanical

Figure 51. VX6854LC outline drawing - sheet 1 of 3

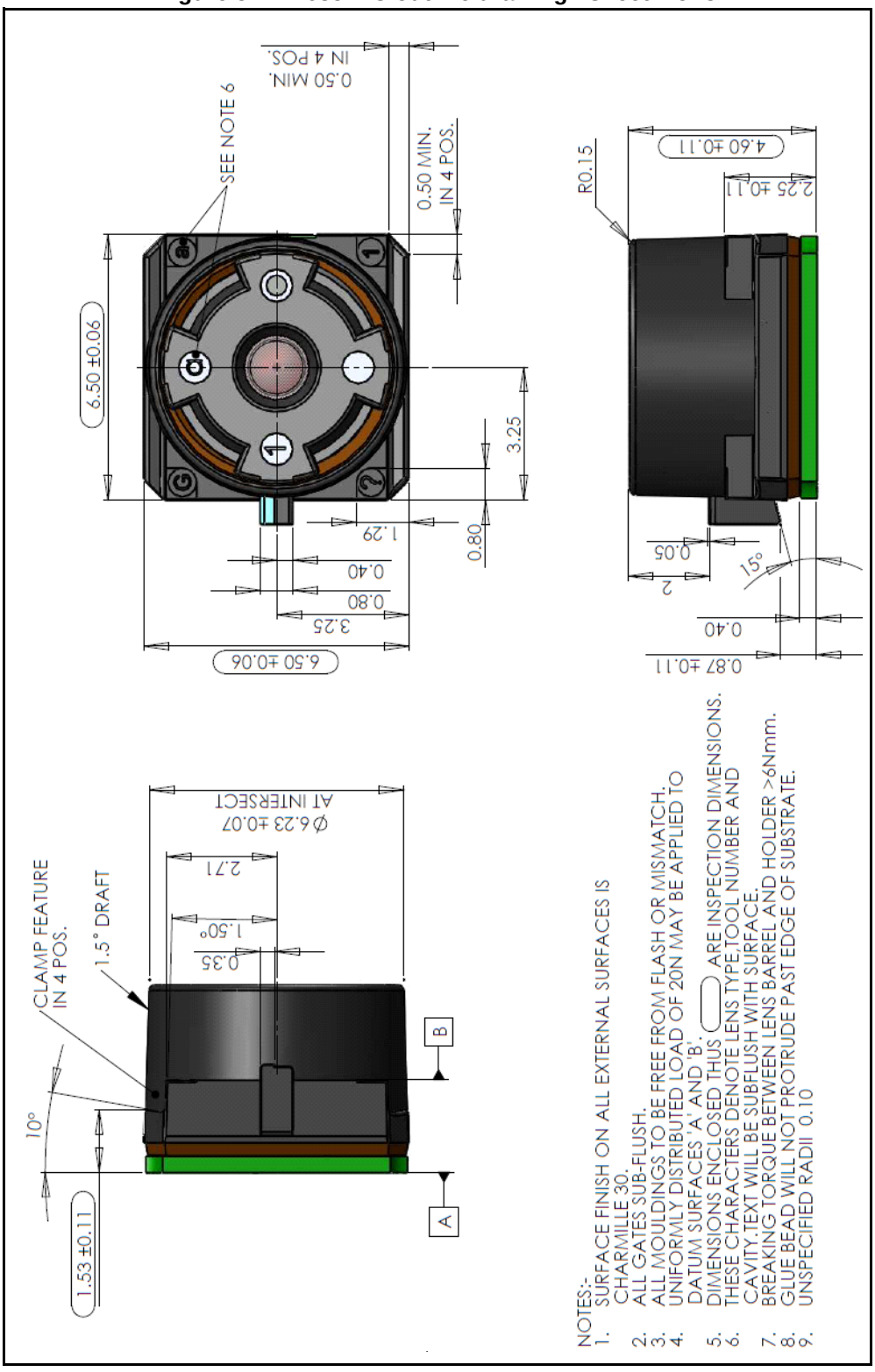
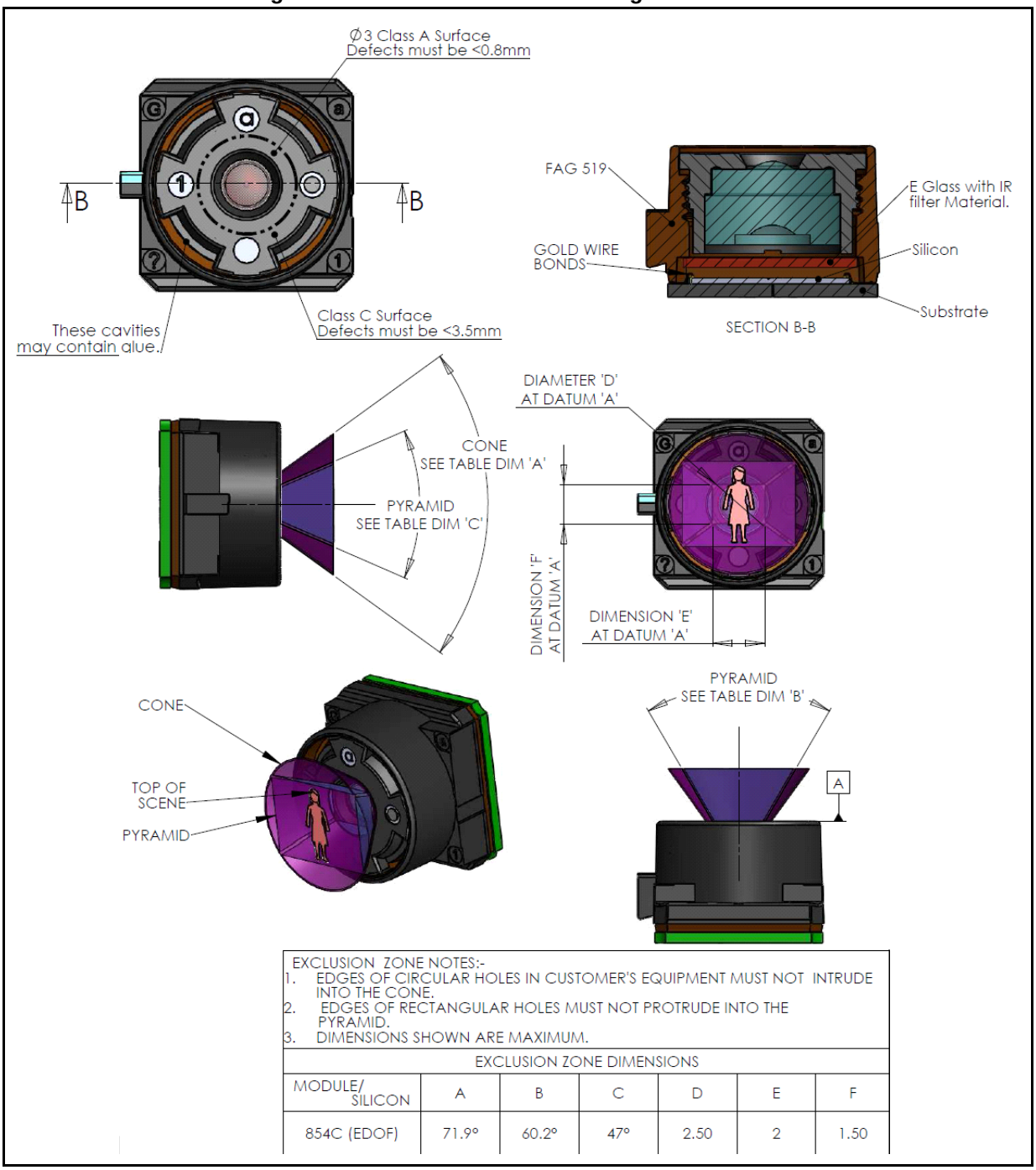


Figure 52. VX6854LC outline drawing - sheet 2 of 3

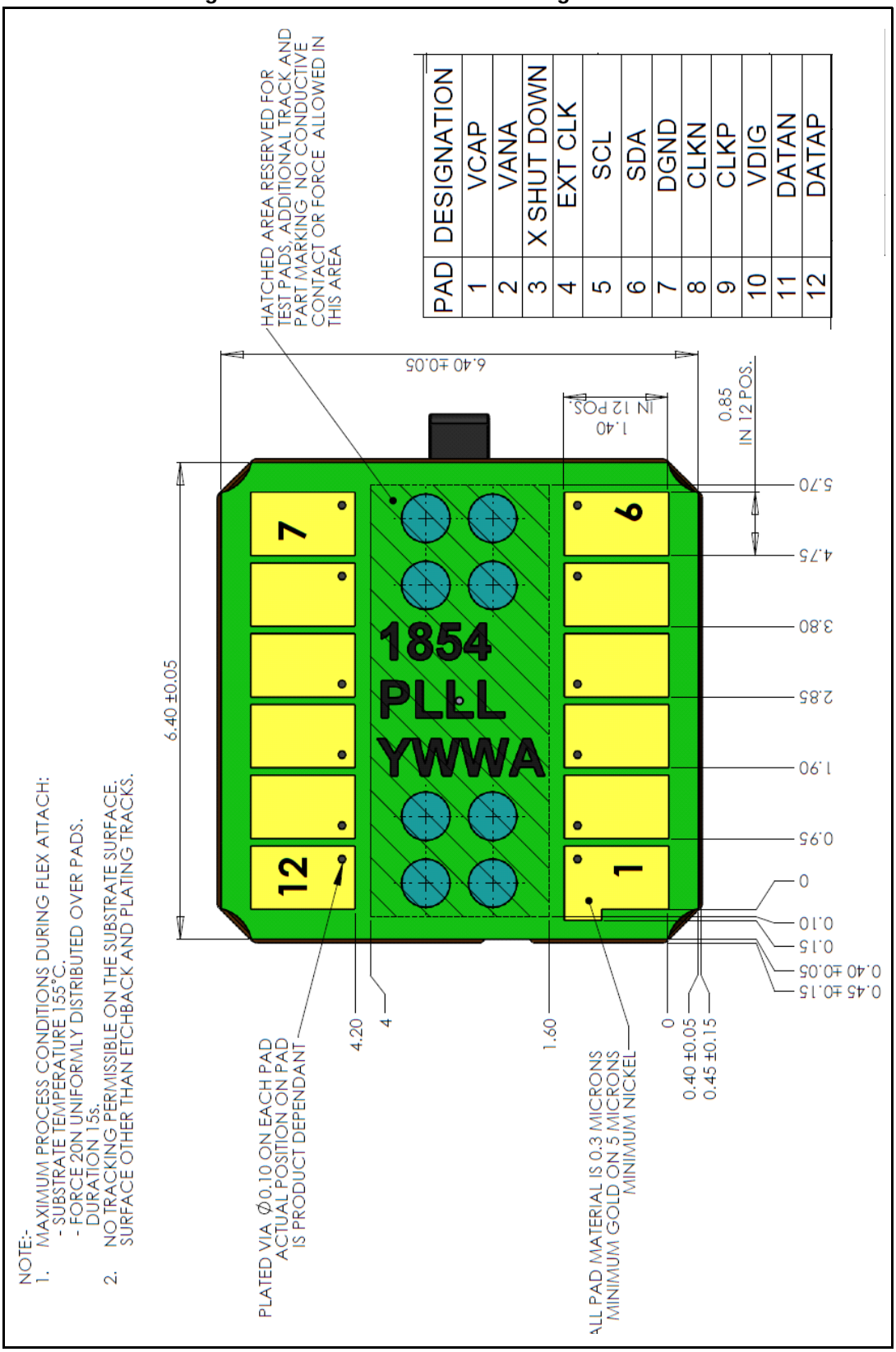


EXCLUSION ZONE NOTES:-
1. EDGES OF CIRCULAR HOLES IN CUSTOMER'S EQUIPMENT MUST NOT INTRUDE INTO THE CONE.
2. EDGES OF RECTANGULAR HOLES MUST NOT PROTRUDE INTO THE PYRAMID.
3. DIMENSIONS SHOWN ARE MAXIMUM.

EXCLUSION ZONE DIMENSIONS

MODULE/ SILICON	A	B	C	D	E	F
854C (EDOF)	71.9°	60.2°	47°	2.50	2	1.50

Figure 53. VX6854LC outline drawing - sheet 3 of 3



15 User precaution

As is common with many CMOS imagers the camera should not be pointed at bright static objects for long periods of time as permanent damage to the sensor may occur.

16 Acronyms and abbreviations

Table 69. Acronyms and abbreviations

Acronym/ abbreviation	Definition
CCP	Compact Camera Port
CCI	Camera Control Interface
CSI	Camera Serial Interface
EDOF	Extended Depth of Field
EMI	Electro Magnetic Interference
EOF	End of Frame
FE	Frame End
fps	Frames per second
FS	Frame Start
HWA	Hardware Accelerator
I2C	Inter ICbus
LSB	Least Significant Byte
LVDS	Low Voltage Differential Signaling
Mbps	Megabits per second
MSB	Most Significant Byte
MSP	Manufacturer Specific Pixels
PCK	Pixel Clock
PCM	Pulse Code Modulation
PLL	Phase Locked Loop
RO	Read Only
RW	Read/Write
SMIA	Standard Mobile Imaging Architecture
SOF	Start of Frame
SubLVDS	Sub-Low Voltage Differential Signaling

17 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

18 Revision history

Table 70. Document revision history

Date	Revision	Changes
27-Oct-2014	1	Initial release.
09-Sep-2015	2	Updated disclaimer