TN0897
Technical note

SPI protocol for ST VIPower High side drivers and automotive smart power devices

Introduction

The document describes a standardized SPI protocol. It defines a common structure of the communication frames and defines specific addresses for product and status information.

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1.1 Feature list

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1.2 Signal description

Serial Clock (SCK): this input signal provides the timing of the serial interface. Data present at Serial Data Input (SDI) is latched on the rising edge of Serial Clock (SCK). Data on Serial Data Out (SDO) is shifted out at the falling edge of Serial Clock (SCK).

Serial Data Input (SDI): this input is used to transfer data serially into the device. It receives the data to be written. Values are latched on the rising edge of Serial Clock (SCK).

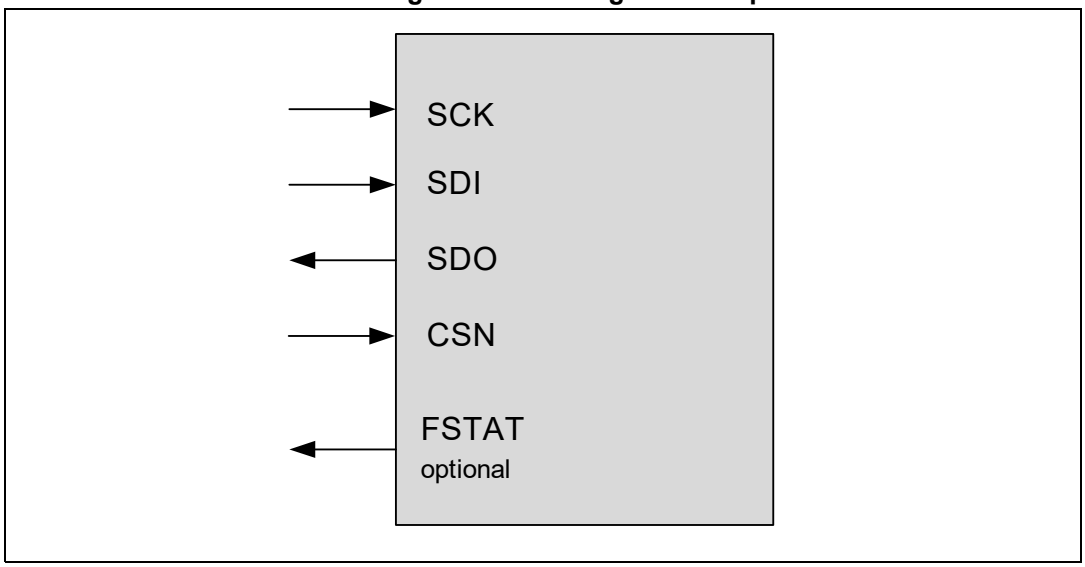
Serial Data Output (SDO): this output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK).

SDO also reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>) while CSN is low and no clock signal is present

Chip Select Not (CSN): when this input signal is High, the device is not selected and Serial Data Output (SDO) is high impedance. Driving this input Low enables the communication. The communication must start and stop on a Low level of Serial Clock (SCK).

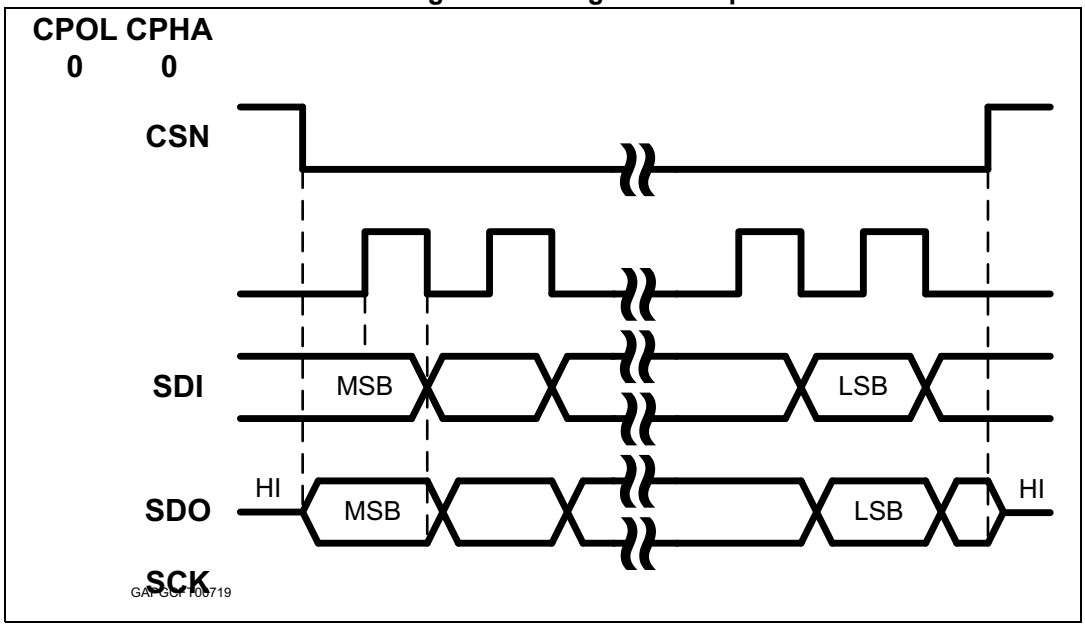
Failure Status (FSTAT) (optional): the <FSTAT> pin reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status Register>). It is an open-drain output signal so that <FSTAT> pins of several devices can be connected to a common pull-up resistor and one microcontroller I/O port in order to indicate a failure in the system.

Figure 1.ST SPI signal description



The SPI can be driven by a microcontroller with its SPI peripheral running in the following mode: CPOL = 0 and CPHA = 0.

Figure 2.SPI signal description



The communication starts at the CSN transition from High to Low. SCK is initially Low.

Data at SDI must be stable at the first SCK transition from Low to High.

Data at SDO is shifted at the first falling edge of SCK.

CSN transition Low to High must occur after the specified number of clock cycles (rising and falling edges of SCK are counted).

2 SPI communication flow

2.1 General description

The proposed SPI communication is based on a standard SPI interface structure using CSN (Chip Select Not), SDI (Serial Data In), SDO (Serial Data Out/Error) and SCK (Serial Clock) signal lines.

At device start-up the master reads the <*SPI-frame-ID*> register (ROM address 3EH) of the slave device. This 8-bit register indicates the SPI frame length (16, 24, or 32 bit) and the availability of additional features.

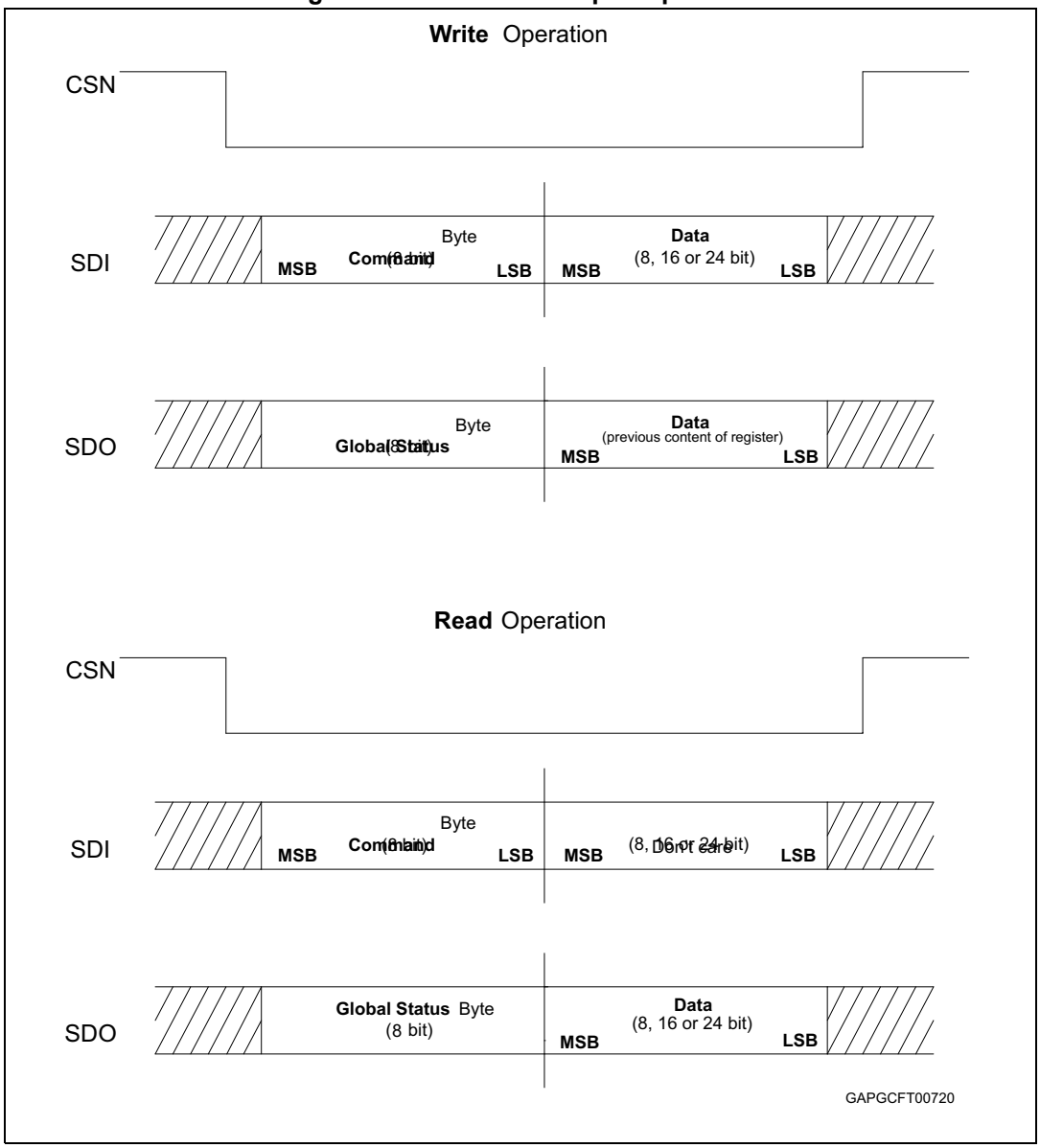
Each communication frame consists of an instruction byte which is followed by 1, 2 or 3 data bytes.

The data returned on SDO within the same frame always starts with the <Global Status> register. It provides general status information about the device. It is followed by 1, 2 or 3 data bytes (i. e. ‘In-frame-response’).

For write cycles the <*Global Status*> register is followed by the previous content of the addressed register.

For read cycles the <Global Status> register is followed by the content of the addressed register.

Figure 3.Communication principle of the ST SPI



2.2 Command byte

Each communication frame starts with a command byte. It consists of an operating code which specifies the type of operation (<Write>, <Read>, <Read and Clear>, <Read Device Information>) and a 6 bit address. If less than 6 address bits are required, the remaining bits are unused but are reserved.

Table 1.Command byte (8 bit)

Operating code		Address					
MSB							**LSB**
OC1	OC0	A5	A4	A3	A2	A1	A0

OCx: operating code

Ax: address

2.2.1 Operating code definition

Table 2.Operating code definition

OC1	OC0	Meaning
0	0	<Write mode>
0	1	<Read mode>
1	0	<Read and clear status>
1	1	<Read device information>

The <Write Mode>, <Read Mode> and <Read and Clear Status> operations allow access to the RAM of the device, i. e. to write and to control registers or read status information.

<Read Device Information> allows access to the ROM area which contains device related information such as the product family, product name, silicon version, register width and availability of a watchdog.

Example 1

For 16-bit frames

Command Byte: 0000 1000

Data Byte: 1111 1111

Write FFH at RAM address 08H

Example 2

For 16-bit frames

Command Byte: 0111 1110

Data Byte: 0000 0000

Read register at RAM address 3EH

Example 3

For 16-bit frames

Command Byte: 1011 1110

Data Byte: 0000 0000

Read register at RAM address 3EH and clear its content at CSN low to high transition

Example 4

For 16-bit frames

Command Byte: 1111 1110

Data Byte: 0000 0000

Read register at ROM address 3EH (i. e. <SPI-frame-ID>)

2.3 Global status register

Table 3.Global Status Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global Error Flag (GEF)	Comm Error	Not (Chip Reset OR Comm Error)	TSD / chip overload	T_{frame} / Temp prewarning	Device specific	Device specific	Fail Safe

Table 4.Definition of Global Status bits

Bit	Description	Optional feature	Polarity	Comment
0	Fail Safe	X	Active high	Indicates that the device is in *Fail Safe Mode* (1). The bit is defined as '0' if no fail-safe functionality is present in the device
1	Device specific	X	Active high	See product datasheet(2)
2	Device specific	X	Active high	See product datasheet(2)
3	Temp pre-warning	X	Active high	The bit is defined as '0' if feature is not present. See product datasheet
4	Thermal Shutdown / Chip Overload	X	Active high	The bit is defined as '0' if feature is not present. See product datasheet
5	Not (Chip Reset OR Communication Error)		Active low	Chip Reset: registers have been set to default Communication Error: see bit 6 The bit is cleared automatically after a valid communication with any register After Power-On the bit is '0' and is set to '1' by a valid SPI communication
6	Communication Error		Active high	Bit is set if the number of clock cycles during CSN = low does not match with the specified frame width or if any other device specific communication error occurs. See product datasheet(2)
7	Global Error Flag (GEF)		Active high	Logic OR combination of all failures in the <Global Status register> and additional device specific failures

1. Fail-safe Mode is an operating mode where the device enters a safe state. The precise definition is device specific and is defined in the product datasheet.
2. See *Appendix A: Reference documents*.

2.3.1 Global error flag definition

The <Global Error Flag> (GEF) is a diagnosis information which is transmitted with every communication frame. It indicates that a failure condition which has been detected can be identified in the Status Registers.

The GEF is composed by a logical OR combination of failures notified in the <Global Status> register and in a device specific Status Registers.

Bits 1, 2 and 3 of the <Global Status> register may be maskable in the <Configuration> register, i.e. these bits may be excluded from the GEF composition.

The clock monitor counts the number of clock pulses during a communication frame (while CSN is low). If the number of SCK pulses does not correspond with the frame width indicated in the <SPI-frame-ID> (ROM address 3EH) the frame is ignored and the <Communication Error> bit in the <Global Status> register is set.

This safety function is implemented to avoid an unwanted activation of output stages by a wrong communication frame.

If a communication error is detected during a read operation, the <Communication Error> bit in the <Global Status> register is set, but the register read is transferred to the SDO pin. If the number of clock cycles is smaller than the frame width, the data at SDO is truncated. If the number of clock cycles is larger than the frame width, the data at SDO is filled with ‘0’.

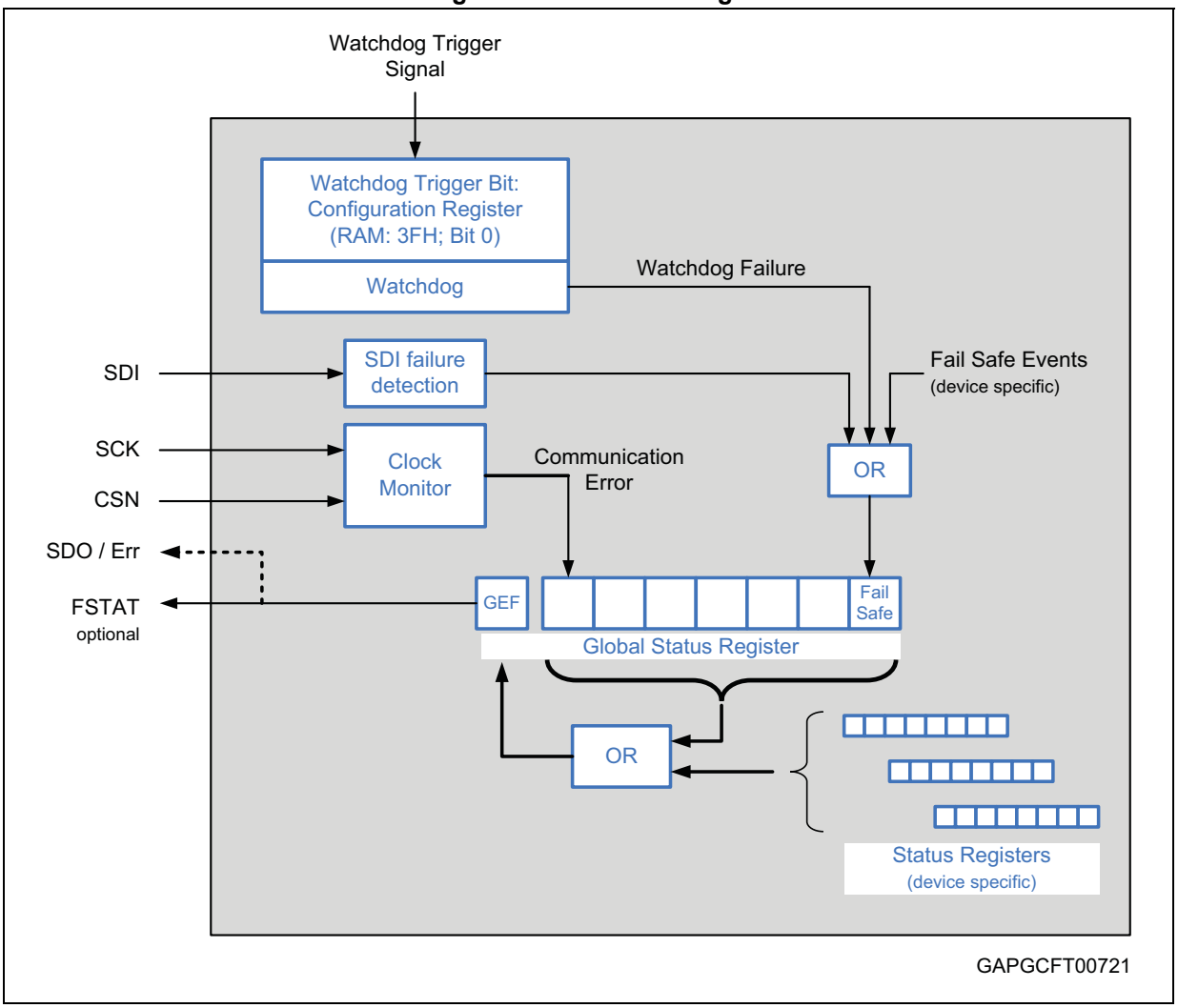
If the frame width is greater than 16 bits, initial Read of <SPI-frame-ID> using a 16 bits communication sets the <Communication Error> bit of the <Global Status> register. A subsequent correct length transaction is necessary to correct this bit.

Due to this safety functionality a daisy chaining of SPI is not possible. Instead, a parallel operation of the SPI bus by controlling the CSN signal of the connected ICs is recommended.

The *SPI Failure Detection* identifies a short circuit condition at SDI if all bits within a received frame are ‘0’ (short to GND) or ‘1’ (short to V_{dd}).

In this case the communication frame is ignored, the device enters the <Fail-Safe Mode> and the <Fail-Safe> bit in the <Global Status> register is set.

Figure 4.Global error flag definition



The open-drain <FSTAT> pin is an optional feature which reflects the status of the <Global Error Flag> (Bit 7 of the <Global Status> register). Several <FSTAT> pins in a system can be connected to one microcontroller I/O port in order to indicate an error in the system. The faulty device can then be identified by reading the <Global Error Flag> bits of all devices.

The <Global Error Flag> is also available on the SDO pin while CSN is low and the clock signal is stable (high or low). The flag at SDO remains as long as CSN is low. This operation does not set the <communication error> bit in the <Global Status Register>. The refresh-procedure of the GEF at SDO is device specific.

A status change during an SPI communication can cause an inconsistency in the <Global Status> register and other Status Registers. For devices intended for safety critical applications, precautions must be taken to avoid such inconsistencies.

2.4 Configuration register (optional)

The <Configuration> register is optional. When available, it is always accessible at RAM address 3FH.

Table 5.Configuration register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device specific fault mask	Device specific fault mask	Device specific fault mask	Device specific fault mask	Masking Bit 3 of <Global Status> register	Masking Bit 2 of <Global Status> register	Masking Bit 1 of <Global Status> register	WD Trigger

<WD Trigger>: this Bit is reserved to trigger the watchdog. The precise procedure required to serve the watchdog is device specific and defined in the product datasheet. The bit is reserved if the device has no watchdog.

<Masking>: bits 1, 2 and 3 allow masking of the corresponding bit in the <Global Status> register. If a Status Bit is masked, it is excluded from the <Global Error Flag> composition, i. e. the information is still indicated in the <Global Status> register but it is not contributing to the <Global Error Flag> (Bit 7 of the <*Global Status*> register).

1 = corresponding bit is masked, 0 = corresponding bit is not masked

3 Address mapping

3.1 RAM address range

Table 6.RAM operation code

Op Code		Operation
OC1	OC0	
0	0	<Write>
0	1	<Read>
1	0	<Read and Clear Status>

Table 7.RAM address range

RAM Address	Description	Access
3FH	<Configuration> optional	R/W
...		
	Status Registers	R
		R
...		
	Control Registers	R/W
		R/W
...		
00H	Reserved(1)	

1. Address 00H is reserved. A Write operation to this address is recognized as a SDI failure (short to GND) and causes the device to enter Fail-Safe Mode.

The RAM memory area contains the Control Registers (Read/Write) and Status Registers (Read). The address assignment for these registers is device specific and defined in the product datasheet.

The register width can be 8, 16 or 24 bit and is defined in the <SPI Frame ID>.

For the <Configuration> register the eight most significant bits of the memory cell are used.

All unused RAM addresses are read as ‘0’.

3.2 ROM address range

Table 8.ROM operation code

Op Code		Operation
OC1	OC0	
1	1	<Read Device Information>

Table 9.ROM address range

ROM Address	Device Information	Access
3FH	Reserved(1)	
3EH	<SPI frame ID>	R
04H to 3DH	Product specific See product datasheet	R
03H	<product code 2>	R
02H	<product code 1>	R
01H	<silicon version>	R
00H	<ID Header>	R

1. ROM address 3FH is unused. An attempt to access this address is recognized as a SDI failure (short to V_{DD}) and causes the device to enter Fail-Safe Mode.

The register width of the ROM area is 8 bit. For products with 16 or 24 bit register width, the eight most significant bits of the memory cell are used.

All unused ROM addresses are read as ‘0’.

4 Write operation

The write operation starts with a Command Byte followed by 1, 2, or 3 data bytes (depending on the register width of the device). The number of data bytes is specified in the <SPI-frame-ID>.

4.1 Write command format

Figure 5.Write command format

Command byte

MSB							**LSB**
Op Code		**Address**					
0	0	A5	A4	A3	A2	A1	A0

Data byte 1

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

Data byte 2(1)

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

1. Only for 24-bit SPI frame width.

A0 to A5: address bits

4.2 Format of data shifted out at SDO during write cycle

Figure 6.SDO Frame composition during WRITE operation

Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global Error Flag (GEF)	Comm Error	Not (Chip Reset OR Comm Error)	TSD / chip overload	T_{frame}	Device specific	Device specific	Fail Safe

Data byte 1 - previous content of addressed register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Data byte 2 - previous content of addressed register(1)

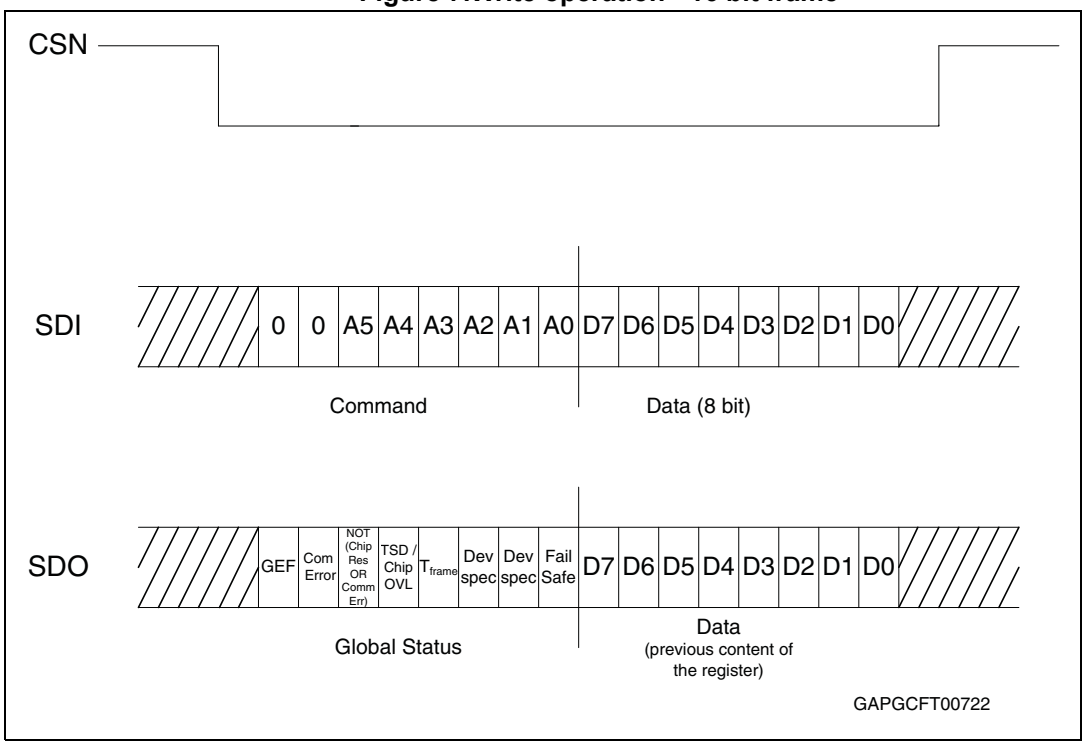
MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

1. Only for 24-bit SPI frame width.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the previous content of the accessed register.

Figure 7.Write operation - 16 bit frame



5 Read operation

The Read operation starts with a Command Byte followed by 1, 2, or 3 data bytes. The number of data bytes is specified in the <SPI-frame-ID>. The content of the data bytes is ‘don’t care’. The content of the addressed register is shifted out at SDO within the same frame (‘in-frame response’).

5.1 Read command format

Figure 8.Read command format

Command byte

MSB							LSB
Op Code		Address					
0	1	A5	A4	A3	A2	A1	A0

Data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Data byte 2(1)

MSB							LSB
0	0	0	0	0	0	0	0

1. Only for 24-bit SPI frame width.

A0 to A5: address bits

5.2 Format of data shifted out at SDO during Read cycle

Figure 9.SDO Frame composition during READ operation

Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global Error Flag (GEF)	Comm Error	Not (Chip Reset OR Comm Error)	TSD / chip overload	T_{frame}	Device specific	Device specific	Fail Safe

Data byte 1 - content of addressed register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Data byte 2 - content of addressed register(1)

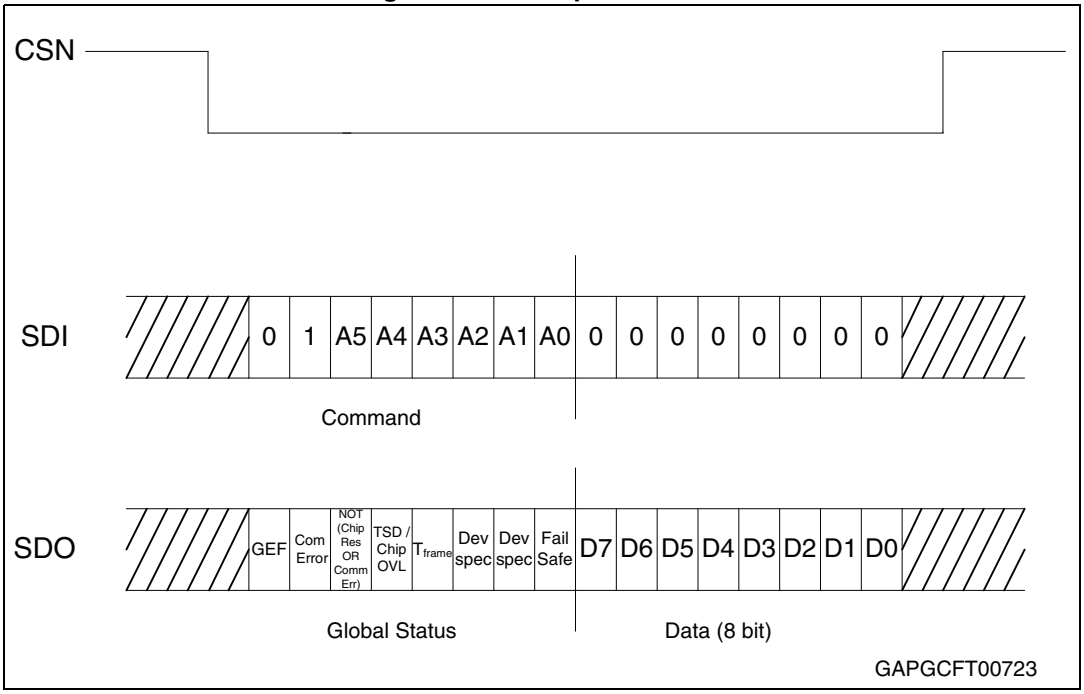
MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

1. Only for 24-bit SPI frame width.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 10.Read operation - 16 bit frame



6 Read and clear status operation

The <Read and Clear Status> operation starts with a Command Byte followed by 1, 2, or 3 data bytes. The number of data bytes is specified in the <SPI-frame-ID>. The content of the data bytes is ‘don’t care’. The content of the addressed status register is transferred to SDO within the same frame (‘in-frame response’) and is subsequently cleared.

A <Read and Clear Status> command addressed to the <Configuration> register (RAM: 3FH) clears all status registers (incl. the <Global Status> register) simultaneously and reads back the <Configuration> register.

6.1 Read and clear status command format

Figure 11.Read and clear status command format

Command byte

MSB							LSB
Op Code		**Address**					
1	0	A5	A4	A3	A2	A1	A0

Data byte 1

MSB							LSB
0	0	0	0	0	0	0	0

Data byte 2(1)

MSB							LSB
0	0	0	0	0	0	0	0

1. Only for 24-bit SPI frame width.

A0 to A5: address bits

6.2 Format of data shifted out at SDO during read and clear status operation

Figure 12.SDO Frame composition during READ and CLEAR operation

Global status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Global Error Flag (GEF)	Comm Error	Not (Chip Reset OR Comm Error)	TSD / chip overload	T_{frame}	Device specific	Device specific	Fail Safe

Data byte 1 - content of addressed status register or configuration register

MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

Data byte 2 - content of addressed status register(1)

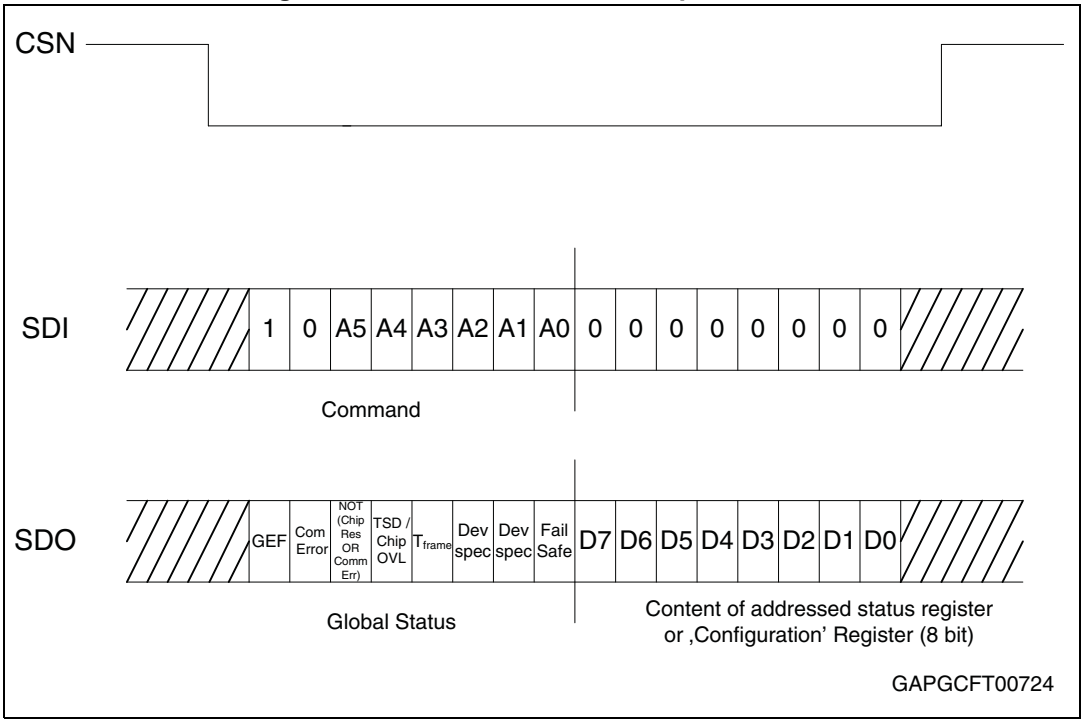
MSB							LSB
D7	D6	D5	D4	D3	D2	D1	D0

1. Only for 24-bit SPI frame width.

Failures are indicated by activating the corresponding bit of the <Global Status> register.

The returned data byte(s) represent(s) the content of the register to be read.

Figure 13.Read and clear status operation - 16 bit frame



7 Read device information

Product specific information is stored in the ROM area and can be read using a dedicated operating code (<Read Device Information>).

Table 10.Device information

Op Code		Address	Device Information
OC1	OC0		
1	1	3FH	Reserved
1	1	3EH	<SPI-frame-ID>
1	1	04H to 3DH	Product specific See product datasheet
1	1	03H	<Product Code 2>
1	1	02H	<Product Code 1>
1	1	01H	<Silicon Version>
1	1	00H	<ID-Header>

7.1 ID-Header

Table 11.ID-Header

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Fam		ROM Address Range for <Device Information>					

The <Address Range> specifies the highest ROM address which contains <Device Information>.

The standard value if no additional information registers are present is 03H

(è content of ID-Header is: XX00 0011)

The <Family Identifier> specifies the product family according to the following family codes:

Table 12.Product family

Bit 7	Bit 6	Product family
0	0	VIPower
0	1	BCD
1	0	VIPower hybrid

7.2 Silicon version

Table 13.Silicon version

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved				Silicon Version			

The <Silicon Version> provides information about the silicon version according to the following table:

Table 14.Silicon version coding

Bit3	Bit 2	Bit 1	Bit 0	Silicon version
0	0	0	0	First silicon
0	0	0	1	V2

7.3 Product code

<Product Code 1> and <Product Code 2> represent a unique set of codes to identify the product. The code is specified in the datasheet (see *Appendix B: Product code*).

7.4 SPI-Frame-ID

The <SPI-frame-ID> provides information about the register width (1, 2, 3 bytes) and the availability of additional features like <Burst Mode Read> and <watchdog>.

Table 15.SPI-frame-ID

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BR	WD	X	X	X	Frame width		

BR: Burst-Mode Read (1 = Burst-Mode Read is supported)

WD: Watchdog (1 = available, 0 = not available)

Frame width: width of SPI frame (see *Table 16*)

Table 16.Frame width

Bit 2	Bit 1	Bit 0	Frame width	Command	Data
0	0	1	16 bit	8 bit	8 bit
0	1	0	24 bit	8 bit	16 bit
1	0	0	32 bit	8 bit	24 bit

Appendix A Reference documents

Table 17. Reference documents

Doc Name	ID	Title
DS7055	18309	Power management IC with LIN transceiver
DS6868	17639	Power management IC with LIN and high speed CAN
DS9732	024767	Advanced power management system IC with embedded LIN and high speed CAN transceiver supporting CAN Partial Networking
DS7038	18620	Automotive door actuator driver
DB1487	022498	Door actuator driver
DS6752	17242	Octal half-bridge driver with SPI control for automotive application
DS6418	16082	Hexa half-bridge driver with SPI control for automotive applications
DB1223	18451	High efficiency constant current LED driver
DS8820	022637	Integrated microprocessor driven device intended for LIN controlled exterior mirrors
DS6340	15872	SPI control diagnosis interface device for VIPower™ M0-5 and M0-5E high side drivers
DS6984	18061	Quad channel high-side driver
DS8688	22315	Quad-channel high-side driver with 16-bit SPI interface

Appendix B Product code

Table 18.Product code

Product	Product code	
	PC1 hex	PC2 hex
L99PM60J	0C	4B
L99PM62GXP	13	4B
L99PM72GXP	4B	27
L99DZ80EP	52	48
L99DZ81EP	01	55
L99MD01	3E	4E
L99MD02	3E	4E
L99LD01	31	51
L99MM70XP	48	48
VNQ6040S-E	1A	00
VNQ6004SA-E	1A	00

Revision history

Table 19. Document revision history

Date	Revision	Changes
31-Oct-2012	1	Initial release.
23-Sep-2013	2	Updated Disclaimer.
12-Apr-2021	3	Updated: – Document title; – *Table 17: Reference documents*; – *Table 18: Product code*.