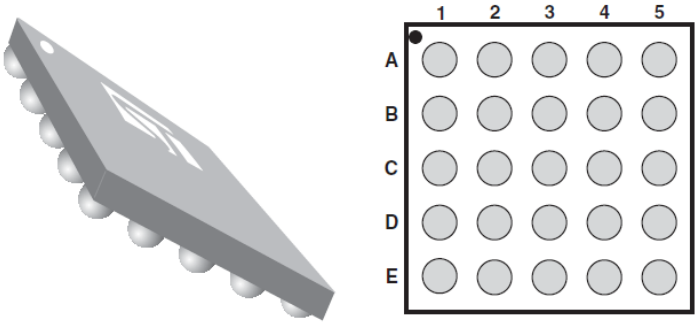
IPAD 500 µm Flip Chip: package description and recommendations for use

Introduction

This document provides package and usage recommendations for 500 µm pitch Flip Chip packages. For information about 400 µm pitch Flip Chip packages, see application note AN2348.

The development of highly integrated products drives the competitive market for portable equipment, especially mobile phones. To enable manufacturers to reduce the size, thickness, and weight of their products, STMicroelectronics has developed Flip Chip packages. The electrical performance of Flip Chips is improved due to shorter connections compared with standard plastic packages such as TSSOP, SSOP, or BGA.

Figure 1. Typical Flip Chip package



The Flip Chip package family is designed to meet the same quality and reliability standards as standard semiconductor plastic packages. Flip Chip packages are considered surface-mount devices and are assembled on printed circuit boards (PCBs) without requiring special or additional process steps. This package does not require extra underfill to improve reliability or protect the device. The package is compatible with existing pick-and-place equipment for board mounting. Only lead-free, RoHS-compliant Flip Chip packages are available in mass production.

This application note covers the following topics:

- Product description
- Mechanical description
- Packing specifications and labeling description
- Recommended storage and shipping instructions
- Soldering assembly recommendations
- User responsibility and returns
- Changes
- Delivery quantity
- Quality

1 Product description

Flip Chips are manufactured using a wafer-level process developed by STMicroelectronics. Solder bumps are attached to the I/O pads on the active side of the wafer, allowing the production of bumped dice. The I/O contact layout can be either a matrix or set at the periphery. No redistribution layer is used, minimizing parasitic inductances from redistribution metal tracks.

The lead-free bump composition is 98.25 % Sn, 1.2 % Ag, 0.5 % Cu, and 0.05 % Ni. This composition is fully compatible with standard lead-free reflow processes. The bump diameter is 310 µm, which allows the pick-and-place process to be compatible with existing equipment, especially that used for ball grid array (BGA) packages. It is also compatible with the PCB design rules for standard integrated circuits.

An optional coating is available on the flat side of the package.

These components are delivered in tape-and-reel packing with the bumps facing down in the carrier tape cavity. The other side of the component is flat, allowing picking as with standard surface-mount device (SMD) packages.

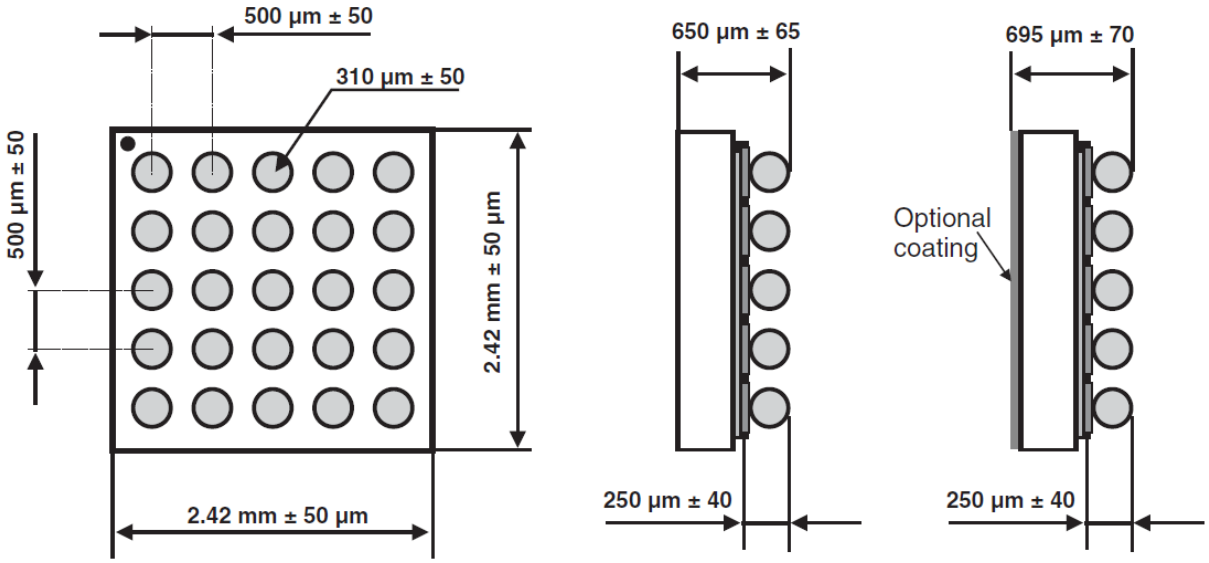
All devices are electrically tested before packing. The product references are marked on the flat side of the device.

Devices are 100 % electrically tested before packing. The product references are marked on the flat side of the device.

2 Mechanical description

Mechanical dimensions for Flip Chips are provided using a product example (see Figure 2). The bumps are lead-free. The bump composition is 98.25 % Sn, 1.2 % Ag, 0.5 % Cu, and 0.05 % Ni alloy, with a near-eutectic melting point of 218 °C to 227 °C. Die size and bump count are adapted to connection requirements.

Figure 2. Mechanical dimensions of a 5 x 5 bump matrix array (sample)



Note: The package height of 0.65 mm (0.695 mm for optionally coated packages) is valid for a die thickness of 0.40 mm. With a die thickness of 0.64 mm, the total package height is 0.89 mm.

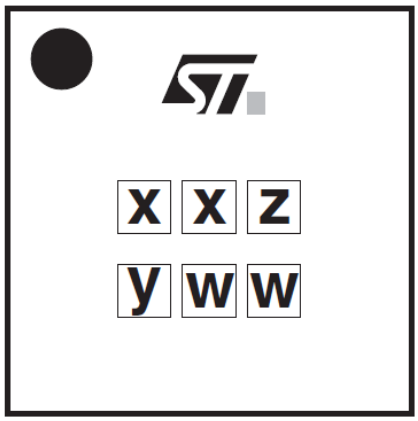
Flip Chip tolerances for bump diameter and height are very tight, ensuring consistent bump shape and good coplanarity between bumps. Optical measurements performed using vertical focus show bump and die coplanarity below 80 µm.

The product marking on the flat side is shown in Figure 3. The Flip Chip includes a pin marker, A1 (see Figure 1), on both the flat side and the bump side. This feature allows users to easily determine the orientation of the component before and after assembly. The dots marked on the flat side and the bump sides are designed for detection by standard vision systems.

Marking dimensions are linked to the die size.

Figure 3. Flip Chip marking example for 5 x 5 bump matrix array

Dot, ST logo
ECOPACK status
xx = marking
z = manufacturing location
yww = datecode
(y = year
ww = week)
When very small die sizes leave insufficient space, the ST logo and ECOPACK symbol are omitted from the marking.



3 Packing specifications and labeling description

Flip Chips are delivered in tape-and-reel packaging to ensure compatibility with standard high-volume surface-mount device (SMD) components. The tape-and-reel materials comply with *EIA-481-D*, *IEC 60286-3*, and *EIA 763 (783)* standards. Features not specified in this section comply with *EIA-481-D*, *IEC 60286-3*, and *EIA 763 (783)* standards.

3.1 Carrier tape

Flip Chips are placed in the carrier tape with the bump side facing the bottom of the cavity, allowing components to be picked up by the flat side. Flipping the package is not required for mounting on the printed circuit board. The products are positioned in the carrier tape with pin A1 on the sprocket hole side. Carrier tape mechanical dimensions are shown in Figure 4. The standard tape width is 8 mm for die sizes smaller than 3 mm (dimension B0).

Note: 12 mm carrier tape width may be used for a larger die size to be in line with EIA standards.

Figure 4. Tape dimensions for Flip Chips (650 µm thickness)

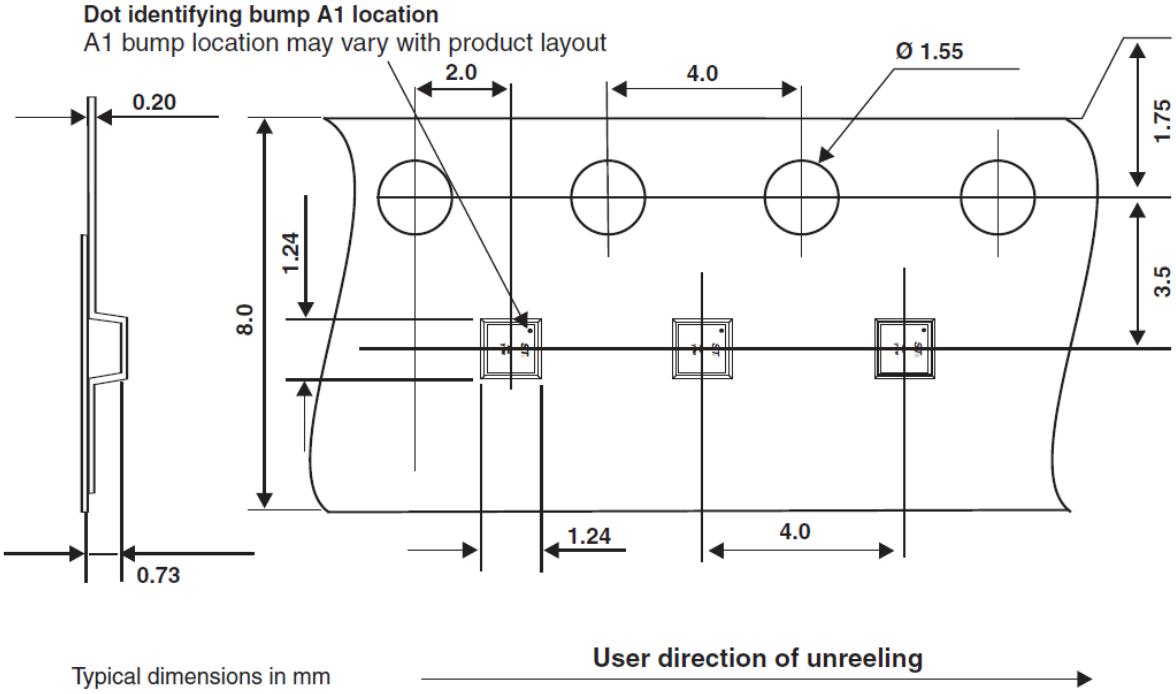


Table 1. Tape cavity sizing

Dimension	Die with both sides smaller than or equal to 1.5 mm	Die with one side larger than 1.5 mm
A0 and B0	Die side size + 70 µm	Cavity dimensions established to ensure that component rotation cannot exceed 5° max.

The cavities in the carrier tape have been designed to avoid any damage to the components. No hole is present in the cavity to avoid any impact or any external contamination to the solder bumps.

The embossed carrier tape is made of black conductive material with a surface resistivity between 10^4 ohm/sq and 10^8 ohm/sq. This material protects components from electrostatic discharge and ensures complete discharge before placement on the PCB. The conductivity remains constant and is not affected by shelf life or humidity. The material does not break when bent and does not leave any residue, powder, or flakes.

3.2 Cover tape

The carrier tape is sealed with a transparent, antistatic polyester film cover tape. The surface resistivity of the cover tape ranges between 1 × 10^5 ohm/sq and 1 × 10^{11} ohm/sq. The cover tape uses a heat-activated adhesive. Its tensile strength is greater than 10 N.

The peeling force of the cover tape is between 0.08 N and 0.5 N, in accordance with *EIA-481-D* and *IEC 60286-3* test methods. Peel the cover tape in the direction opposite to the carrier tape travel. The angle between the cover tape and the carrier tape must be between 165° and 180°. Perform the test at a speed of 120 mm/minute ± 10 %.

3.3 Reels

The sealed carrier tape with the Flip Chip is wound on seven-inch reels (see Figure 5). These reels comply with the *EIA-481-C* standard and are made of antistatic polystyrene. The reel color may vary depending on the supplier.

The quantity of dice per reel is 5000, with a typical package thickness of 650 µm. In compliance with *IEC 60286-3*, each reel contains a maximum of 0.1 % empty cavities. Two successive empty cavities are not permitted. Each reel may contain components from two different wafer lots.

Each reel includes a minimum leader of 400 mm and a minimum trailer of 160 mm, in compliance with *EIA 481-C* and *IEC 60286-3* standards. The leader is a section of carrier tape with empty cavities, sealed by cover tape at the beginning of the reel (external side). The leader attaches to the last turn of the carrier tape with adhesive tape. The trailer is located at the end of the reel and consists of empty, sealed cavities (see Figure 6).

Figure 5. Seven-inch reel mechanical dimensions outline

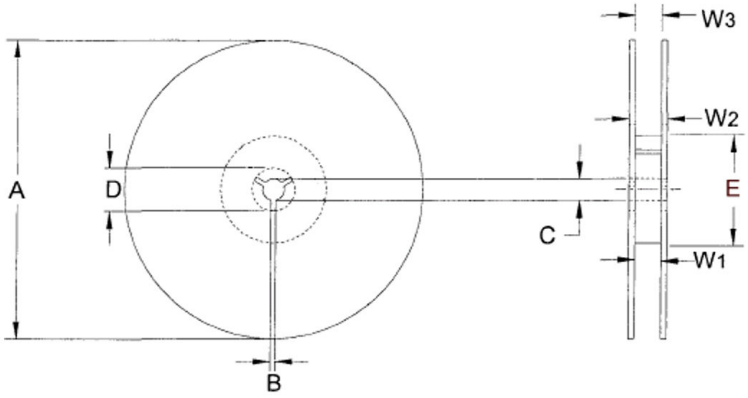
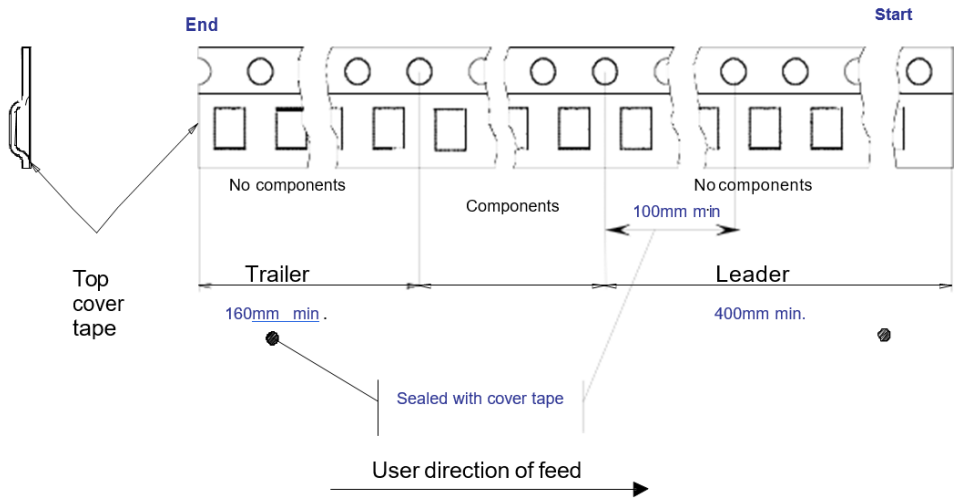


Table 2. Seven-inch reel mechanical dimensions (in mm)

A max.	B min.	C	D min.	E min.	W1 (Hub)	W2	W3 (external)
180	1.5	13 +0.5/-0.2	20.2	60	8.4 +1.5/-0	14.4	8.4 +2.5/-0.5

Figure 6. **Leader and trailer**



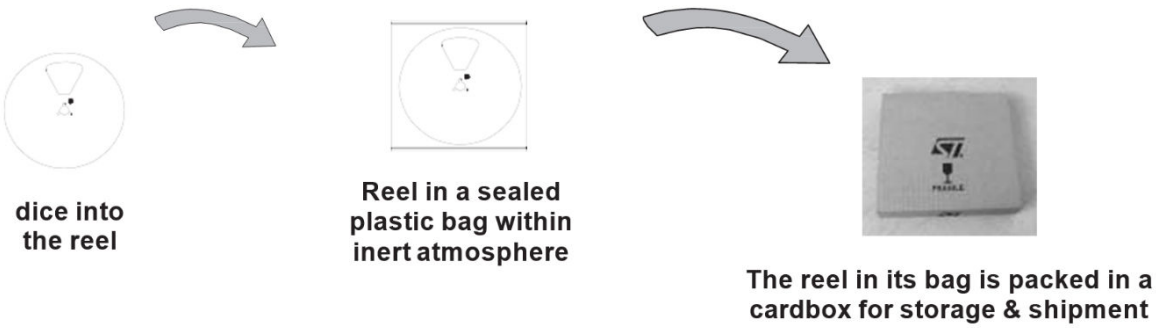
3.4 Final packing

Each reel is heat-sealed under an inert atmosphere in a transparent, recyclable, antistatic polyethylene bag with a minimum material thickness of 4 mils.

Reels are then packed in cardboard boxes.

The complete description of the packing is shown in Figure 7.

Figure 7. **Packing flow chart**



3.5 Labeling

To ensure component traceability, labels are affixed to the reels and the cardboard box. The seven-inch reels and the cardboard box are identified by labels that include the part number, shipped quantity, and traceability references (see Figure 8).

Traceability is ensured for each production lot and shipment lot through labeling.

The trace code number printed on the labels enables backward traceability from the lot received by the customer at each step of the process, including in and out dates and quantities at diffusion, assembly, test, and final storage. Forward traceability enables tracking of lot history from the wafer fabrication facility to the customer location.

Figure 8. **Example of a reel label**

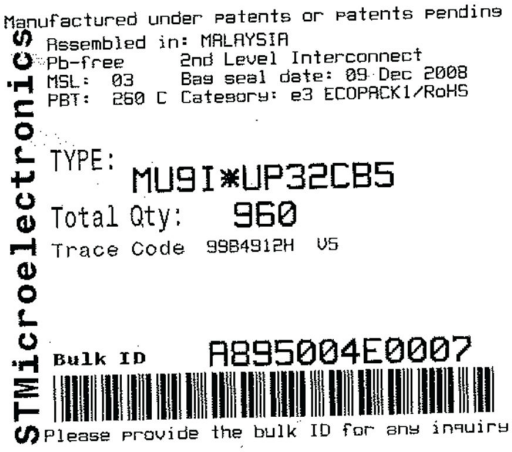


Table 3. **Parameter reel label**

Field	Field type
Assembled in	Mandatory-country of origin
Pb-free 2nd level interconnect	As per JEDEC standard JESD97
MSL	Mandatory for concerned products as defined in MPI Moisture sensitivity level as per *JEDEC J-STD-020* mandatory for SMD
Bag seal date	For MSL 2 and above, date of vacuum sealing of dry bag For MSL = 1, “Not moisture sensitive” must be printed instead
PBT	Peak package Body temperature as *JEDEC J-STD-020* mandatory for the SMD
Category	Pb-free category as pr JEDEC standard JESD97 mandatory for concerned products as defined in MPI
Eco level	Mandatory for ECOLEVEL devices only as defined in MPI
Type	Mandatory: • First line: Not required • Second line: Raw line product name
Total qty	Mandatory: Bulk quantity
Trace code	Mandatory: Traceability code with wafer fab Production area code
Bulk ID	Mandatory: Bulk ID number, Start with A
Bar code	Mandatory: Bar code area

3.6 Recommended storage, shipping instructions and descriptions

Flip Chip reels are packed under an inert nitrogen (N_2) atmosphere in a sealed bag. For shipment and handling, the reels are packed in a cardboard box.

STMicroelectronics recommends the following shipping and storage conditions:

- Relative humidity between 15 % and 70 %
- Temperature ranges from -55 °C to +150 °C

Components in an unopened sealed bag can be stored for up to six months after shipment. Components in tape and reel must be protected from direct sunlight.

Moisture sensitivity level (MSL) according to *JEDEC J-STD-020C* does not apply to Flip Chip devices because they have no plastic encapsulation. Therefore, there is no risk of moisture absorption or package cracks.

4 Soldering assembly recommendations

4.1 PCB design recommendations for 500 µm Flip Chips

For optimum electrical performance and highly reliable solder joints, STMicroelectronics recommends the PCB design guidelines listed in Table 3.

Table 4. PCB design recommendations

Reference	Description
PCB pad design	Non solder mask defined Micro via under bump allowed
PCB pad size	Ø = 300 µm max. (circular) – 250 µm recommended
Solder mask opening	Ø = 340 µm min. (for 300 µm diameter pad)
PCB pad finishing	Cu – Ni (2–6 µm) – Au (0.2 µm max) or Cu OSP (Organic Solderability Preservative)

To optimize the natural self-centering effect of CSP on the PCB, PCB pad positioning and size have to be properly designed.

Note: A gold layer finishing on the PCB pad is not recommended (low joint reliability).

Microvias

An alternative to routing on the top surface is to route on buried layers. To achieve this, connect the pads to the lower layers using microvias.

4.2 PCB assembly guidelines

For Flip Chip mounting on the PCB, STMicroelectronics recommends using a solder stencil aperture of up to 330 × 330 µm and a typical stencil thickness of 125 µm.

Flip Chips are fully compatible with near-eutectic solder paste consisting of 95.8% Sn, 3.5% Ag, and 0.7% Cu, with no-clean flux.

STMicroelectronics recommendations for Flip Chip board mounting are illustrated in the soldering reflow profile shown in Figure 9.

Figure 9. ST ECOPACK recommended soldering reflow profile for Flip Chip mounting on PCB (definitions)

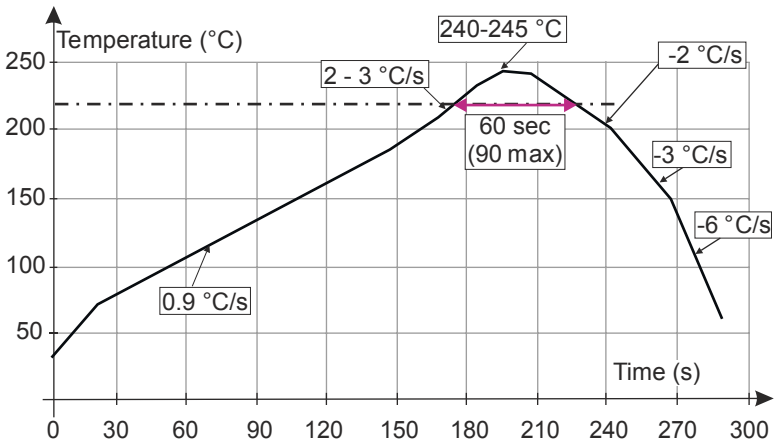


Table 5. ST ECOPACK recommended soldering reflow profile for Flip Chip mounting on PCB (values)

Profile	Value	
	Typical	Max.
Temp. gradient in preheat (T = 70 – 180 °C)	0.9 °C/s	3 °C/s
Temp. gradient (T = 200 – 225 °C)	2 °C/s	3 °C/s
Peak temp. in reflow	240 - 245 °C	260 °C
Time above 220 °C	60s	90 s
Temp. gradient in cooling	-2to - 3 °C/s	-6 °C/s
Time from 50 to 220 °C	160 to 220 s	

Dwell time in the soldering zone, where the temperature is higher than 220 °C, must be as short as possible to prevent damage to components and substrates.

Peak temperature must not exceed 260 °C.

A controlled atmosphere, such as nitrogen (N_2) or forming gas (N_2H_2), is recommended throughout the entire reflow process, especially when the temperature is above 150 °C.

Flip chips can withstand three reflow cycles according to the recommended profile. This allows compatibility with double reflow when surface-mount devices (SMDs) are mounted on both sides of the printed circuit board (PCB), plus one additional repair cycle.

A maximum of three soldering reflow cycles are allowed for these lead-free packages, including repair steps.

Use no-clean paste to avoid cleaning operations.

To prevent bump cracks, do not use ultrasonic cleaning methods.

4.3 Underfilling

Underfilling is not essential for Flip Chips. These devices can operate without underfill if the process temperature does not exceed 175 °C and if the process time is short (typically 5 minutes).

4.4 Manual rework

Flip chips can tolerate one repair in addition to the two reflows described in Section 4.2: PCB assembly guidelines.

As with other BGA-type packages, the use of laser systems is the most suitable method for flip chip repair.

Manual hot gas soldering is acceptable, but iron soldering is not recommended.

For leaded flip chip manual rework, the maximum temperature allowed is 260 °C (compatible with lead-free standards), and the dwell time must not exceed 30 seconds.

For lead-free flip chip manual rework, the maximum temperature allowed is also 260 °C.

The typical soldering profile shown in Figure 9 can be used.

Remove the device

The rework process begins with device removal. To remove the device, apply heat to melt the solder joints so the component can be lifted from the board.

Large-area bottom-side preheaters can be used to raise the board temperature. This helps to minimize board warping and reduce the amount of heat needed on the component.

Apply top heating using a laser or convective hot gas nozzle, selecting a nozzle size matching the component footprint. After the solder has melted, apply vacuum through the pick-up nozzle to lift the component.

Direct heat carefully to avoid reflowing solder joints of adjacent components. Shielding, gas flow control, and accurate temperature management are key.

Removing solder

The next step is to clean solder from the work site. Due to space constraints and the need for precise temperature control, automatic tools are recommended.

Typically, site cleaners use controlled noncontact gas heating combined with vacuum tools. The objective is to remove residual solder without damaging pads, solder masks, or adjacent components, and to prepare the site for the application of a new component.

New device soldering

For device placement, several solutions are possible:

- Use a mini-stencil and solder paste, then place the device. This solution is preferred to ensure homogeneous assembly conditions when assembling a WLCSP (wafer-level chip scale package) with solder paste, even if small footprints and tight dimensions make this operation difficult.
- Apply no-clean flux to the site and place the device.
- Dip the WLCSP in no-clean flux, then place it on the board.

The next operation is to reflow the solder joint by applying controlled heat to the component. This process is similar to component removal; however, accurate temperature control is essential to ensure proper soldering of the joint.

Alternatively, reflow can be performed by placing the entire board in a furnace. See for reflow profile recommendations.

Equipment

Systems for these operations are available at different automation levels. Methods and techniques used in advanced automatic systems can be replicated with manual equipment. Do not use soldering irons for these operations. Avoid using tweezers or any picking tools that apply pressure to the sides or bottom (bump side) of the WLCSP, as these tools can damage the silicon and cause chip outs.

Figure 10 shows an example of semi-automatic equipment for component rework. (See the website of comintec for more information.)

Figure 10. Comintec ONYX32 - Semi-automatic equipment for component rework

ONYX32 Key features

- Fully automated X,Y,Z, and theta control
- Fully automated alignment using digital feature separation (DFS) technology
- Precision force sensor and mass flow controller
- Four zone bottom preheater
- Flux dipping station
- FireWire (*IEEE 1394*) controls
- Visual machines software
- Machine table including power supply cabinet

ONYX32 options

- Dispensing head for solder paste, flux, underfill or adhesives
- Non-contact temperature sensor
- Site solder removal system

5 Changes

STMicroelectronics reserves the right to implement minor changes to geometry and manufacturing processes without prior notice. These changes do not affect the electrical characteristics of the die, the pad layout, or the maximum die size. However, for confirmed orders, no changes are made without customer approval.

6 Quality

6.1 Electrical inspection

Flip Chip products are electrically probed for all critical parameters defined in the ST product specification. Electrical testing is the final operation before packing. Other parameters are specified by technology, design rules, and continuous monitoring systems.

6.2 Visual inspection

A visual control is performed on all manufacturing lots according to the *MIL-STD-883* Method 2010.

7 Conclusion

Lead-free Flip Chip packages have been developed by STMicroelectronics for electronic applications where integration and performance are primary concerns for designers. STMicroelectronics Flip Chip packages offer the following benefits:

- Significant board space savings: The package size equals the die size, with a total height less than 715 µm.
- Enhanced electrical performance: Parasitic inductance is minimized due to very short electrical paths and the absence of a redistribution layer.
- High reliability: Integration of complete functions, traditionally based on discrete interconnected components, increases reliability.

Flip Chip packages are delivered in tape and reel and are fully compatible with other high-volume SMD components, such as standard plastic packages or CSP/BGA packages, regarding existing pick-and-place equipment, standard solder reflow assembly, and PCB techniques.

Revision history

Table 6. Document revision history

Date	Revision	Changes
June-2002	1	First issue
January-2004	2	Lead free information added
25-May-2004	3	Mechanical description notes updated on page 2
15-Sep-2006	4	Reformatted to current standard.
15-Oct-2006	5	Added *section 5.4.1 on Rework procedure*.
09-Mar-2010	6	Updated bump composition in *Section 1: Product description* and *Section 2: Mechanical description*. Updated solder paste composition in *Section 5.2: PCB assembly guidelines*.
06-Sep-2011	7	Updated references to standards. Added *Figure 6*. Updated reel label in *Figure 8*. Updated soldering reflow profile in *Figure 9*.
19-Oct-2012	8	Corrected typographical error in *Figure 9*. Restructured *Table 4*
13-Feb-2026	9	Updated Section 4.2: PCB assembly guidelines. Minor text changes.

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