STV3550

LCD and Matrix Display Integrated Up-convertor with 32-bit CPU

DATA BRIEF

FEATURES

- Fully-programmable digital video output stage for direct rgb interface to flat display panel with 4- to 10-bit color resolution and pixel resolution from VGA to WXGA including HDTV2.
- Versatile integrated up-converter
  - 50/60-Hz progressive output with line-interpolation: (A + A*), field-merging (A + B) or with motion-adaptive de-interlacing based on median f(A, B)
  - Advanced still picture modes: AA*AA* and ABAB interlaced or AAAA non-interlaced
  - Automatic movie mode detection and scanning
- Standard definition input
  - ITU-R BT.656/601 video input
  - Separate H/V inputs synchronous with input clock
  - 3D temporal noise reduction with comet-effect correction
  - Movie mode detection with motion phase recovery
  - Scene-change detector for contrast enhancer and up-conversion control
  - Letterbox format detection and auto-format correction
- High-quality video display
  - Picture structure improvement including: color transition improvement, Luma peaking/coring and Luma contrast enhancer
  - H/V format conversion with zoom in/out (4x to 1/8x) with H/V decimation
  - Letterbox and 4:3 to 16:9 format conversion with programmable 5-segment panoramic mode
  - Very flexible Sync generator for master and slave modes by Vsync and Hsync signals generation
  - Progressive display mode (60 Hz, 50 Hz) for full-screen graphic planes
  - Mosaic mode with up to 16 pictures displayed
  - Picture compositor to provide transparency mode between video and graphic planes
  - Gamma correction
- High-performance 8-bit bitmap OSD generator
  - Pixel-based resolution with 10-bit RGB outputs
  - Programmable resolution up to WXGA, all standard displays are supported: teletext 1.5 (480x520) and 2.5 (672x520), double-page teletext (960x520) with picture-and-text, teleWeb (640x480)
  - 4 graphic planes with full alpha-blending capabilities: 24-bit background plane, 10-bit RGB video plane, bitmap OSD plane with color map, up to 128 x 128 pixel cursor plane
  - 2D graphics accelerator
- Embedded 32-bit ST20 CPU core
- Peripherals and I/Os for TV chassis control:
  - 30 fully-programmable I/Os (5V tolerant)
  - 4 external interrupts,
  - 8-bit programmable PWM with 4 inputs/outputs
  - Infrared digital preprocessor
  - Real time clock and watchdog timer
  - Four 16-bit standard timers
  - 10-bit ADC with 6 inputs and wake-up capability
  - 2 Master/slave I²C bus interfaces
  - UART and support for IrDA interfaces
- Teletext 1.5 and 2.5, closed-caption, VPS and WSS VBI data decoding, TeleWeb compliant
- Embedded emulation resources with in-situ flash programming capabilities
- 1.8V and 3.3V power supplies

- Eco standby mode
- 27-MHz crystal oscillator
- PC input compatible

DESCRIPTION

This integrated circuit (IC) is dedicated to flat panel display TV chassis. Combined with a digital multi-standard video decoder (STV2310) delivering an ITU-R BT.601/656 video stream, it provides a cost-effective, high-performance solution for plasma or LCD TV applications. The STV3550 includes an up-converter, a 32-bit ST20 CPU core with all peripherals required for controlling the TV chassis. Teletext data is extracted from the incoming stream and decoded by the CPU. An embedded On-Screen Display (OSD) generator delivers the text and graphics. The Video Display Pipeline performs feature box image processing such as picture improvement, horizontal and vertical rescaling and Temporal Noise Reduction.

The chip operates with an external SDRAM that is used for the field-rate up-conversion and text and graphic generations.The external SDRAM can be configured as a single bank of 16/64/128 Mb (16-bit configuration) or a dual bank of 16/64 or 128 Mb (32-bit configuration). Application program codes are stored in an external Flash memory.

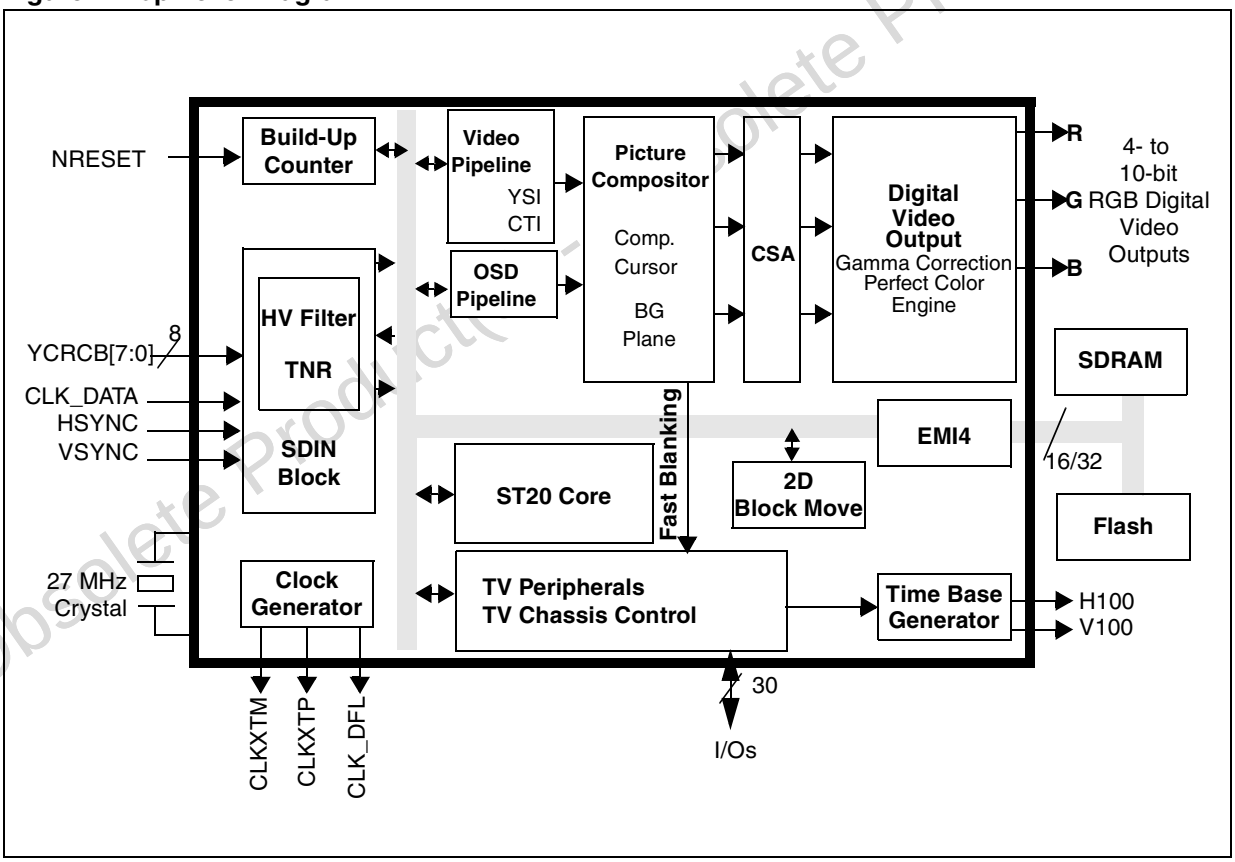
The STV3550 is designed using an 0.18 micron CMOS process and delivered in a 208-pin PQFP (0.5 mm pitch) package.

The STV3550 completes the Digital IC Core family (STi5xxx, STi7xxx) which offers common CPU and software platforms based on STMicroelectronics' 32-bit ST20 CPU core. This device, which is specifically designed for plasma or LCD TV applications, is completely compatible with the architecture and software of the STV3500 CTV100-CRT platform that targets CRT-based TV chassis.

Table 1. Order Codes

Part Number	Description
STV3550	Device in low-cost 0.65 mm pitch PQFP 160 package

Figure 1. Top Level Diagram



REVISION HISTORY

Table 2. Revision History

Date	Revision	Description of Changes
November 2004	1	First Issue