



## STF24NF12

N-channel 120V - 0.070Ω - 24A TO-220FP  
Low gate charge STripFET™ II MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STF24NF12	120V	<0.077Ω	24A

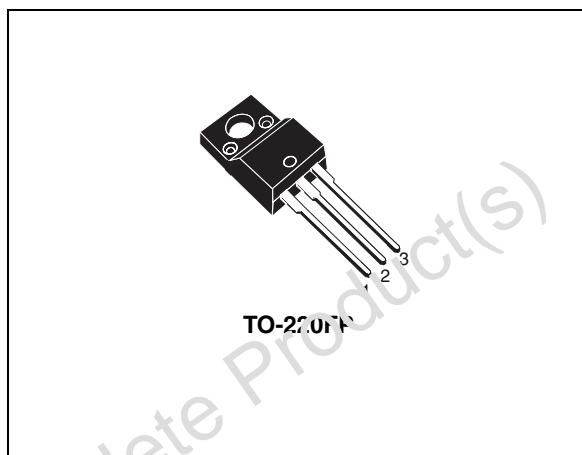
- Exceptional dv/dt capability
- Low gate charge at 100°C
- Application oriented characterization
- 100% avalanche tested

### Description

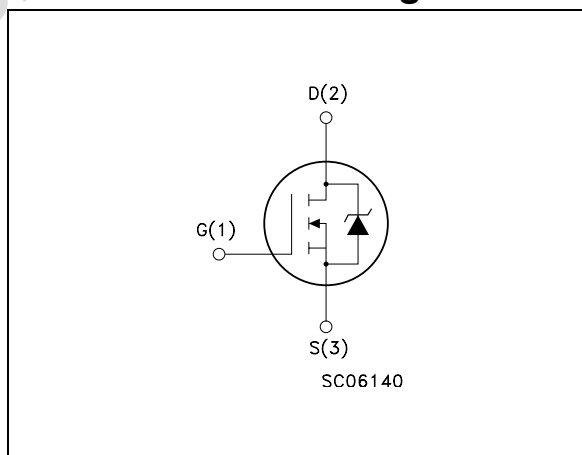
This MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STF24NF12	F24NF12	TO-220FP	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	120	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	24	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	13	A
$I_{DM}^{(2)}$	Drain current (pulsed)	96	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	30	W
	Derating Factor	0.2	W/°C
$dv/dt^{(3)}$	Peak diode recovery voltage slope	3	V/ns
$E_{AS}^{(4)}$	Single pulse avalanche energy	220	mj
$T_J$	Operating junction temperature	-55 to 175	°C
$T_{stg}$	Storage temperature		

1. Pulse with limited by safe operating area
2. Pulse width limited by safe operating area
3.  $I_{SD} \leq 24\text{A}$ ,  $di/dt \leq 600\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{J,MAX}$
4. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 12\text{A}$ ,  $V_{DD} = 30\text{V}$

**Table 2. Thermal data**

$R_{thj-case}$	Thermal resistance junction-case Max	5	°C/W
$R_{thj-a}$	Thermal resistance junction-ambient Max	62.5	°C/W
$T_l$	Maximum lead temperature for soldering purpose	300	°C

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}C$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	120			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 12A$		0.070	0.077	$\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15V, I_D = 15A$		10		S
$C_{iss}$	Input capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		870		pF
$C_{oss}$	Output capacitance			125		pF
$C_{rss}$	Reverse transfer capacitance			50		pF
$Q_g$	Total gate charge	$V_{DD} = 80V, I_D = 24A$		30	72	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10V$		6		nC
$Q_{gd}$	Gate-drain charge	(see Figure 13)		10		nC

<sup>(1)</sup> Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 50V, I_D = 12A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12)		60		ns
$t_r$	Rise Time			45		ns
$t_{d(off)}$	Turn-off-delay time	$V_{DD} = 50V, I_D = 12A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12)		50		ns
$t_f$	Fall time			20		ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				13	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				96	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=24A, V_{GS}=0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD}=24A,$ $di/dt = 100A/\mu s,$ $V_{DD}=30V, T_j=150^\circ C$ (see Figure 14)		100		ns
$Q_{rr}$	Reverse recovery charge			375		nC
$I_{RRM}$	Reverse recovery current			7.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

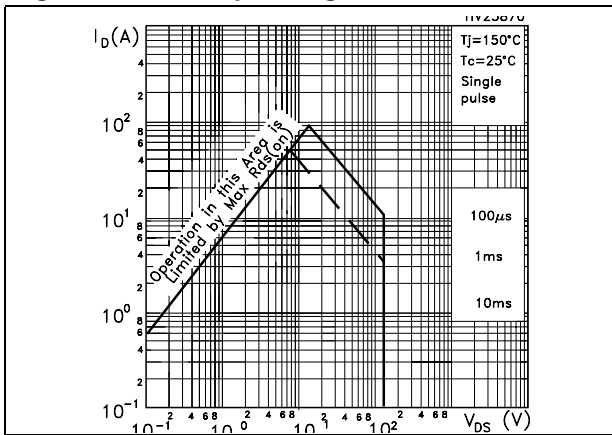


Figure 2. Thermal impedance

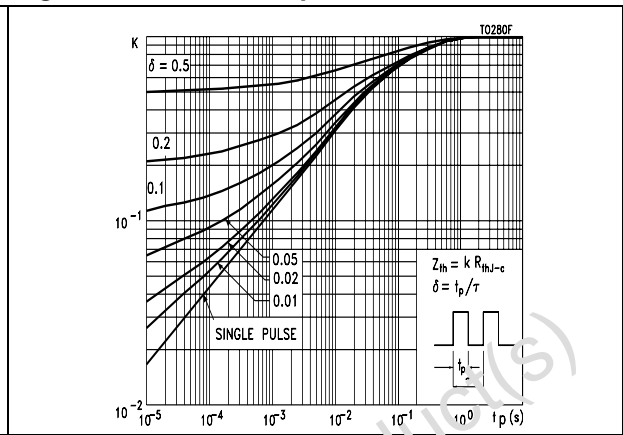


Figure 3. Output characteristics

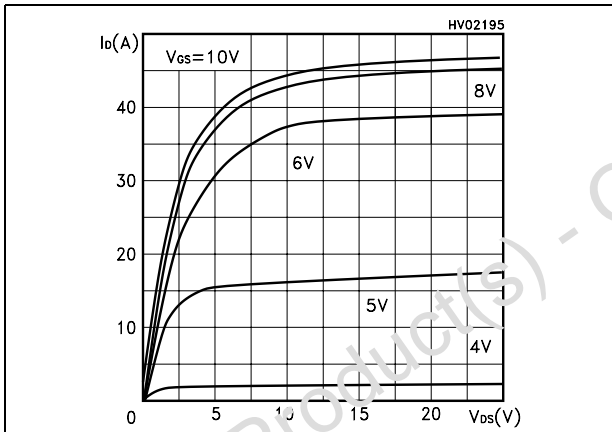


Figure 4. Transfer characteristics

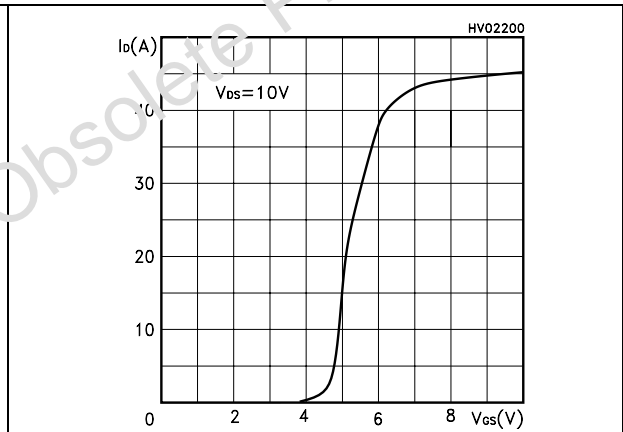


Figure 5. Transconductance

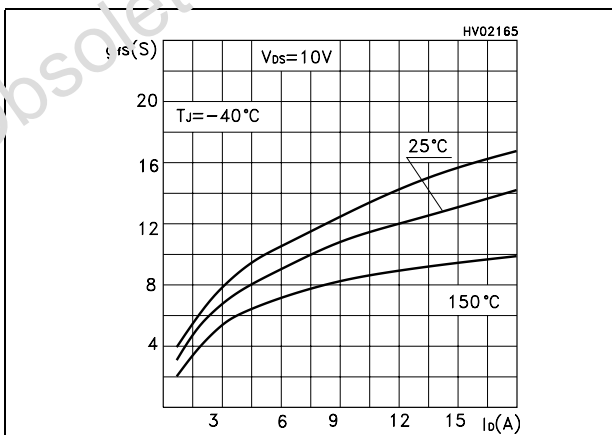


Figure 6. Static drain-source on resistance

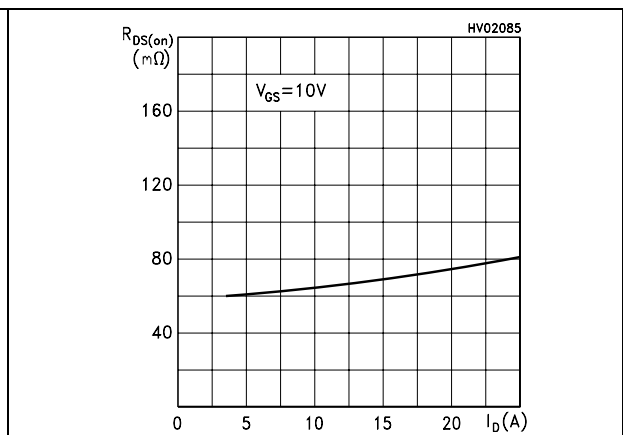


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

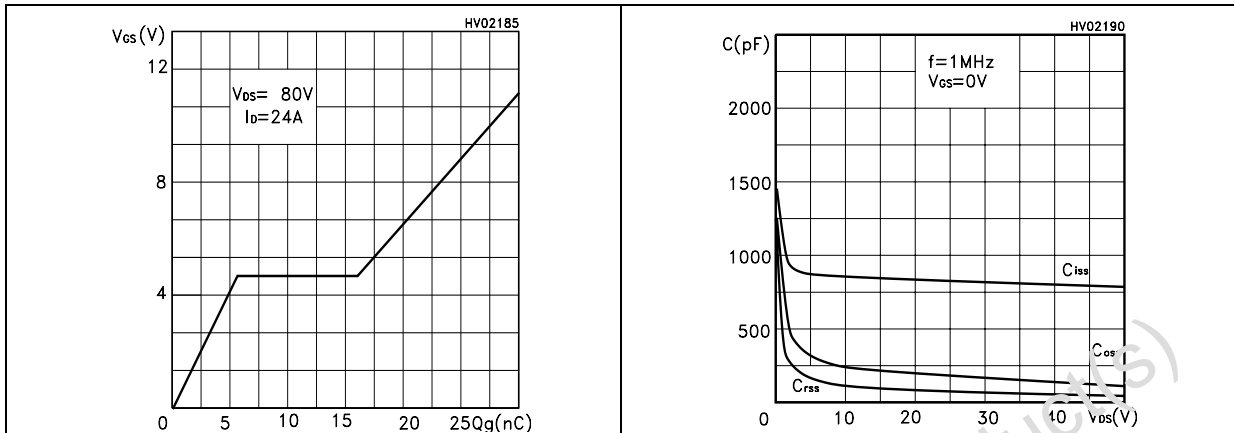


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

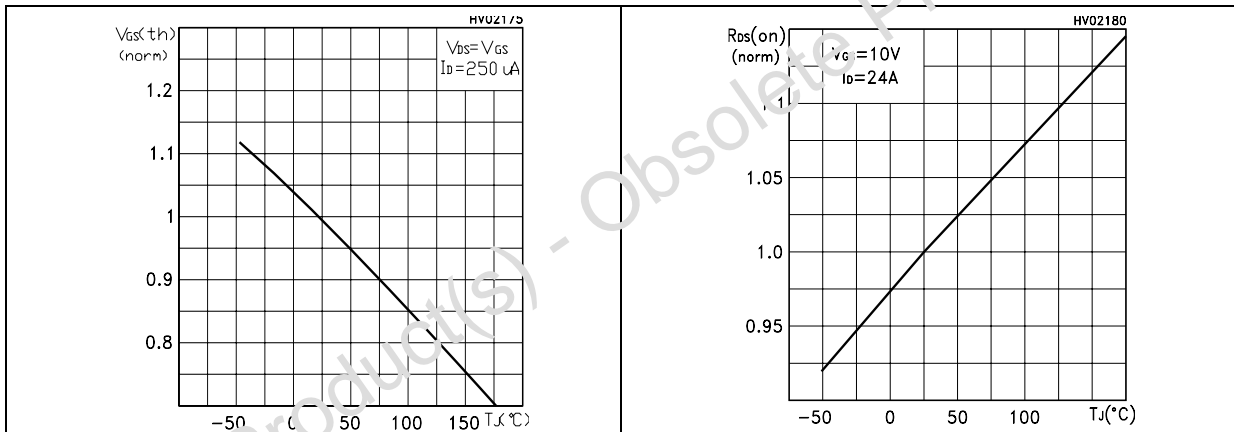
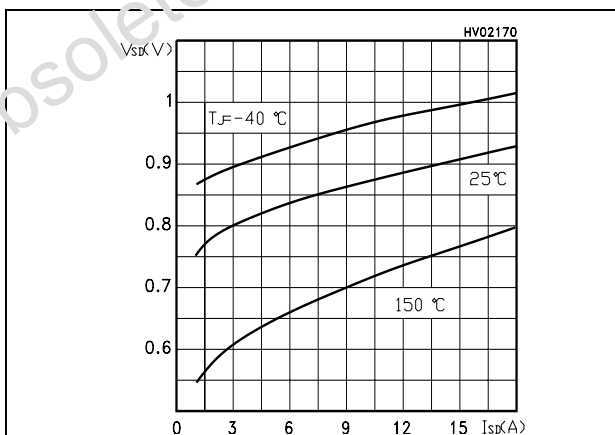


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

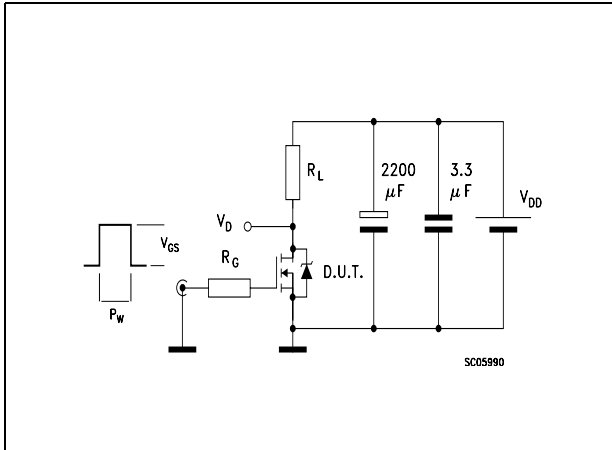


Figure 13. Gate charge test circuit

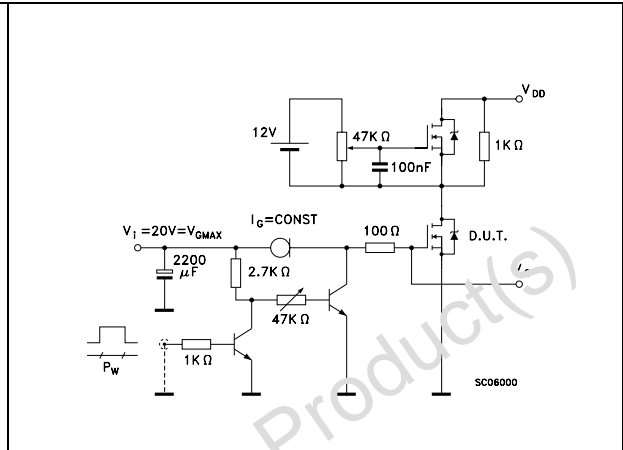


Figure 14. Test circuit for inductive load switching and diode recovery times

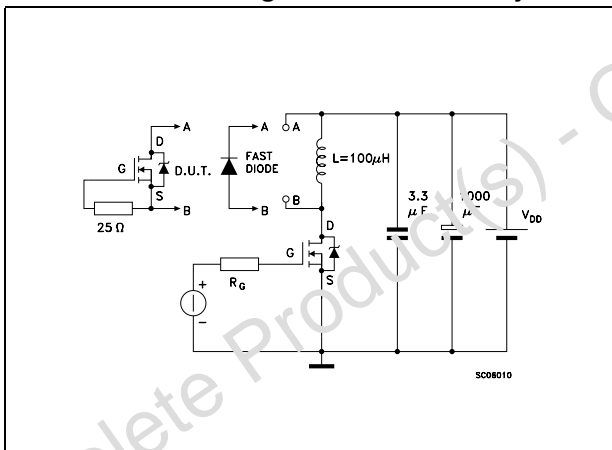


Figure 15. Unclamped Inductive load test circuit

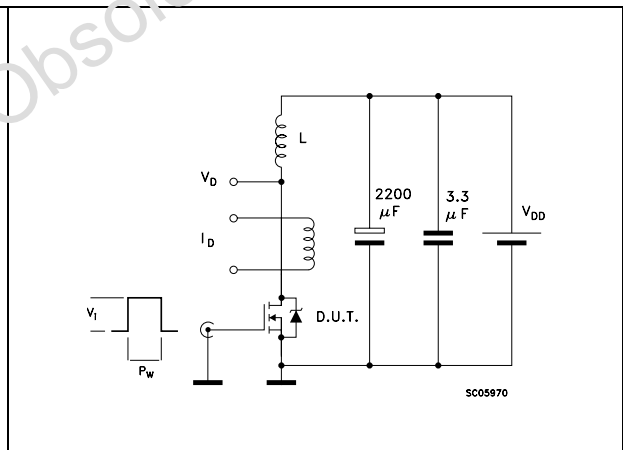


Figure 16. Unclamped inductive waveform

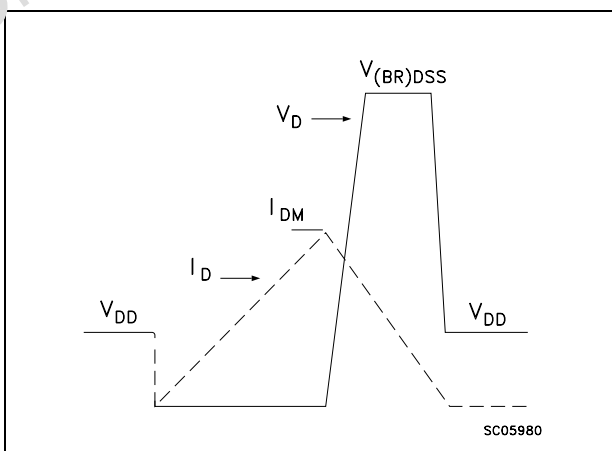
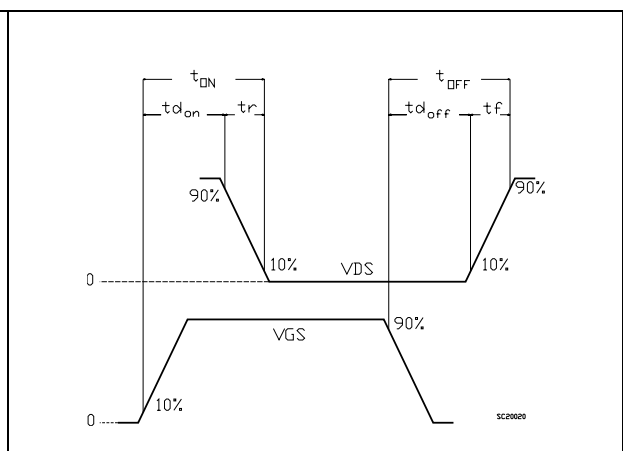


Figure 17. Switching time waveform



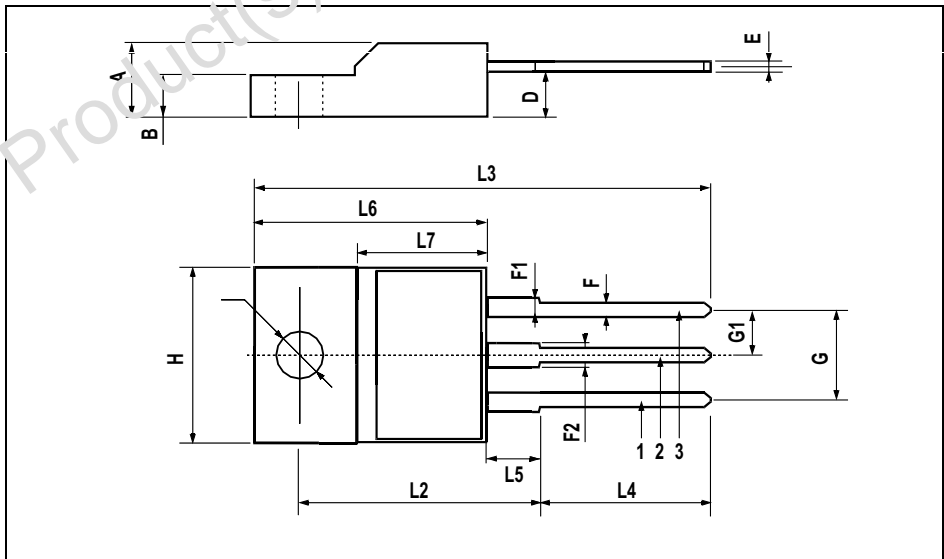
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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**TO-220FP MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



## 5 Revision history

Table 7. Revision history

Date	Revision	Changes
31-may-2005	1	First issue
04-Sep-2006	2	New template, no content change

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