

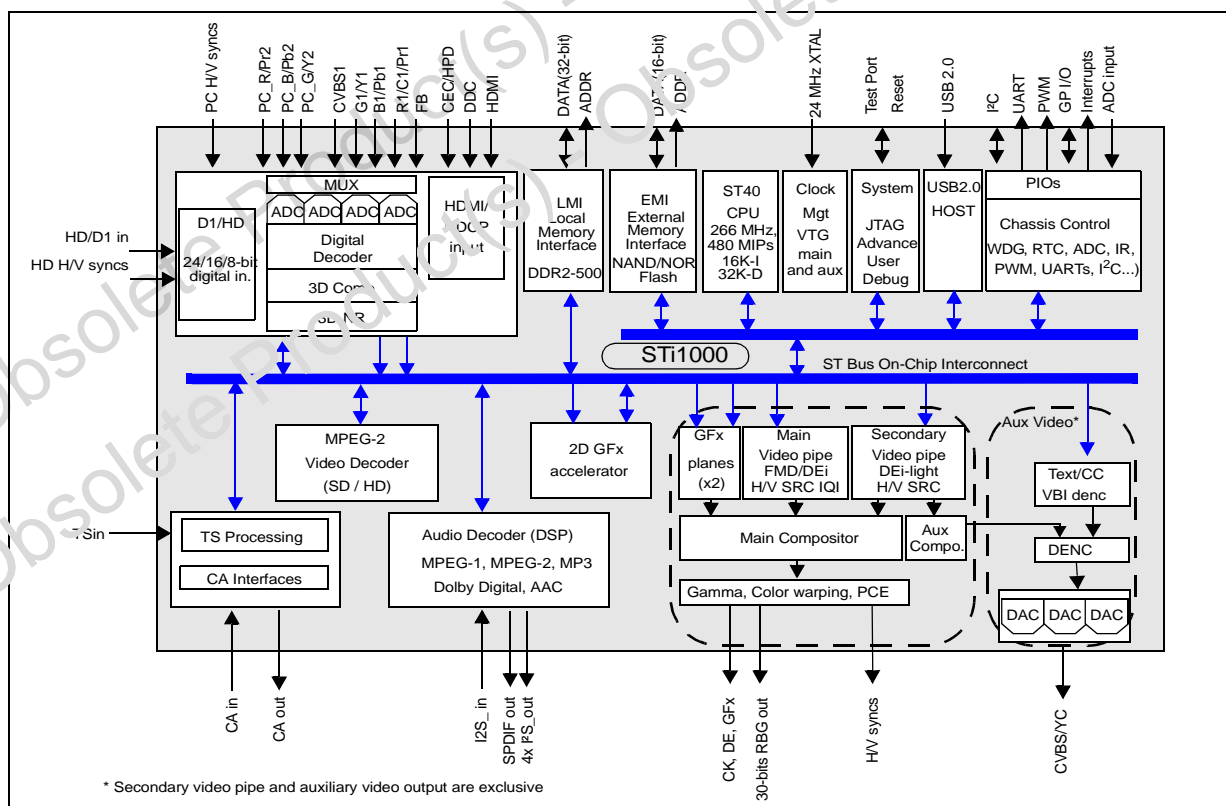
Single-chip worldwide iDTV processor

Data Brief

Features

The STi1000 is a single-chip worldwide iDTV Processor that includes:

- 32-Bit RISC ST40 CPU, 266 MHz, 480 MIPs
- DDR2 unified memory interface, 250 MHz clock
- Transport stream demultiplexer with DES, DVB and Multi2 descrambler
- CableCard and DVB-CI interface
- MP@ML and MP@HL MPEG-2 video decoder
- 24-bit audio DSP core, MPEG-1(layers 1,2,3), MPEG-2, MPEG-2-AAC, Dolby® Digital, MP3 decoder
- Analog video input: CVBS, SVHS(Y/C), Component (from SD up to HD 720p, 1080i, 1080p)
- PC input, analog RGB up to UXGA/60 Hz (162 MHz sampling frequency)
- 24-bit digital video input, up to 1080p and UXGA/60 Hz
- HDMI/HDCP input, RGB/YCrCb up to 1080p, UXGA/60 Hz, support stereo and 5.1 multi-channel audio. Compliant with HDMI 1.3, DVI 1.0, HDCP v1.1
- USB2.0 high speed interface (480 Mbits/s)
- High definition video processor
- Multi-standard color decoder (PAL/SECAM/NTSC), with 3D comb filtering in NTSC and PAL, Luma and Chroma spatio-temporal (3D) noise reduction
- Double video pipe for Picture In Picture (PIP) display
- 2D graphic accelerator and enhanced true color on screen display. Bitmap OSD generated at native resolution
- Video and graphic composition for Picture And Text (PAT), Picture And Graphic (PAG), mosaic
- Exhaustive set of peripherals for DTV chassis control
- Flat panel display video output, up to 1920 x 1080p resolution



1 Description

The STi1000 is a highly-integrated, high-performance System-on-Chip (SoC) iDTV processor that is compliant with worldwide digital TV standards such as ATSC (US), DVB (Europe), ARIB (Japan), DMB-TH(China) and with PAL/SECAM/NTSC analog TV standards.

The STi1000 provides a cost-optimized solution for iDTV (basic TV platform DTV150), with a minimum number of external components, 32-bit unified DDR2 memory interface for CPU, OSD, video.

The STi1001 version permits low-cost iDTV implementation with a single 16-bit DDR2 memory interface.

The STi1000 can receive analog and digital TV signals from transmissions through a cable or satellite tuner, and from external video sources such as DVD players, STB, PVR, and PC. It allows low-cost implementation of matrixed-display integrated Digital TV, including HDTV LCD, Plasma Panel Display (PPD), Rear Projection TV (RPTV) and Digital Light Processing (DLP) RPTV up to 1920 × 1080p resolution.

The STi1000 provides up to 30-bit digital RGB output, with programmable Line and Pixel output formats (including 1366 × 768 and 1920 × 1080 resolution), CVBS and YC output from digital PAL/SECAM/NTSC encoders.

The STi1000 supports the decoding and processing of Standard Definition (SD) and High Definition (HD) analog and digital video sources; and the decoding and processing of digital audio from stereo up to 5.1 audio channels. It also provides high-performance video processing for:

- 3D Comb Filter for NTSC and PAL standards
- 3D noise reduction
- Automatic film mode detection: automatic letter box detection, 3:2 pull-down, interlaced/progressive modes and scene change detection
- 3D motion adaptive, pixel-based, advanced deinterlacing with diagonal compensation and contour-sensitive de-interlacing CSDiTM
- Horizontal and vertical scaling
- Image quality improvement, including 10-bit resolution (up to 12-bit processing), LTI, CTI, horizontal and vertical peaking, automatic contrast enhancement, automatic color enhancement
- Flexible H/V scaling
- Picture-in-Picture (PIP) display

The STi1000 supports high-quality bitmap graphic display, multi-plane on screen display (OSD) generated at display panel resolution.

The STi1000 permits the development of Integrated Digital TV (iDTV) applications with services such as US Closed Caption, US Vchip, Teletext, DVB-subtitles, EPG, and middleware such as MHEG-5 and MHP. It supports conditional access for US (open cable CableCard, Europe (DVB-CI) and Japan (ARIB Conditional access).

Figure 1. US basic FPD iDTV

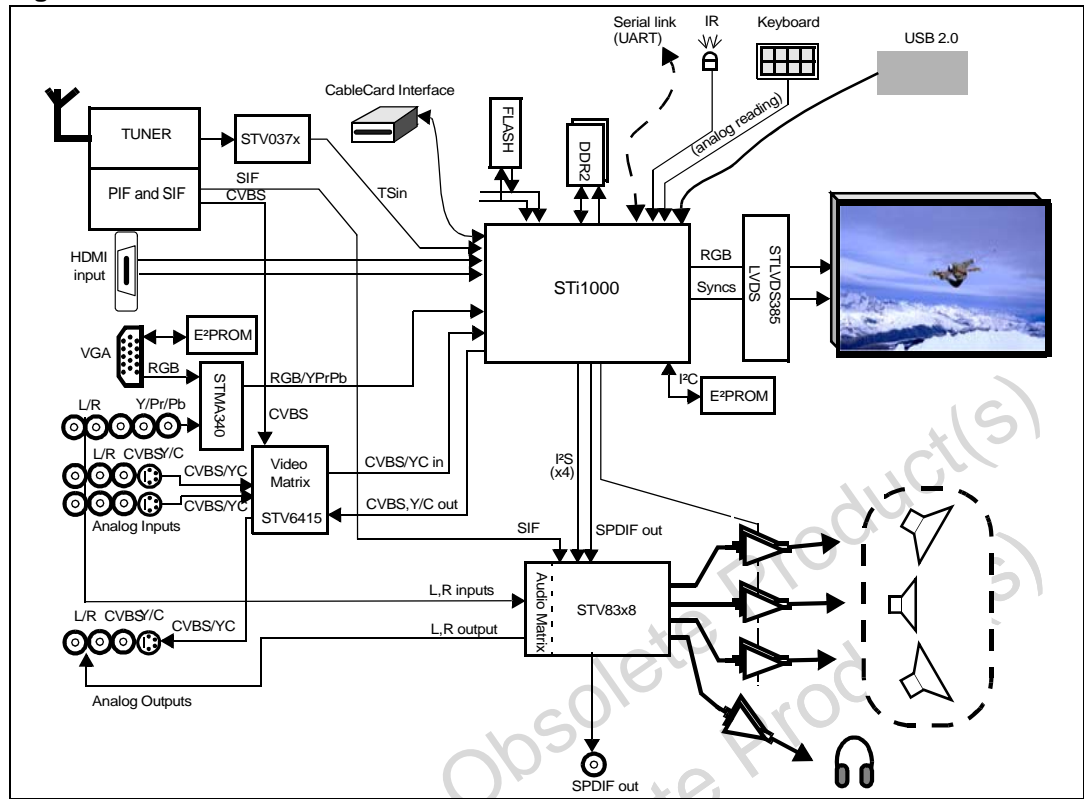
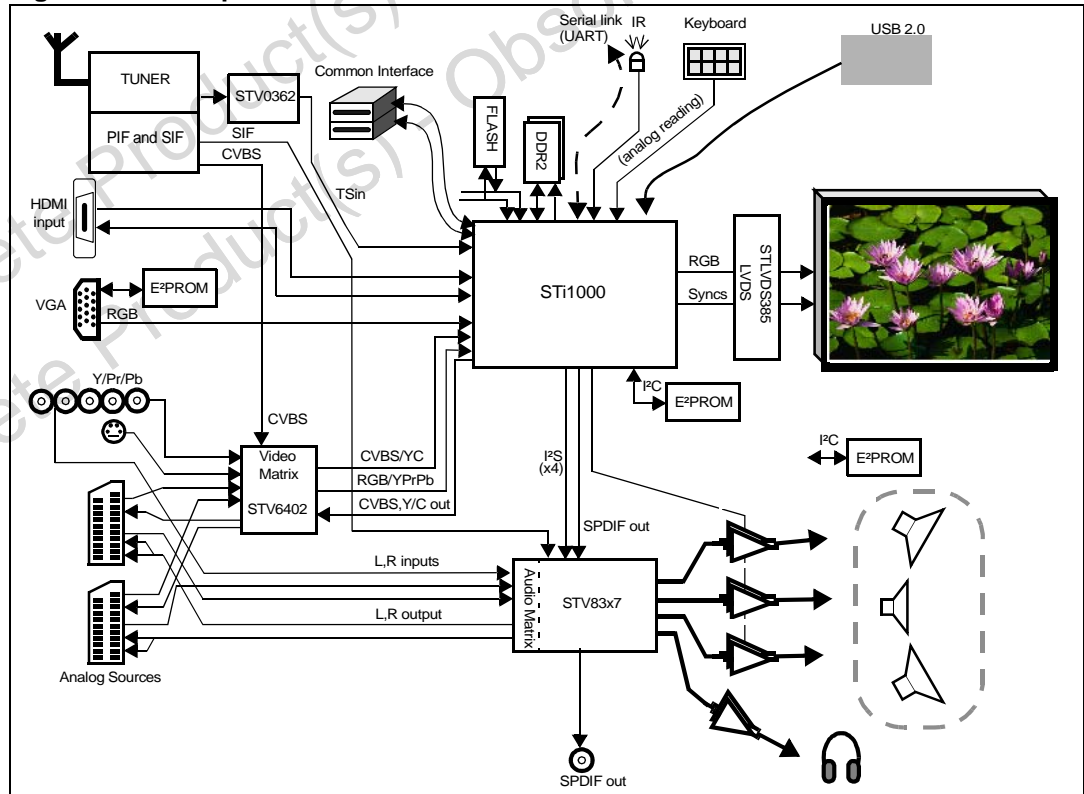


Figure 2. European basic FPD iDTV



Package: The STi1000 uses a PBGA 532 + 36, 35 x 35, 4L package.

Table 1. Package information

Package type	PBGA	Unit
Body size	35x35	mm
Ball pitch	1,27	mm
Ball count	568	balls
Ball matrix	26x26 - 7 row perimeters (532)	balls
Center matrix	6x6	balls
Substrate	4	layers

2 Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Oct-2007	1	Initial release.

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