STE08PSP

08-channel high-power integrated PSE line manager

Preliminary Data

Features

- Full programmable power sourcing equipment (PSE) power control device
- Supports up to 8 independent high-power (up to 50 W) channels, no need for external FET
- Low cost small size TQFP80 14 x14 exposed pad slug down plastic package
- Wide operating range: up to 90 V
- Legacy POE+ capable, with double current limitation (Standard 802.3af or POE+)
- IEEE 802.3at pre-standard compliant
- Auto EEPROM download for parameter setting
- Global power management for smart power sharing between different controllers
- Enhanced integrated system power management algorithm with dynamic power allocation
- Automatic setting of power budget according to battery level (3 batteries supported)
- Independent per-port power settings (also runtime configurable)
- Current sensing with external resistor down to 500 mΩ
- In-Rush current control, short circuit protection with folding, overload
- Open circuit detector: AC and DC methods
- On-chip options
  - 3.3 V SMPS controller
  - 3.3 V linear regulator
- Low noise 12-bit A to D converter
- Standard slave I2C interface for communication with host (Primary I2C)
- Master/slave I2C (Secondary I2C) for intra-system communication
- Full support of RFC3621 MIB

TQFP80 exposed pad
14 mm x 14 mm

- Contiguous channel power consumption registers for easy I2C reading
- Parallel monitor interface to ease channel operation monitoring
- 3-level detection with signature resistance linearity check
- Customizable signature detection capability with double signature detection distinct windows (IEEE or legacy)
- Multiple classification attempt (MCA) programmable structure

Applications

- Ethernet switches/routers
- Midspan power supplies
- IP-PBX

Description

The STE08PSP architecture provides a complete PSE interface and a smart digital controller to efficiently manage all the functions in a high-power POE system (up to 45 W) with port counts up to 64 without any host controller.

Contents

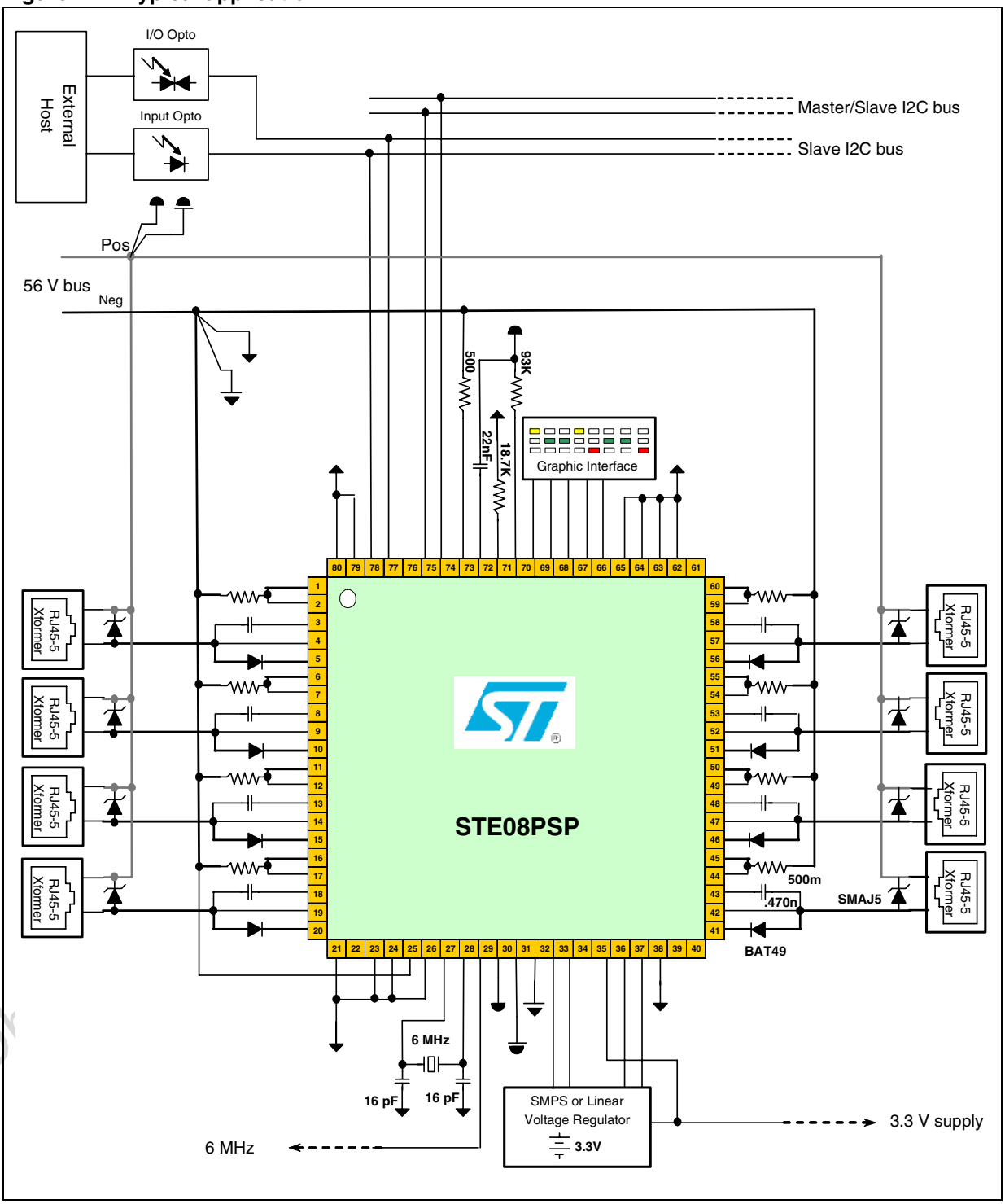
1 Acronyms and definitions

Table 1. Acronyms and definitions

Acronym	Definition
ADC	Analog-to-digital converter
DSP	Digital signal processor
FSM	Finite state machine
GPM	Global power management.
IEEE802.3af	IEEE Standard for information technology – Telecommunication and information exchange between systems – Local and metropolitan area networks – Specific requirements.
IEEE802.3at	Draft standard for information technology – Telecommunication and information exchange between systems – Local and metropolitan area networks – Specific requirements.
RFC3621 MIB	Document that defines a portion of the Management Information Base (MIB) for use with network management protocols.
PAvail	Available Power: instant available system power. (PAvail=PBudget – Pgap –Pused)
PBudget	Budged power: total system power available.
PD	Powered device.
PGap	Power gap: Power guard used in GPM algorithms.
PNew	New Power requested by a new valid connected PD.
POE	Power over ethernet.
POE+	Power over ethernet (higher than 15 W that is defined in IEEE802.3at).
PSE	Power sourcing equipment.
PUsed	Power used: Instant power used, sum of PDs requested power or sum of PDs instant power.
SMPS	Switched mode power supply.

2 Application diagram

Figure 1. Typical application



3 Block diagram

Figure 2. Functional block diagram

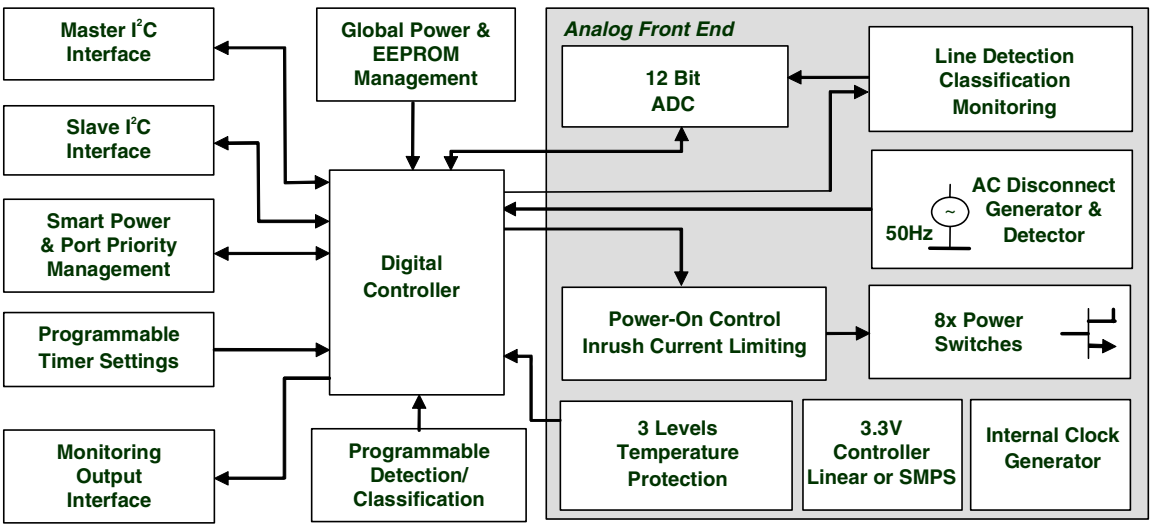
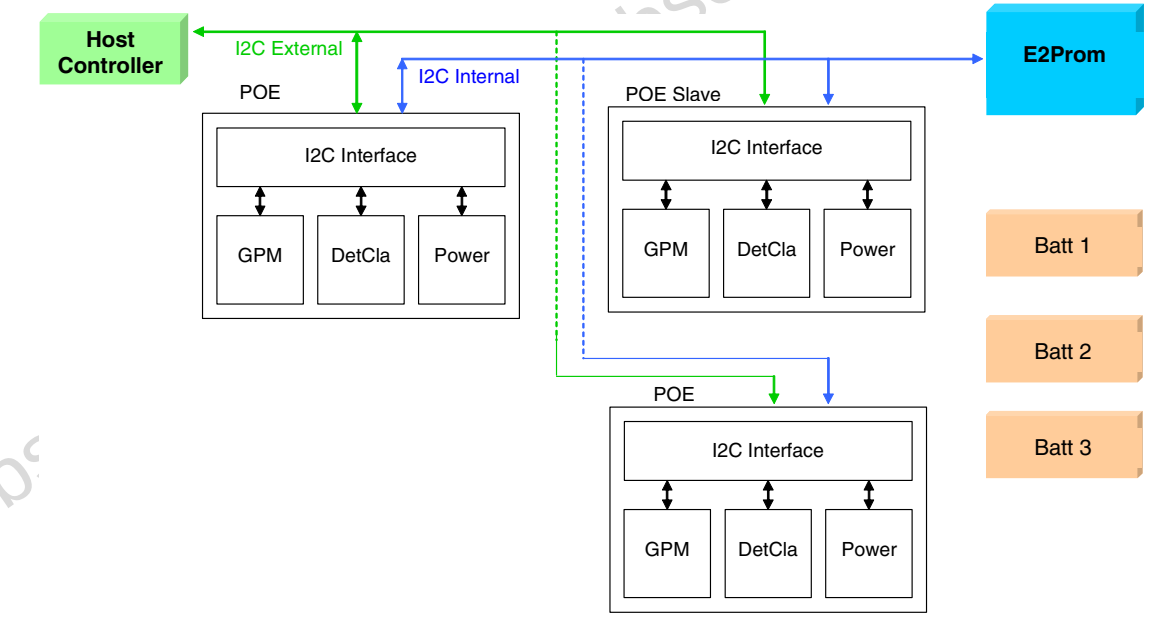


Figure 3. Typical multi-port application diagram



4 Pin description

Figure 4. View through package

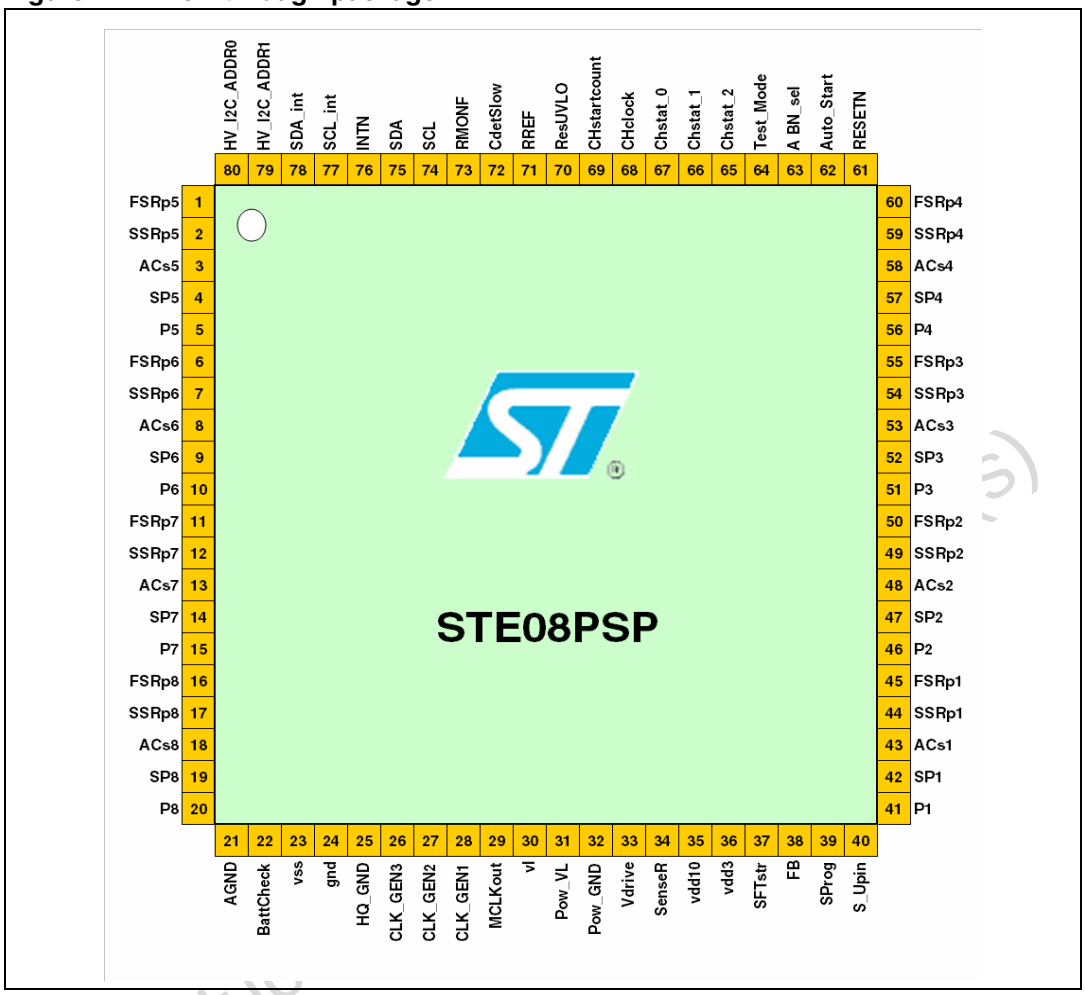


Table 2. Pin description

Pin #	Pin name	I/O	Function
Power and ground pins			
21	gnd, AGND	I	Analog grounds
23	vss	I	Digital grounds
25	HQ_GND	I	High quality ground Kelvin sensing
32	POW_GND	I	Linear or SMPS 3.3 V regulator power ground
31	POW_VL	I	+48 V battery voltage for linear or SMPS 3.3 V regulator
36	Vdd3	I	3.3 V power supply
35	Vdd10	IO	10 V power supply. (internally generated 8.6 V typ. or external 10 V min)
30	VL	I	Battery voltage
Analog pins			
72	CdetSlow	O	Detection rise/fall time capacitor (up to 25 nF). Tr/f customizable from 1ns to 4 ms
34	SenseR	O	3.3 V regulator current limiting reference resistor (100 mΩ for SMPS 3.3 Ω for linear)
33	Vdrive	O	External p-channel MOSFET gate driving voltage for SMPS. It provides a square wave with VL as upper limit and (VL-10 V) as lower limit voltage
37	SFTstr	O	SMPS switched mode power supply soft start capacitor. 200 nF. Or external NPN base driving in case of 3.3 V linear regulator
38	FB	IO	SMPS (switched mode power supply) feedback pin. Cfb = 2.2 nF
20	P8	O	Drain Power DMOS. If switched on activates channel 'x'. x= 1 to 8
15	P*7*		
10	P*6*		
5	P*5*		
56	P*4*		
51	P*3*		
46	P*2*		
41	P*1*		

Table 2. Pin description (continued)

Pin #	Pin name	I/O	Function
Analog pins (continued)			
18	ACs8	O	Provides a 50 Hz sinusoidal AC disconnection signal for port 'x'. x= 1 to 8
13	ACs7		
8	ACs6		
3	ACs5		
58	ACs4		
53	ACs3		
48	ACs2		
43	ACs1		
19	SP8	I	Detection Classification and AC disconnection sensing port 'x'. x= 1 to 8
14	SP7		
9	SP6		
4	SP5		
57	SP4		
52	SP3		
47	SP2		
42	SP1		
17	SSRp8	I	Line current to the monitoring resistor for channel 'x'. x= 1 to 8. Allowed values are 0.5 or 1 (see also Sprog preset pin). Sensing pin.
12	SSRp7		
7	SSRp6		
2	SSRp5		
59	SSRp4		
54	SSRp3		
49	SSRp2		
44	SSRp1		
16	FSRp8	O	Source power DMOS connected to the sense resistor. Forcing pin.
11	FSRp7		
6	FSRp6		
1	FSRp5		
60	FSRp4		
55	FSRp3		
50	FSRp2		
45	FSRp1		
73	RMONF	O	Mirror monitoring resistance (1000*SenseR) pin to let the internal ADC evaluate the line currents

Table 2. Pin description (continued)

Pin #	Pin name	I/O	Function
Analog pins (continued)			
71	RREF	I	Reference biasing resistor 18.7 kΩ
28	CLK_GEN1	I	Crystal Oscillator pin1 for high performance clock generation
27	CLK_GEN2	I	Crystal oscillator pin2 for high performance clock generation
26	CLK_GEN3	I	Low profile clock input pin or clock input pin in multi device configuration
29	MCLKout	O	Master clock output for multi device configuration.
22	BattCheck	I	Sensing pin for battery check
Digital pins			
61	RESETN	I	Reset pin. Active low
STATUS flag interface			
69	CHstartcount	O	Indicates the beginning of the scanning (ch1) of the channel whose status flags (Ch_stat (2:0)) are currently notified externally. The status flag notification is enabled via the configuration register Global_cfg2, STATUS_FLAG_EN bit.
68	CHclock	O	Clock signal indicating the change of the of the channel whose status flags (Ch_stat (2:0)) are currently notified. This clock is 60 * MCLKout clock cycles.
65	Ch_stat_2	O	“000” →Current channel not operating (NOP) “001” →Current channel under detection (DetClass) “010” →Current channel disconnection procedure (AC/DC discon) “110” →Current channel in fault condition (OVcurr/OVld) “100” →Current channel in normal powering mode (POK)
66	Ch_stat_1		
67	Ch_stat_0		
Configuration signals			
63	A_BN_Sel	I	A or B Alternative configuration mode select. ‘0’→Alternative B (Midspan-PSE) ‘1’→Alternative A (Endpoint-PSE)
62	Auto_Start	I	AUTO start mode enable. ‘0’→Auto Start Mode disabled: all the ports are disabled after the Reset, neither detection nor power on is performed (MODE[1:0] register selected to Power Down at the reset event) ‘1’→Auto Start Mode enabled: all the ports are automatically enabled, detection, classification and power are performed (MODE[1:0] register selected to AUTO after the reset event)
40	S/Upin	I	SMPS (switch mode power supply) mode selector bit. When Not connected (→“1”) the device works as DC-DC converter controller. 3.3 V linear regulator or external (→“0”)
39	Sprog	I	Preset pin for sensing resistor programmability. “0” →SenseR= 0.5 “1” →SenseR= 1

Table 2. Pin description (continued)

Pin #	Pin name	I/O	Function
I^2C signals			
79	HV_I2C_ADDR1	I	This defines the device address for the I2C interfaces x = 0,1
80	HV_I2C_ADDR0		
Digital pins			
74	SCL	I	Serial clock input pin for the I2C SLAVE interface. Vs HOST
75	SDA	I	Serial data pin for the I2C SLAVE interface. Vs HOST
76	INTN	O	I2C Open drain output that goes low when interrupt event is notified
77	SCL_int	I	Serial clock input pin for the I2C MASTER/SLAVE interface. For internal communication
78	SDA_int	I	Serial data pin for the I2C MASTER/SLAVE interface. For internal communication
Test mode signals			
64	TEST_MODEx	I	Test Mode Enable “0” →Functional mode “1” →Reserved

5 General description

The STE08PSP is designed to supply power over multiple Ethernet channels, thus avoiding the need for different individual power supplies. It is designed for applications such as Web cams, IP Phones, Bluetooth access points and WLAN access points.

The equipment providing the power to the twisted-pair cabling is referred to as power sourcing equipment (PSE). The main functions of the PSE are to:

- to look for links to a powered device (PD)
- to classify a PD, to supply power to the link
- to monitor power on the link
- to remove power from the link.

Due to its enhanced power capabilities the STE08PSP can drive PD devices demanding currents that exceed IEEE802.3af.

The STE08PSP is fully programmable, supporting the detection and powering of IEEE802.3at (pre-standard draft) as well as legacy PDs.

The STE08PSP allows easy and cost-effective POE system design due to its secondary Master/Slave I2C STE08PSP that can interact with up to 7 additional PSE devices to easily build a multi-port system with up to 64 ports.

This configuration can be managed without any additional host processor since one of the STE08PSP acts as Master of the system.

The STE08PSP can detect the presence of an external EEPROM and auto-download the whole system setting.

When needed, the STE08PSP can manage efficiently cases or applications where a limited amount of power is available to the ports (global power manager).

All operations are controlled via the Primary I2C bus. The status condition of some ports is also notified externally via dedicated pins.

Ethernet port isolation is easy to maintain by means of an integrated 3.3 V (SMPS or linear regulator) power source and opto-couplers.

The STE08PSP has two multilevel address selection inputs to assign up to 16 possible addresses. Power can be provided to the PD by using either the spare lines of the Ethernet cable or the data wires, as specified by IEEE 802.3af/at.

6 Functional description

The STE08PSP architecture provides a complete PSE interface and a smart digital controller for efficient management all the functions in a high-power PoE system (up to 45 W) with port counts of up to 64, without any host controller.

The STE08PSP is designed to control the power delivery on up to 8 separate lines and autonomously co-operate with another 7 devices (GPM) and boots from EEPROM.

Each device controls 8 integrated MOS transistors on the low side of the line, monitoring the line voltage and sensing the line current by means of external resistors (one per port). Turning a port on means switching the relevant MOS that controls the inrush current, in order to increase the port voltage to up to 50 volts (typical battery voltage) after a valid PD signature has been detected. The STE08PSP also retains the advantage of the ST extended signature validation procedure which enhances the detection procedure with a linearity check of the signature resistance.

The STE08PSP's flexibility allows the user to select a proper 802.3at-ready classification strategy for high-power applications with the 5 standard classes (that can be programmed) or using up to 20 custom classes.

In addition, all operations can also be controlled through R/W registers via a standard I2C interface, and almost all the parameters can be changed at runtime allowing the user to perform custom power allocations or strategies.

The ST08PSP can also monitor the number of battery banks (up to 3), re-budgeting the available power (BATTERY CHECK functionality)

6.1 Operating modes

The digital controller can operate in one of six possible modes for all channels, selectable through the Global Configuration registers. These modes are:

- Auto
- Semi Auto
- Manual
- Stand-by
- Power Down
- Global power management (GPM).

When the reset condition is removed, the controller looks for an EEPROM for system parameter setting through the secondary I2C link. When other STE08PSP are also performing this research, this procedure is used for Master/Slave negotiation since in a multi-device system, one STE08PSP acts as master and the others as Slaves.

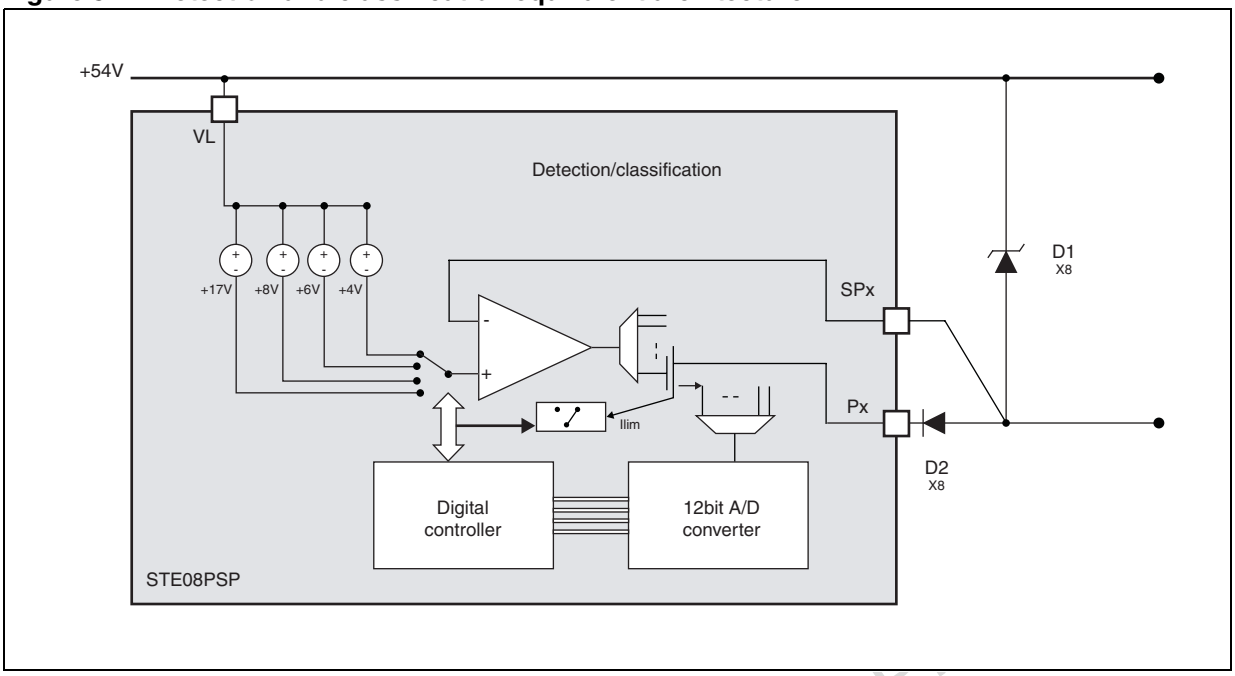
If the device is unable to boot from EEPROM, it defaults to Power Down mode if the AUTO_START pin is tied low. If AUTO_START is tied high the mode is configured in Auto mode. The mode can only be changed during a limited time interval (100 ms) after the reset is released, accessing the Global Configuration registers before the detection procedure is started, or placing the device in Stand-by mode via the I2C interface.

The characteristics of the six possible operating modes are described below:

- **STAND-BY:** the controller allows only the read/write operations suitable for changing programmability. To set this mode a reset must be initiated through the reset pin or by setting the reset bit in the REG0x05 register.
- **AUTO:** the controller autonomously performs detection, MCA classification and power_on (AF or AT) command without the need of host commands. The power and the priorities are managed locally. A subset of the status flags stored in the channel monitor registers is reported externally through the Status Flag Interface pins, allowing easy monitoring of the channel status without the presence of the host.
- **GPM Global Power management:** (This implies AUTO mode enabled). When in GPM mode the device cooperates with other STE08PSP devices (up to a maximum of 8) in order to manage the entire system power. The controller autonomously performs all the channel management, taking into account the Global Priority settings and global power consumption without needing any host command.
- **SEMIAUTO:** after a triggering command the controller autonomously performs detection and classification while waiting for a dedicated command from the host processor for the power on. Based on the detection and classification results reported in the Channels Status registers, the host controller decides whether to power on the selected channel. The disconnection of a channel is automatic as in AUTO mode, unless disabled.
- **MANUAL:** any action is performed manually. The host controller has the responsibility to force any state transition in the FSM. Based on the measures performed automatically by the ADC on several parameters, the host controller can then decide to classify the channel and afterwards issue the power-on command. The STE08PSP controller can also automatically disconnect a channel in fault condition (if not enabled, the STE08PSP automatically notifies only a short-circuit condition or a disconnection event. Overload is the responsibility of the host controller.) The host controller can also power on a channel, skipping detection and/or classification procedures.
- **POWER DOWN:** the controller is in power-down state. No actions are performed until the power down mode is removed.

6.2 Detection and classification

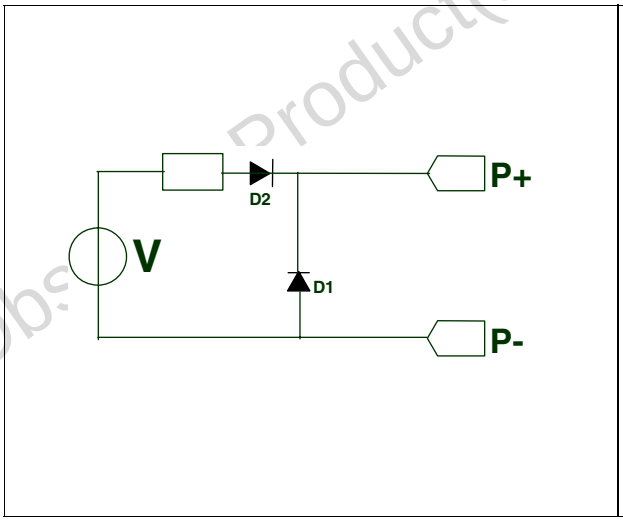
Figure 5. Detection and classification equivalent architecture

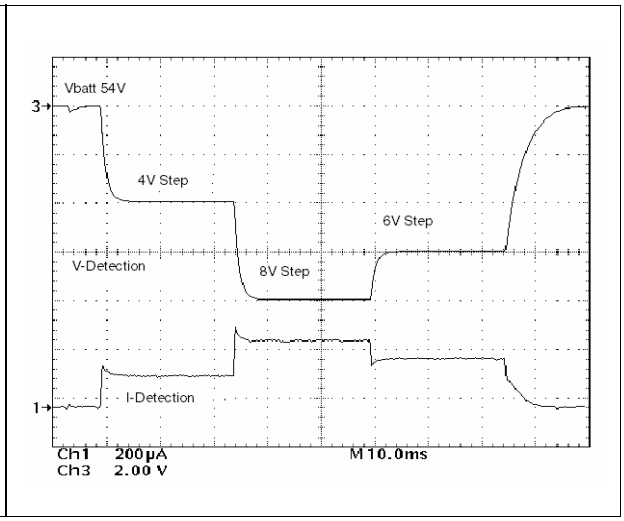


6.2.1 Detection

As shown in *Figure 7*, the STE08PSP looks for a valid PD signature by driving three different voltage levels in turn on the available free ports (4 V, 8 V and 6 V). The internal DSP calculates the slope resistance/conductance by monitoring the current difference between the 4 V and 8 V steps.

Figure 6. Detection circuit (as IEEE802.3af) **Figure 7. Detection wave @ 25 kΩ 50 pF load**





With the current measure at 6 V step, the STE08PSP also performs a linearity check which ensures that the discordance between this value and the theoretical one is less than a programmable value.

This particular (patent pending) detection sequence allows the user to gain full description of the signature impedance (signature resistance, capacitive load, drop on non-linear rectifier).

Figure 6 shows the equivalent circuit for the detection phase as defined in IEE802.3af.

Since the detection is performed by multiplexing a common voltage generator, if more than one port is connected to PDs, a delay in the start of the detection can be present. See Tdetd time in *Table 12: Electrical characteristics*.

The STE08PSP recognizes as valid a signature with the following characteristics:

- Default windows:
  - Standard 802.3af resistance slope at the port output: between 17 kΩ and 26.5 kΩ.
- Programmable windows:
  - Resistance slope can be set: between 8 kΩ and 33 kΩ (Rdl, Rdh).
- The two windows can be chosen or also combined with logical AND, OR operator.

In Midspan applications, where power is applied via spare wires, when the PSE fails to detect a PD, the port remains in high impedance, for a time at least equal to 2 s. If the signature resistance is higher than 500 kΩ the 2 s waiting is avoided (detection collision avoidance mechanism).

The transitions of the port voltage between the probing levels can be customized by the value of an external capacitor connected to the Cdetslow pin.

6.2.2 Classification

With a valid signature detected the port is probed for the classification in order to perform the smart power management (if enabled).

Figure 3 shows the default settings Classification voltage waveform, in accordance with the 802.3at pre standard draft. The STE08PSP performs two classification attempts separated by two mark events. The default behavior is composed of

V0	0 V	for	T0	3 ms
VClass1	17 V	for	TClass1	15 ms
VMark1	8 V	for	TMark	9 ms
VClass2	17 V	for	Tclass2	15 ms
VMark2	8 V	for	TMark2	9 ms

The time and the voltage for each step are programmable, the time can be set between 0 s minimum to 25 ms maximum. The voltage can be 0 V, 4 V, 6 V, 8 V or17 V.

During the classification it is possible to set the current limitation to high (70 mA) or low (1.2 mA) values, except for 17 V which is internally limited to the high value of 70 mA.

Figure 8. Classification waveform

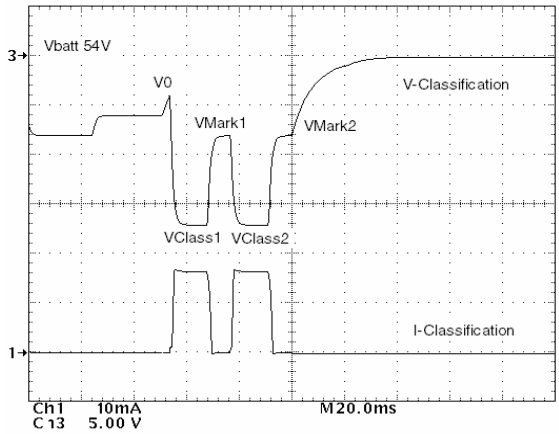


Table 3. PD power classification

Classification code	Iclass
0	I*class* <Ithcl0
1	Ithcl0< I*class* <Ithcl1
2	Ithcl1< I*class* <Ithcl2
3	Ithcl2< I*class* <Ithcl3
4	Ithcl3< I*class* <Ithcl4
0	Ithcl4< I*class*

During the two classification attempts the line current is measured and the results are stored in the Channels Monitor Classification registers.

Each current is compared with different thresholds (see *Table 4*). An attempt classification code is assigned accordingly and stored in the Channel Status registers.

The PD power class is defined by the combination of these two results and is shown in *Table 5*. where the default settings are shown.

These values can be set through the Primary I2C or EEPROM boot at up to 45 W each.

Table 4. Default setting for classification powers

Classification code	P assign (W)	802.3af 802.3at (prest.)	Note
00	15.976	Power on as AF	Standard class
11	5.045	Power on as AF	Standard class
22	8.969	Power on as AF	Standard class
33	15.976	Power on as AF	Standard class
44	37.556	Power on as AT	Standard class
01	15.976	Power on as AF	Extra class
02	15.976	Power on as AF	Extra class
03	15.976	Power on as AF	Extra class
04	15.976	Power on as AF	Extra class
10	15.976	Power on as AF	Extra class
12	1.962	Power on as AF	Extra class
13	2.803	Power on as AF	Extra class
14	3.924	Power on as AF	Extra class
20	15.976	Power on as AF	Extra class
21	5.886	Power on as AF	Extra class
23	7.007	Power on as AF	Extra class
24	8.128	Power on as AF	Extra class
30	15.976	Power on as AF	Extra class
31	10.090	Power on as AF	Extra class
32	12.052	Power on as AF	Extra class
34	14.014	Power on as AF	Extra class
40	15.976	Power on as AF	Extra class
41	19.899	Power on as AT	Extra class
42	24.944	Power on as AT	Extra class
43	29.989	Power on as AT	Extra class

6.3 Powering on

The port is powered after the classification phase.

Once activated, the power-on sequencer manages the channel's activation requests received through the signature detection circuitry. Based on the classification code the power on sequence can be set as **Power on AF** mode or **Power on AT** mode.

The incoming channel's activation requests are stored in the power-on sequencer. They are satisfied one at a time, only when the previously activated channel leaves the current limiting condition that normally occurs at power on, due to the capacitive element of the load.

A port is turned on by increasing the voltage and ramping the current up toward its upper current limit value. After a programmable time (Tinrush default value is 60 ms) if the port reaches full voltage without exceeding its current limit, it is marked as powered. The related port power bit and the power class bits are set, according to the class, in the logic interface bit stream.

The active ports are continuously monitored in order to detect a fault condition such as short circuit, disconnection or excess power (overload).

Figure 9. Power on AF sequence

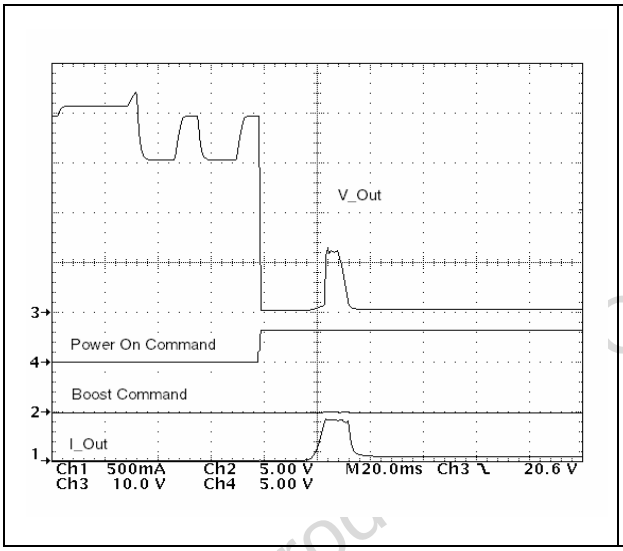
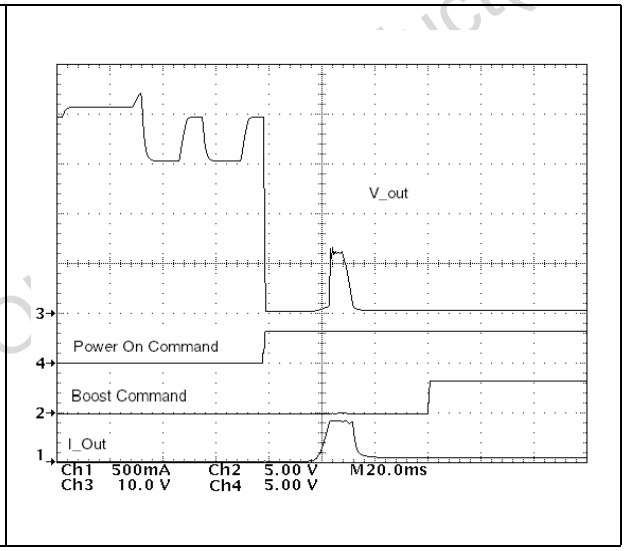


Figure 10. Power on AT sequence



6.3.1 Power on AF mode

If the classification power of the channel is lower than or equal to the AF-AT power threshold value (programmable and set as default at 19.969 W) the connected PD is switched on in the standard AF mode *Figure 9*.

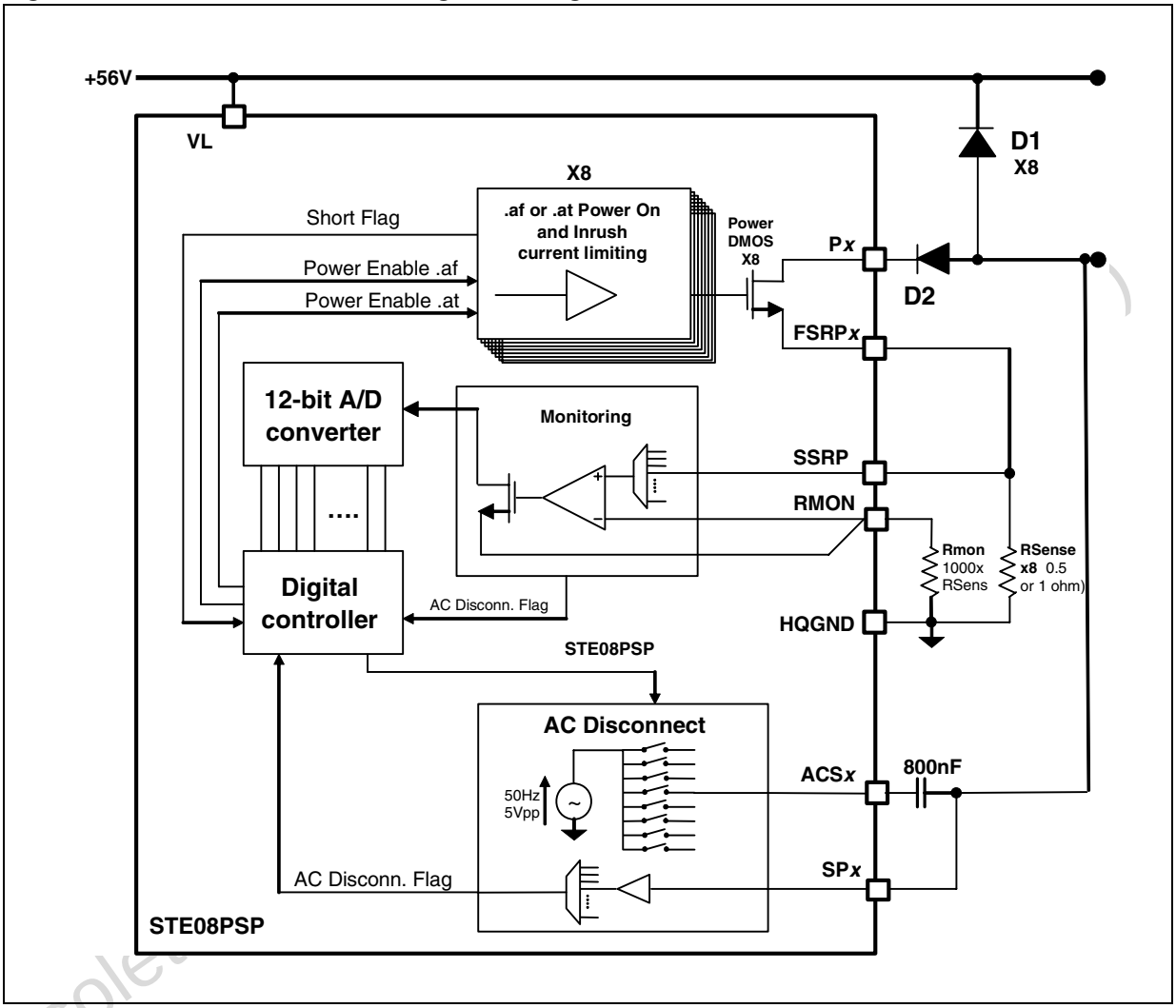
In this condition the internal command **boost** remains at a low level and after the inrush time (Tinrush means a channel working with a maximum current limit of 425 mA) the maximum current limit of the port is set to 425 mA.

6.3.2 Power on AT mode

If the classification power of the channel is higher than the AF-AT power threshold value the connected PD is switched on in the power boost enhancement (AT) mode *Figure 11*.

In this condition the internal command **boost** is set at a high level after the inrush time (Tinrush means a channel working with a max current limitation of 425 mA) and the maximum current limit of the port is set to 820 mA.

Figure 11. Power on and monitoring block diagram



6.3.3 Power management

The STE08PSP manages the power-on (standard, AF, or power boost enhancement, AT, procedures. It continuously calculates the power supplied and manages the power-off procedures of the various lines.

When a new valid PD is connected there is a new power request and the STE08PSP verifies if Pnew is greater or less than Pavail where:

Pnew = requested power from the PD

and

Pavail = PBudget - PGap - PUsed.

- When Pnew < Pavail the STE08PSP behavior is simple and the new PD request is satisfied.
- When Pnew > Pavail, the STE08PSP has different responses depending on the setting of smart-power and priority algorithms (set in configuration register), as explained in the following chapters.

The STE08PSP continuously measures the instantaneous Vbatt level and the instantaneous current for each powered Port. It calculates the supplied power and reports these measurements in the corresponding registers.

The monitoring machine also manages all operations related to fault and disconnection events as well as managing power-off commands forced by:

- temperature
- smart power
- priority
- GPM algorithms.

PUsed is interpreted as:

The sum of the PD instant powers (instantaneously supplied to the PDs) when dynamic power is enabled

The sum of requested power (static power assigned during classification procedure) when dynamic power is disabled.

The requested power can be either related to the Class declared by the PD or can be customized for each single port. Both can be changed at runtime allowing non-standard power management by accessing just a few registers.

6.3.4 Smart power and priority algorithms

As mentioned above these two algorithms are invoked every time the power requested for a new PD is higher than the current available power. Three types of response are possible depending on the setting of smart-power and priority algorithms which can be enabled or disabled by the corresponding bit in the Global Configuration-2 register.

- The first possible setting disables both algorithms. In this case all the PD requests are satisfied, even if the amount of power is over the maximum power available. It is important to note that in this case no power checks are implemented.
- The second possibility is smart-power enabled but priority disabled. In this case the PD requests are satisfied up to the maximum power available value. Over this limit any other PD request is refused by the STE08PSP regardless of the priority level. In this configuration the STE08PSP cannot switch off any channel in favor of a higher priority one.
- The third possible choice (set by default) enables both smart-power and priority. In this case, with a new PD power request, the STE08PSP tries to release the necessary power, switching-off some lower priority PDs in order to satisfy the new high priority request.

With GPM disabled, the investigation concerning the switching-off of PDs is implemented independently by the STE08PSP. With GPM enabled, the investigation is implemented by the Master device looking for the lowest priority ports to be switched off.

6.3.5 Battery crash

The STE08PSP can be supplied from a maximum of 3 batteries. The total power budget is split according to the number of batteries actually available.

The number of batteries suppling the device is monitored through a dedicated pin Vbatt_Check (see *Figure 12* for implementation).

During the normal operation the device continuously monitors the number of batteries which can suddenly decrease if a crash happens. If one or two batteries are crashed or switched-off, the available power is instantly re-budgeted and, if it drops below the amount of power supplied PUsed, an error flag is set and the STE08PSP reacts by switching-off some of the PDs. The priority algorithm influences the switching-off of powered channels.

Figure 13 shows a typical 3-battery operation (a single- or 2-battery scheme can easily be substituted).

Table 5 shows the Vbatt_check voltage thresholds.

Figure 12. Battery crash implementation circuit

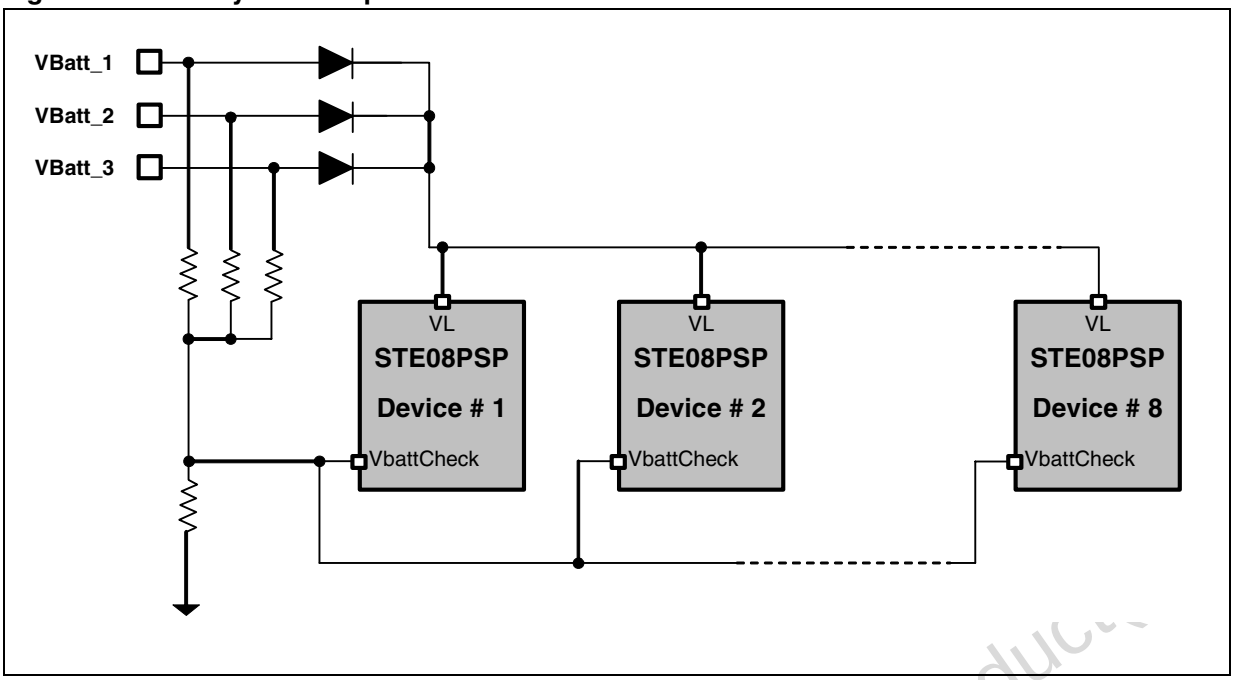


Table 5. Battery check thresholds versus Vbatt value

	Battery voltage		
	VL < 46 V	**46 V < VL < 52 V**	**VL > 52 V**
1 Batt	Vbatt-check < 0.92 V	Vbatt-check < 1.07 V	Vbatt-check < 1.22 V
2 Batt	0.92 V < Vbatt-check < 1.53 V	1.07 V < Vbatt-check < 1.68 V	1.22 V < Vbatt-check < 1.83 V
3 Batt	1.53 V < Vbatt-check	1.68 V < Vbatt-check	1.83 V < Vbatt-check

6.4 Multi device application

The STE08PSP can be used alone. In a multi-device application it can manage a system of up to 8 devices for a total of 64 channels without the need of an external micro-controller. In this case, to save area and cost, the clock generation, battery check management and the 3.3 V voltage regulator can also be shared among the devices. In a multi-device application the STE08PSP connected through the secondary I2C must have 3 different address LS bits.

6.5 Master negotiation

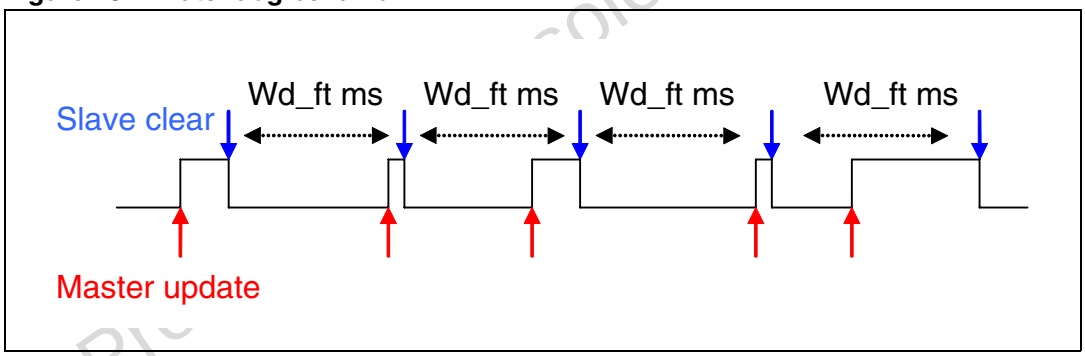
A dedicated state machine is included in the GPM block to manage the master negotiation at the startup of the system. The FSM does this by using the secondary I2C bus, which can work both as master and slave (see related chapter). At system startup a Master negotiation procedure is implemented, after which only one STE08PSP is the Master controlling the I2C interface. All the other devices are Slaves. In this implementation the secondary I2C bus supports a maximum of 8 STE08PSP devices, one Master and seven Slaves. One EEPROM defines the dedicated default settings. The address of the STE08PSP used to communicate through the secondary I2C is *0010xxx* (note that it is slightly different from the address used for Primary I2C). The address of the EEPROM must be *1010yyy*. They are in both cases defined by setting dedicated devices and memory pins. At startup, after the system power up, each STE08PSP device starts the negotiation to try to assume the status of Master. Each STE08PSP starts with its own 3 least-significant I2C address bits as the EEPROM I2C address, then probes the EEPROM with 8 possible I2C addresses. During a read operation, the I2C Master arbitration ends and Master STE08PSP is generated.

Note: According to the I2C master arbitration strategy, for the master negotiation the first powered STE08PSP or the STE08PSP with I2C address "0000" wins the master negotiation. The figures below show the evolution of the master negotiation. This procedure is supported in the I2C bus standard specification.

6.5.1 Master alive and master re-negotiation

To prevent a system crash if the Master STE08PSP is out of service, a master alive watchdog flag has been introduced.

Figure 13. Watchdog behavior



The scope of this flag is to ensure that every Slave knows if the Master is alive or not. A living Master, which is functioning correctly, sets the flag to '1' in each Slave periodically, usually before each read of the power data from the Slaves (every 15 ms for each STE08PSP of the system). Each Slave also checks if the flag is set to '1' and resets the flag to '0' every Wd_ft milliseconds (customizable in EEPROM register 0x0A). Thus, if a Master fails, the system is able to react by generating a new Master. If the flag is not updated by the Master, all the Slaves restart the negotiation algorithm and try to assume the status of Master. At the end of this re-negotiation a new Master able to manage the system is generated. In this case there is no need to re-read the EEPROM data. *Figure 13* illustrates the watchdog behavior.

6.5.2 Global power management overview

The global power management feature is introduced to avoid the need of an external micro controller to manage a system of several STE08PSP devices in a single board. The system architecture is shown in *Figure 3*.

The global power management allows management of a system of 8 STE08PSP devices for a total of 64 channels. The communication among the elements of the system is possible using the secondary I2C interface which connects all the devices. At the startup one of the STE08PSPs of the system wins control of the secondary interface and assumes the status of master, the other devices become slaves. The master manages the complete system 'reading from' and 'writing into' the slaves (up to a total of 7) all the necessary data and commands. A dedicated GPM state machine is embedded in the STE08PSP device in order to implement the global power management feature.

After boot the master reads the value of the power used from each slave. It then calculates the total power of the system as the sum of all the power contributions and finally writes the total power used value into all the slaves. When a new PD connection requires more than the available system power, an alert flag present in every STE08PSP (and periodically read by the Master) is set. In this case the Master decides if the new PD can be switched on, switching off some PDs with lower level of priority, or refuses the new PD.

Power information propagation

To manage the power of the system the master must read information about power and priority from each slave. This information is structured to decrease the amount of data passing on the secondary I2C, in order to reduce the time requested to implement any decision and action. The master reads from slave number *n* the value of power (PUsed) referred to the priority level *m* defined P*nm*. All the information is stored in a 4x8 matrix of registers in the GPM block as shown in *Table 6*.

Table 6. GPM power information

	Poe0	Poe1	Poe2	Poe3	Poe4	Poe5	Poe6	Poe7
Priority 0	P00	P10	P20	P30	P40	P50	P60	P70
Priority 1	P01	P11	P21	P31	P41	P51	P61	P71
Priority 2	P02	P12	P22	P32	P42	P52	P62	P72
Priority 3	P03	P13	P23	P33	P43	P53	P63	P73

After the reading this information, the Master calculates the total power used by the system, *Ptot*, writing the value into all the Slaves. Starting from the total power used information, every Slave is then able to calculate the remaining power supply capacity by itself.

Global power-on and power-off management

In a multi-device configuration every STE08PSP knows the total power used in the system by the information propagated by the Master, through the secondary I2C.

Using this information, the STE08PSP can calculate the amount of power available for new PD connection. Every STE08PSP in the system knows the total available power, since it is able to calculate it using the information propagated by the master through the secondary I2C. Accordingly, each slave knows if a new PD insertion can be managed directly by itself or not. The first case happens when the power requested from a new PD is lower than the value of the total power available. In this case no power fault is detected and the slave needs no Master feedback. The slave simply satisfies the power-on request and updates its own value of supplied power. Then the master reads the new power information, calculates the new total power used and updates the new value into all the slaves.

However, if the new power request is higher than the power available, an alarm is sent from the slave to the master and a global action is requested. The master, applying to all the system the smart-power and priority algorithms, decides what to do.

6.6 Programmability

6.6.1 Parameter settings

This section contains the codification of the various parameters such as:

- detection conductance or resistances
- classification currents
- monitoring currents
- port voltages
- port powers or power budgets.

For more details please refer to STE08PSP *register description programming manual (PM0050).*

Table 7. Parameter coding

Parameter	Description	Range	Step	Units	Bits
Detection					
I det	Detection current	0 to 1023	1	µA	10
Idet	Detection linearity check	0 to 255	1	µA	8
Gdet, Gdl, Gdh	Detection conductance	0 to.256	0.250	µS	10
Rdet, Rdl, Rdh	Detection resistance	8 to 71.98	.01562	kΩ	12
Tnull	Detection current recovery time (8 V to 6 V step)	0 to 25559	0.39	µs	16
Classification					
Iclass	Classification current	0 to 70	0.065064	mA	10
Tclass	Classification steps timings	0 to 25	0.1	ms	8
Pclass	Channel power assigned	0 to 71	0.070068	W	10
Monitoring					
Imon	Channel current during powering	0 to 1024	0.031266	mA	15
Vport	Battery voltage	0 to 70	0.068	V	10
Pmeas	Channel power usage	0 to 71680	1.094	mW	16
Other settings					
System Power	System power budget	0 to 13775	0.070068 * Nbatt	W	16
Power Gap	System power guard	0 to 143	0.560	W	8
Power settings	Power class or custom setting	0 to 71	0.280	W	8

Note: Rdet- Rdl- Rdh set is in alternative to the Gdet -Gdl- Gdh set which is the default one. If Rdet measured is more than 500 kΩ the open circuit flag is set

6.6.2 EEPROM management

A small EEPROM can be connected to the secondary I2C bus and used to configure a single STE08PSP or a system, which can be composed of up to 8 devices.

The address of the EEPROM must be *1010xxx*. The 3 least-significant bits are typically set by means of dedicated pins of the memory device.

At startup, after the system power up and negotiation, the Master STE08PSP probes the secondary I2C looking for a compliant EEPROM. Starting from its own 3 leas-significant bit address it scrolls all the eight possible EEPROM 3-bit addresses (see also *Section 6.5: Master negotiation*).

The EEPROM also provides the STE08PSP with information related to the system architecture (single-device or multi-device system).

In the first case the EEPROM is simply read by the STE08PSP which sets its own registers according to the data stored in the EEPROM. In the second case, one of the devices (Master), reads the setting data from the EEPROM and writes them into all the other devices (Slaves).

If no EEPROM is connected to the secondary I2C bus, the STE08PSP works stand-alone using its default settings, and the GPM function is automatically disabled.

For EEPROM register content, please refer to the STE08PSP programming manual PM0050.

6.7 Monitor interface (I2C and LED drivers)

6.7.1 I2C protocol overview

The I2C bus Interface serves as an interface between the STE08PSP and the serial I2C buses.

The Primary Interface can only provide Slave functions and its purpose is to connect the device with the host controller. It can be connected both with a standard I2C bus and a Fast I2C bus.

The secondary interface provides both multi master and slave functions, and controls all I2C bus-specific sequencing, protocol, arbitration and timing. It supports fast I2C mode (400 kHz).

The interrupts are enabled or disabled by software. The interfaces are connected to the I2C bus by a data pins (SDA_S for Primary I2C, SDA_M for secondary) and by clock pins (SCL_S and SCL_M).

6.7.2 I2C device address

The device primary I2C address is in the form: *001xyzv b*.

The device secondary I2C address is in the form: *0010yzv b*.

The user can set the lower I2C address bits just connecting HV_I2C_ADDR [1:0] to VL (through a 200 kΩ resistor), V3.3, V10 or GND as in *Table 8*:

Table 8. Address map

4-bit device address	HVI2C address1	HVI2C address0
0000	0 V	0 V
0001	0 V	3 V
0010	3 V	0 V
0011	3 V	3 V
0100	0 V	10 V
0101	10 V	0 V
0110	10 V	3 V
0111	3 V	10 V
1000	10 V	10 V
1001	0 V	VL
1010	VL	0 V
1011	3 V	VL
1100	VL	3 V
1101	10 V	VL
1110	VL	10 V
1111	VL	VLt

6.7.3 Functional description

In Master mode, the device initializes a data transfer and generates the clock signal. A serial data transfer always begins with a start condition and ends with a stop condition. Both start and stop conditions are generated in master mode. Data and addresses are transferred as 8-bit bytes, MSB first. The first byte following the start condition contains the device address. A 9th clock pulse follows the 8 clock cycles of a byte transfer, during which the receiver must pull down the SDA line to acknowledge the transfer.

In Slave mode as soon as a start condition is detected, the address is received from the SDA line and sent to a shift register; then it is compared with the internal address. In the case of an address mismatch the interface ignores it and waits for another.

If the address matches, the interface generates an acknowledge pulse.

Following the address reception, the digital controller receives bytes from the SDA line, storing them in the data register via an internal shift register, or sends bytes from the data register to the SDA line through the internal shift register. After each byte reception an acknowledge pulse is generated by the controller.

A Stop condition generated by the host processor, after the last data byte is transferred, closes the communication.

An error state is generated when Stop or Start conditions are detected during a byte transfer. When Stop is detected, the interface discards the data, releases the lines and waits for another Start condition. When Start is detected, the interface discards the data and waits for the next slave address on the bus.

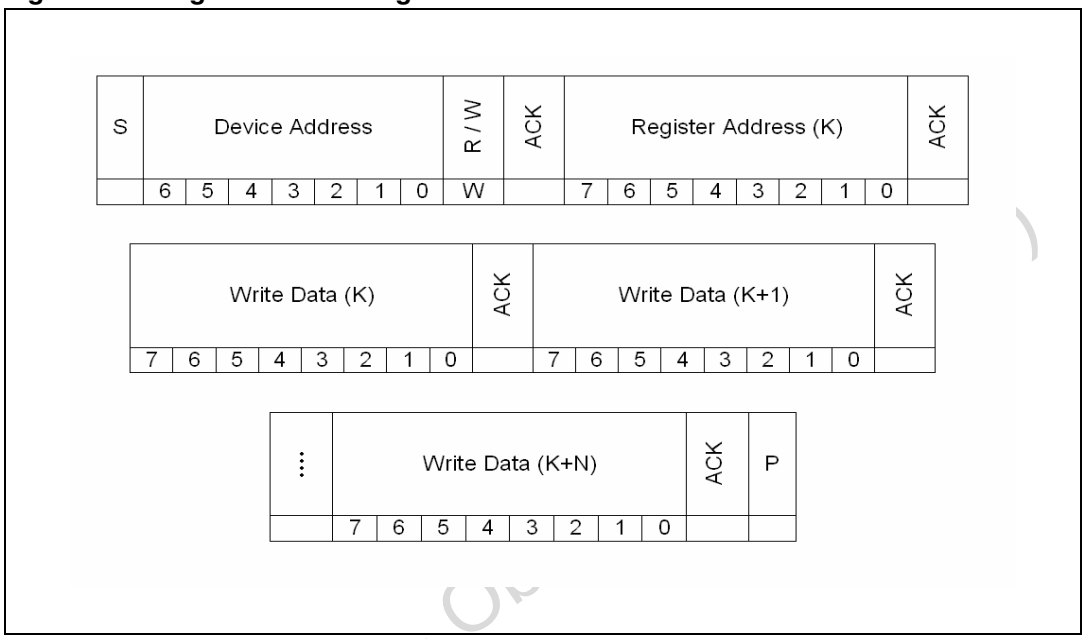
Interrupts

The Irq register bits indicate which signals can generate an interrupt. The register is read only and to clear the interrupt bits the corresponding source event has to be cleared. The logic OR condition of the interrupt bits causes the INTN pin assertion. The INTN assertion can be masked via the interrupt mask register Irq_mask.

6.7.4 Register addressing: write command format

The I2C write command format is shown in *Figure 14*.

Figure 14. Register addressing: write command format



The formatting bits shown in *Figure 14* are defined as follows:

- S - I2C start condition
- P - I2C stop condition
- ACK – acknowledge
- NACK - negative acknowledge
- R/W - read/write.

The device address is the value specified in the I2C device address. The register address is an eight-bit value that is written into an internal Index Register. Each time a byte of data is written to, or read from the POE controller, the Index Register increments by one.

If the start value written to the Index Register is K, the byte after the Register Address byte is written into the register at address K. The next byte is written into the register whose address is K+1 and so on.

An I2C write command can contain from 0 to 255 write data bytes. Write commands to an unknown register location are ignored by the interface.

As indicated in *Figure 14*, the bits are ordered with the most significant bit first.

6.7.5 Register addressing: read command format

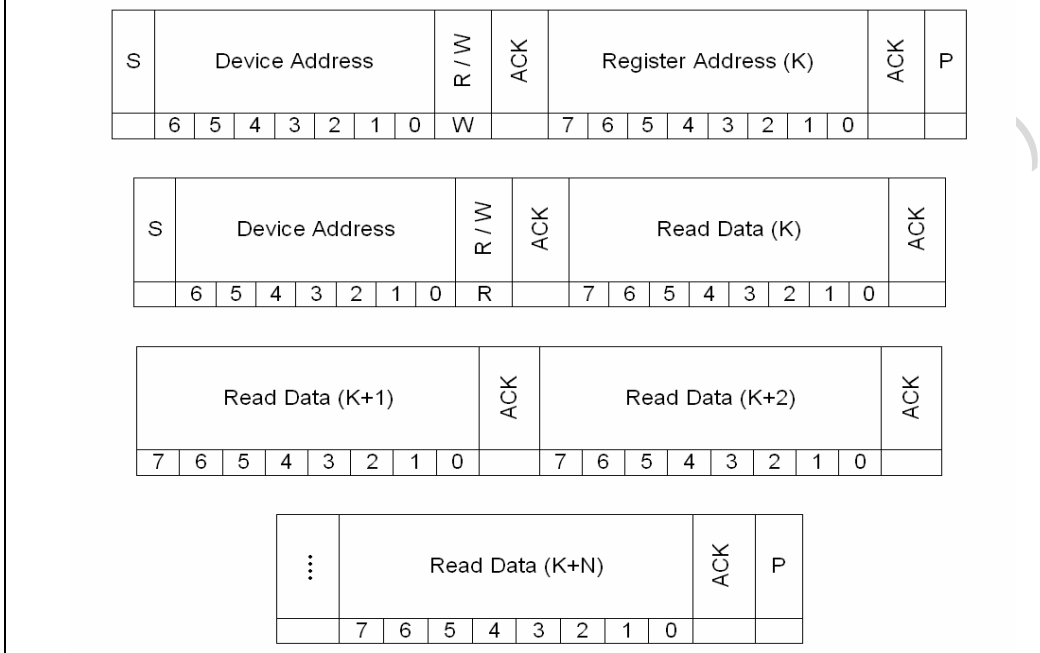
The general form of the read command is shown in *Figure 15*.

First part of the general read command consists of writing an address to the Index Register of the POE controller. If the Index Register already contains the address of the register to be read, as the result of a previous read or write command, then it is not necessary to write that address to the Index Register again.

After each byte is read from the POE controller, the Index Register increments by one.

A read command can contain between 0 and 255 read data bytes.

Figure 15. Register addressing: read command format



6.7.6 Status monitoring interface

In order to monitor the status of the different ports without the I2C register addressing a simple output status interface has been implemented. The status flag notification is enabled via the configuration register Global_config2, STATUS_FLAG_EN bit (by default this bit is high, enabled).

This interface comprises 5 digital output signals which cyclically show the status of the 8 channels:

- **CHstartcount**: indicates the beginning of the scanning (ch1) of the channel whose status flags (Ch_stat (2:0)) are currently notified externally. It is high each 8 cycles of CHclock
- **CHclock**: clock signal indicating the change of the channel whose status flags (Ch_stat (2:0)) are currently notified. This clock is 60 * MCLKout clock cycles 1.67% duty-cycle (100 kHz with a 6 MHz MCLKout).

Ch_stat (2:0) can be interpreted as follows:

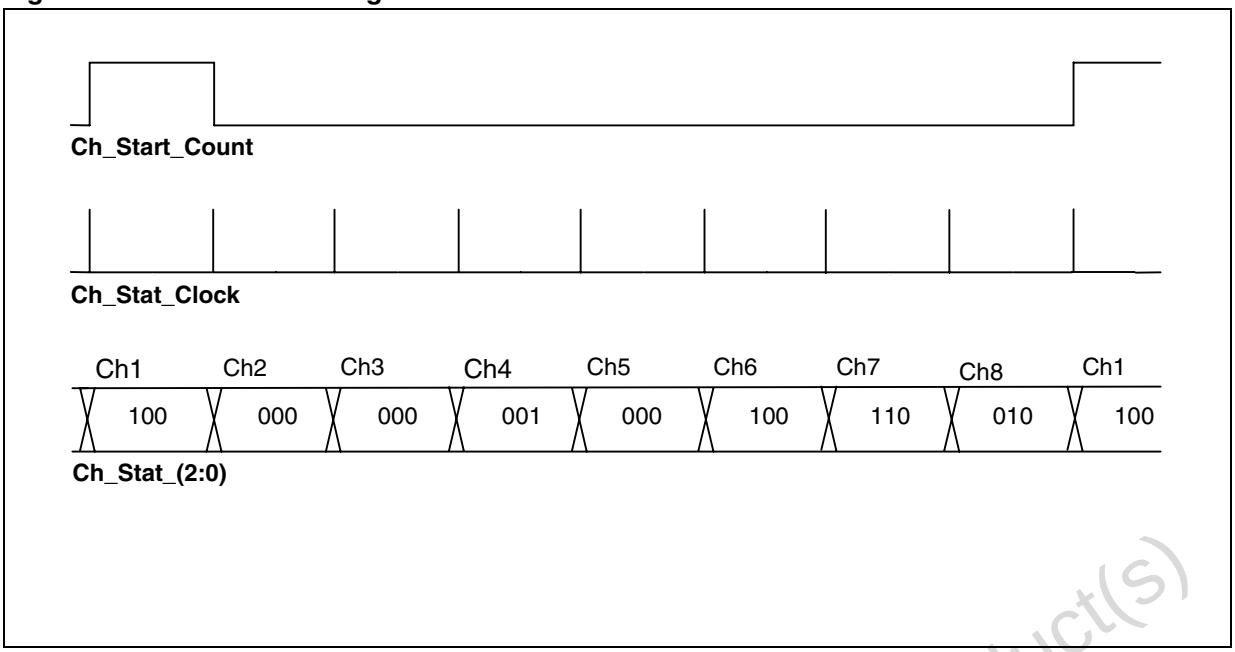
- 000: current channel not operating (NOP)
- 001: current channel under detection (DET-CLASS)
- 010: current channel disconnection procedure (AC/DC discon.)
- 110: current channel in fault condition (OVcurr/OVLD)
- 100: current channel in normal powering mode (POK)

where:

- DET-CLASS indicates a situation where a channel is not yet powered and is currently probed for the signature research.
- AC/DC disconnection rises when a powered channel fails in providing a correct MPS (maintain power signature) this typically happens when a PD is disconnected from the line.
- POK stands for power OK, where high indicates that channel is currently powered in normal condition.
- OVLD stands for over load and indicates a faulty condition due to abnormal power absorption (more than Pclass) of a powered channel.
- OVcurr stands for over current and it highlights a channel whose current has reached the power on current limit (425 mA for standard port and 850 mA for boosted channel).

This information is particularly useful in the case of simple applications without a microprocessor or for testing purposes. Another use is to easily build up an LED graphical interface showing the runtime status of the various channels.

Figure 16. Status monitoring data format



In the above example, channels 1 and 6 are in power on condition while channel 4 is in detection/classification, channel 7 is in over current/over load (fault) condition, channel 8 is in disconnection and channels 2, 3 and 5 are waiting for operations.

6.8 DC-DC converter

The STE08PSP can easily be configured either as a 3.3 V generator or load. Thus, the need for extra-low voltage batteries is avoided, greatly simplifying the system design. The device can operate in 3 ways depending on the status of S/U pin and circuit topology:

- If S/U is left open the device operates as an SMPS controller.
  The SMPS can be used to power the 3.3 V up to 800 mA load and high voltage conversion efficiency also powering an entire system.
- If S/U is tied low and if the device is solely responsible for biasing itself a LINEAR regulator is sufficient and the presence of a BJT easily allows the device to function.
- S/U is tied low and the 3.3 V is provided. The device simply acts as a load.

The 10 V biasing is internally generated from VL. In case of low-power applications the 10 V biasing can also be externally provided or generated by the 3.3 V SMPS.

Figure 17 is a typical application with the DC-DC converter in Buck configuration supplying the 3.3 V voltage. The 10 V voltage is generated by means of an internal linear regulator. The 3.3 V can supply up to 1 A load.

In *Figure 18* the usage of a small transformer supplying the 10 V can save up to 0.3 W for each powered device. Both 3.3 V and 10 V voltages can supply others devices.

Figure 19 depicts a typical application with external BJT implementing a Linear regulator topology power supply.

Figure 17. 3.3 V SMPS buck configuration

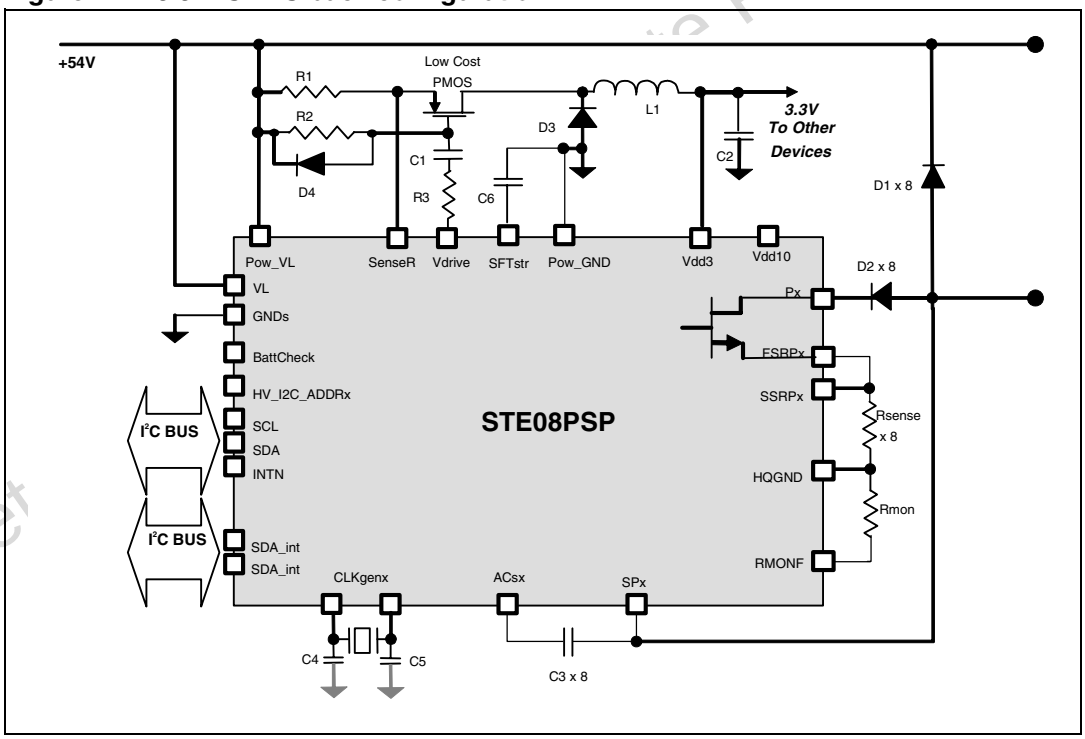


Figure 18. 3.3 V and 10 V SMPS application

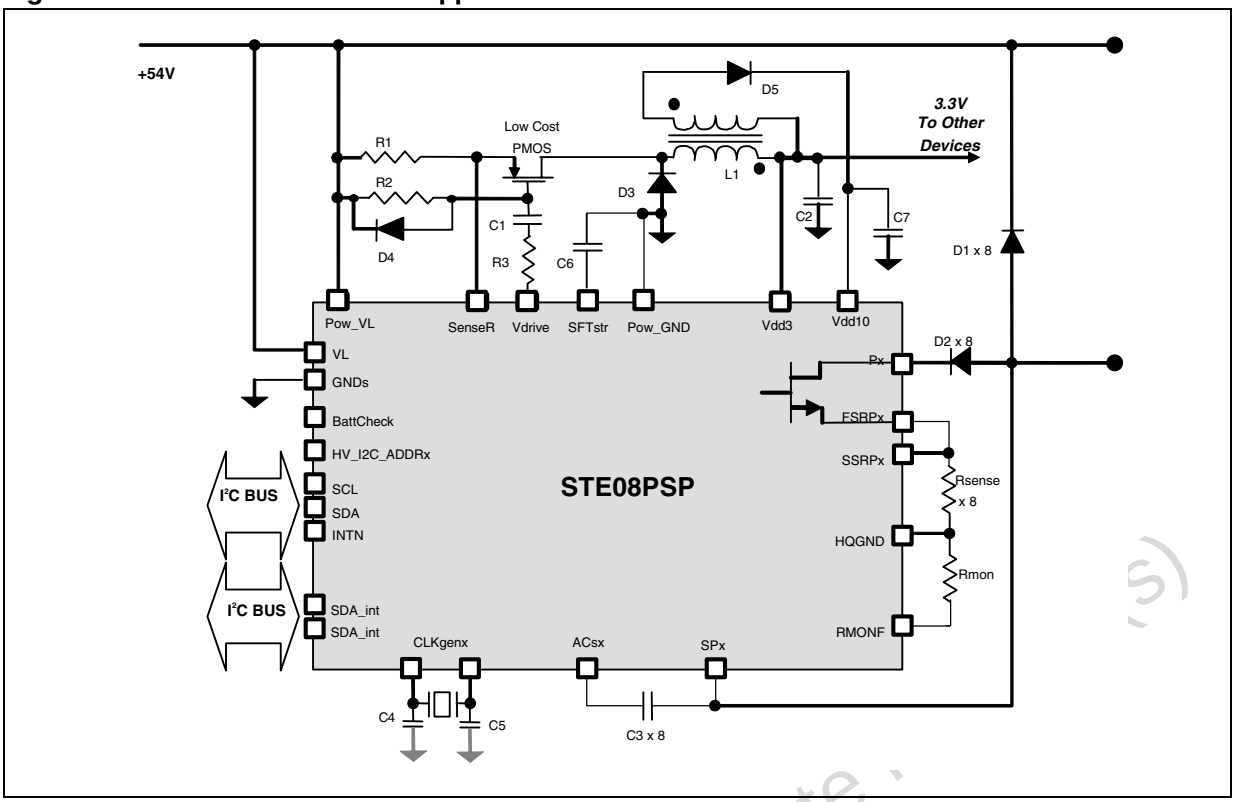
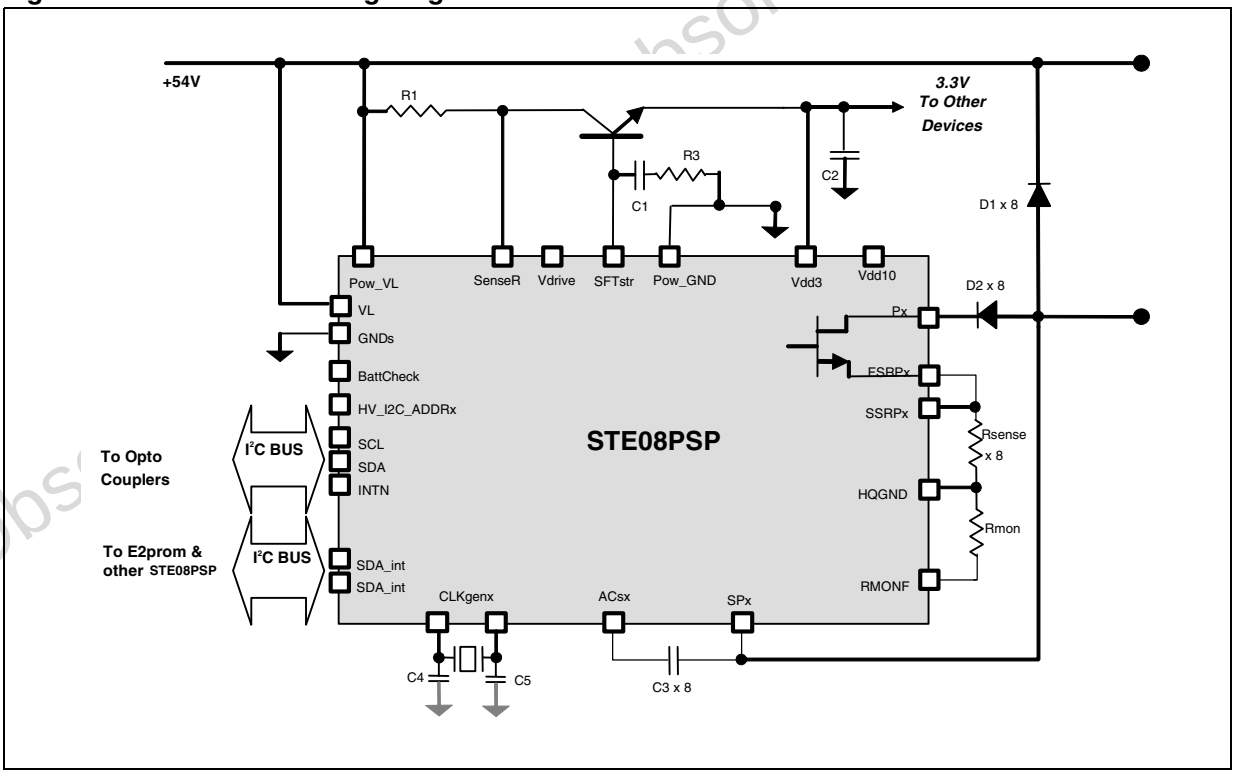


Figure 19. 3.3 V linear voltage regulator



6.9 Clock generators

The following figures illustrate the three possible configurations for the clock generation:

- *Figure 20* shows the generation of a high precision clock with a 6 MHz crystal,
- *Figure 21* shows the clock generation with an RC oscillator in a low-cost application,
- *Figure 22* shows the configuration with an external clock.

Figure 20. Crystal high precision clock

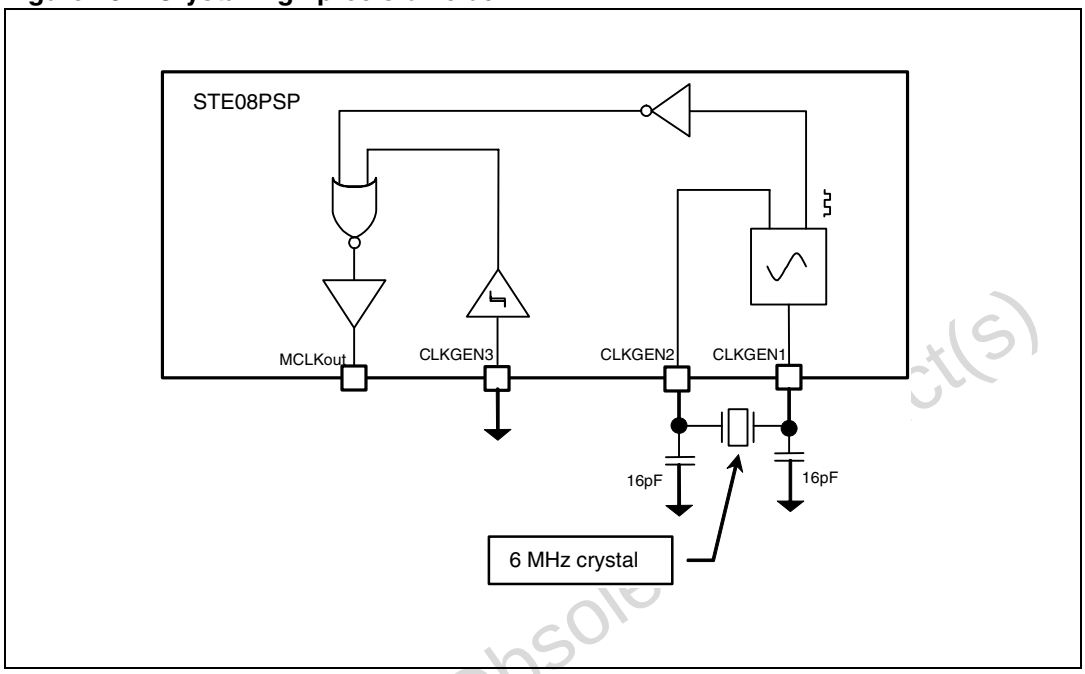


Figure 21. RC oscillator clock

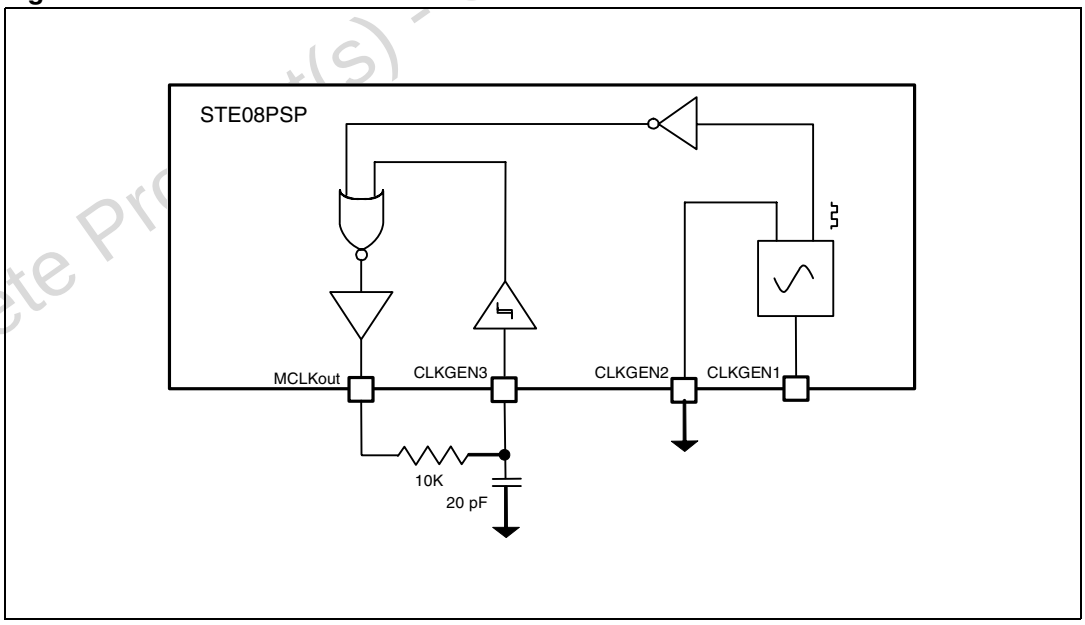
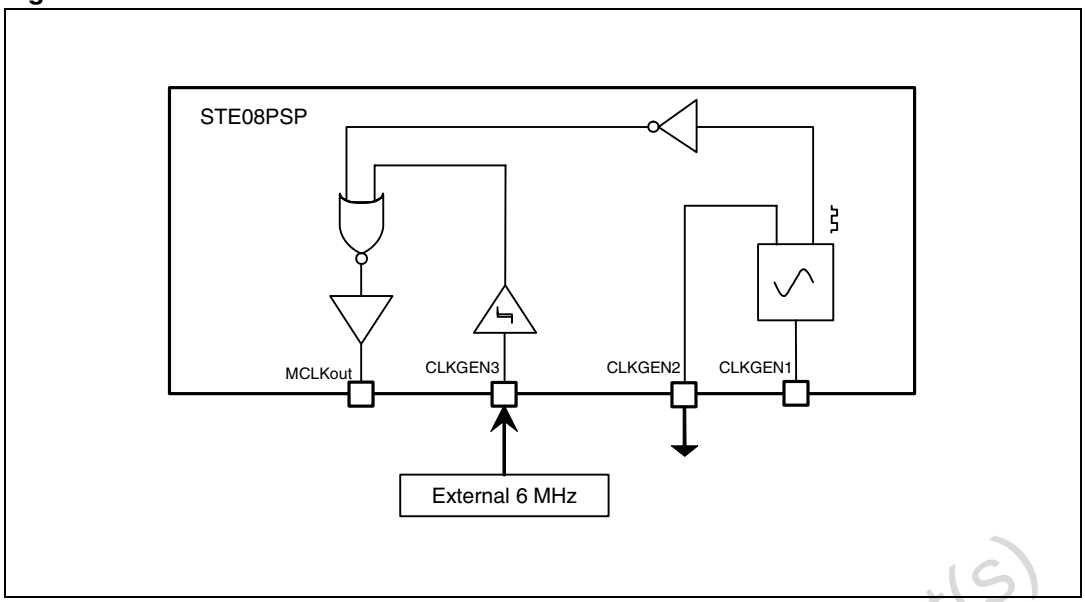


Figure 22. External clock



6.10 Thermal monitoring

The procedures performed by the digital controller are impacted by the thermal monitoring data indicating the measured temperature.

Its behavior is based on a three-level control system:

- When the device internal temperature reaches 110 °C, only the channels already powered are maintained. New ones are rejected and processed when the temperature cools down to 100 °C. This behavior can be disabled by setting the relevant register bit.
- A second temperature threshold is set at 130 °C. When this threshold is reached the device behavior is similar to the previous one but the channels that are in current limiting or inrush condition are immediately switched off and their reactivation, subject to a positive re-detection, is only possible when the device internal temperature has cooled to 100 °C. This behavior can be disabled by setting the relevant register bit.
- The third temperature threshold is set at 150 °C. When this temperature is reached all activated channels are immediately switched off and their reactivation, subject to a positive re-detection, is only possible when the device internal temperature has decreased to 100 °C. This behavior cannot be disabled.

7 Electrical and timing characteristics

Table 9. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VL, Pow_VL	Battery voltage	90	V
Vdd3	3.3 V power supply	3.6	V
Vdd10	10 V power supply	12	V
Tj	Maximum junction temperature	150	°C

Table 10. Operating range

Symbol	Parameter	Value	Unit
Topt	Operating temperature range	-20 to +85	°C
VL, Pow_VL	Battery voltage	44 to 57	V
GNDs	GND separation	0.3	V
Vdd3	3.3 V when externally supplied	3 to 3.6	V
Vdd10	10 V when externally supplied	9 to 11	V
IVdd10	10 V current sink (when externally supplied)	Typ 6.7	mA
IVL	Battery current sink (when 10 V is externally supplied)	Typ 0.4	mA
IVL	Battery current sink (when 10 V is self generated)	Typ 7.4	mA
IV3.3	3.3 V current sink (AUTO mode)	Typ 20	mA

Table 11. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ\text{-}Amb}$	Thermal resistance Junction to Ambient (Natural convection)	25	° C/W

Table 12. Electrical characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Detection						
Vdl	Detection voltage low	3.7	4	4.3	V	Between port terminals
Vdh	Detection voltage high	7.4	8	8.6	V	Between port terminals
Vdm	Detection linearity check voltage	5.6	6	6.4	V	Between port terminals
Tds	Transient time between Vdl and Vdh	300			µs	Customizable with external capacitor Cdetslow
Gdl	Conductance signature lower limit	25		50	µs	Software programmable
Gdh	Conductance signature Higher limit	41		82	µs	Software programmable
Rdl	Resistance signature lower limit	12		24	kΩ	Software programmable To be used in alternative to Gdh
Rdh	Resistance signature Higher limit	20		40	kΩ	Software programmable To be used in alternative to Gdl
Idlim	Current limit during detection			1.1	mA	
Tdet	Detection time		50		ms	8 ports configuration. One channel at a time
Tdetd	Detection delay time (from PD insertion to the end of detection)			852	ms	Maximum delay for 8 ports configuration.
Tdbo	Back off time (midspan mode)	2			s	Back off time in case of failed PD detection Avoided if Rdet > 500 kΩ or Gdet < 2 µs
Ted	Error delay time	750			ms	
Classification						
Vcl	Classification probing voltage	15.9	17	18.1	V	Between port terminals
Icllim	Current limit during classification	55		70	mA	
Tcl	Classification time		15		ms	Programmable
Vmark	Mark Voltage during MCA		8		V	Programmable
Tmark	Mark Time during MCA		9		ms	Programmable
Ithcl0	Class0-1 current threshold	5.5	6.5	7.5	mA	
Ithcl1	Class1-2 current threshold	13.5	14.5	15.5	mA	
Ithcl2	Class2-3 current threshold	21.8	23	24.2	mA	
Ithcl3	Class3-4 current threshold	31.5	33	34.5	mA	

Table 12. Electrical characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Ithcl4	Class4-0 current threshold	45.5	46.5	47.5	mA	
Powering						
Pall	Maximum power per channel			40	W	See also classification paragraph
Iinrush	Output current startup mode	400		450	mA	Inrush current soft start
Imin	Power off current	5		10	mA	Disconnect for t > TPMDO (DC disconnection method)
Acfre	AC disconnection sinusoidal generator		50		Hz	Frequency spread related to clock stability
Vacd	AC generator open line voltage		5		Vpp	
Zac	AC impedance needed to maintain power		100		kΩ	
Tmpdo	PD power maintenance request drop out time limit (Software programmable)	300		400	ms	The STE08PSP does not remove power if the PD maintenance signal is absent for less than 300 ms duration. If an absence of power maintenance signal has been detected, the STE08PSP shall remove power within 400 ms max (see also timers programmability)
Icut	Over load current	Pall/ VPort		400/ 720	mA	After a time duration of Tovld the STE08PSP disconnects the power from the port. Depending AF or AT mode
Tovld	Over load time limit (Software programmable)	50		75	ms	In fault condition for Tovld the STE08PSP disconnects the port. (See also timers programmability)
Tshort	Short-circuit/inrush time limit (Software programmable)	50		75	ms	In fault condition for Tshort the STE08PSP disconnects the port. (See also timers programmability)

Table 12. Electrical characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Notes
Ilim	Output current – at short load condition	400 820		450 900	mA	Max. value of the port current during short circuit condition. The power is disconnected from the port within Tshort. Depending AF or AT mode
Tinrush	Rise time of Vport time limit			75	ms	Expired Tinrush if the channel is still in limiting condition it is considered in fault
Toff	Turn off time			100	ms	From VPort to 2.8VDC
Ron	Internal Mos resistance			300	mΩ	
VsLR	3.3V range in generator mode	3	3.3	3.6	V	
V10 int	10V range internally generated		8.7		V	
	Battery check					TBD
Digital						
Fclk	Clock frequency		6		MHz	
Vih	Input high voltage	2			V	@VDD=3.3V
Vil	Input low voltage		0.8		V	@VDD=3.3V
Ith	Input high current			30		
Iil	Input low current			10		

8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

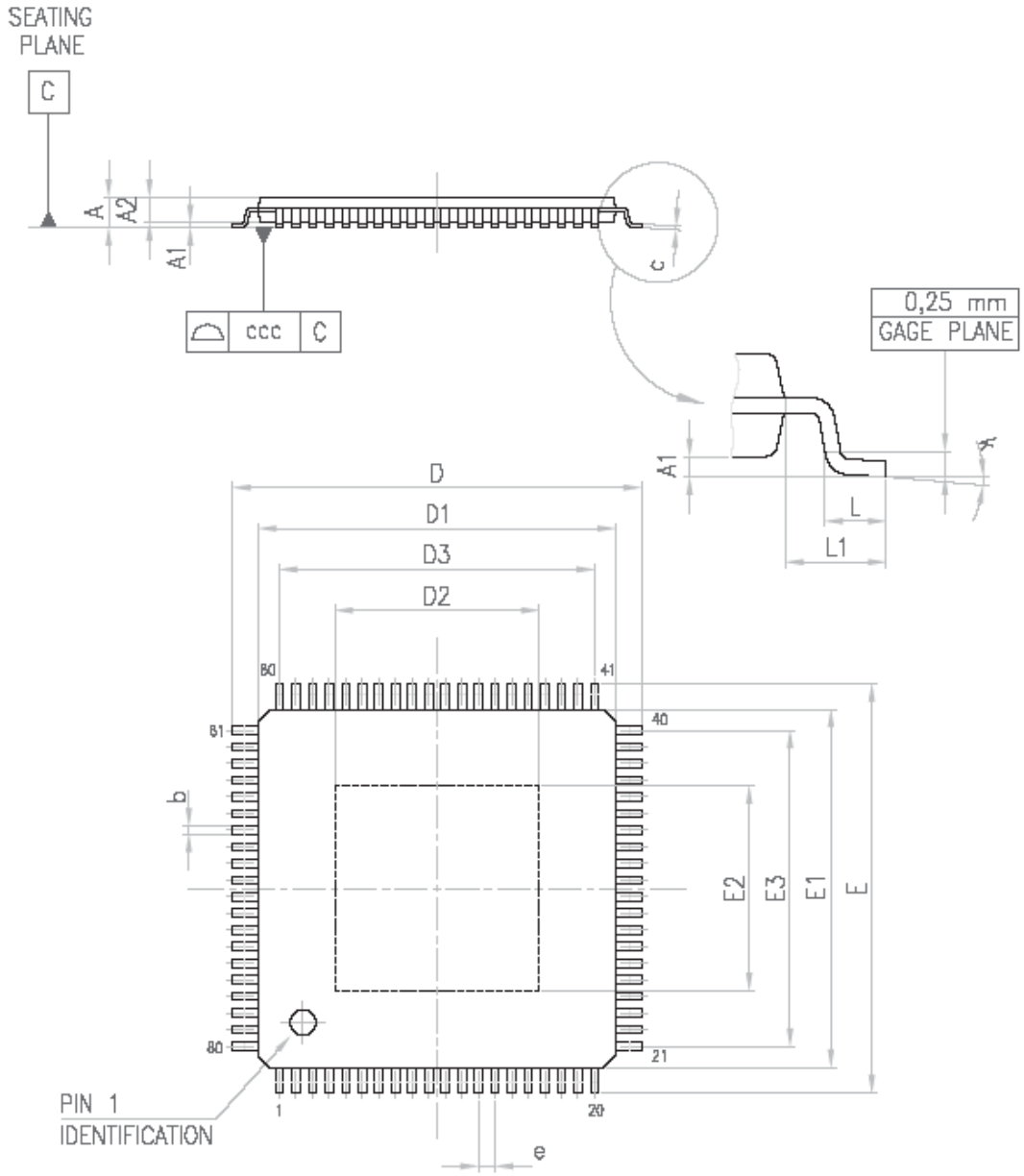
The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 13. TQFP 80L 14x14x1.0 foot print 2.0 (2x1.0 mm) exposed pad down(1)

Reference	Min.	Typ.	Max	Unit
A			1.20	mm
A1	0.05		0.15	mm
A2(2)	0.95	1.00	1.05	mm
B	0.22	0.32	0.38	mm
C	0.09		0.20	mm
D	15.80	16.00	16.20	mm
D1	13.80	14.00	14.20	mm
D2	According to pad size(3)			
D3		12.35		mm
E	15.80	16.00	16.20	mm
E1	13.80	14.00	14.20	mm
E2	According to pad size(3)			
E3		12.35		mm
e		0.65		mm
L	0.45	0.60	0.75	mm
L1		1.00		mm
K (degrees)	0	3.5	7	deg.
ccc			0.10	mm

1. JEDEC/EIAJ reference number: JEDEC MS-026-AEC-HD
2. TQFP stands for Thin profile Quad Flat Package. Thin profile: body thickness A2 = 1.00 mm
3. The size of exposed pad is variable depending of lead-frame design pad size. End user should verify “D2” and “E2” dimensions for each device application.

Figure 23. TQFP 80L 14x14x1.0 foot print 2.0 (2x1.0 mm) exposed pad down



1. Exact shape of each corner is optional.

9 Ordering information

Table 14. Order code

Order code	Package
E-STE08PSP(1)	TQFP80 14 mm x 14 mm exposed pad slug down plastic package

1. RoHS (lead-free) package

10 Revision history

Table 15. Document revision history

Date	Revision	Changes
31-Jan-2008	1	Initial release.

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