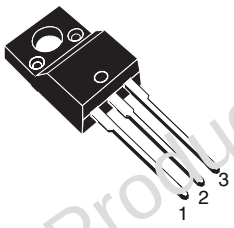
STP30NS15LFP

N-channel 150V - 0.085Ω - 10A - TO-220FP
MESH OVERLAY™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STP30NS15LFP	150V	<0.1Ω	10A

- Extremely high dv/dt capability
- Application oriented characterization
- 100% avalanche tested



TO-220FP

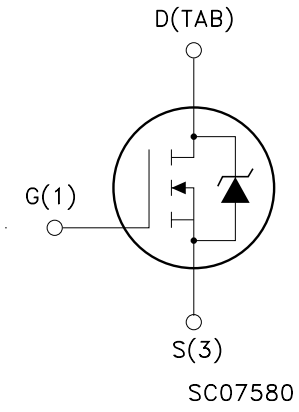
Description

Using the latest high voltage MESH OVERLAY™ process, STMicroelectronics has designed an advanced family of power MOSFETs with outstanding performances. The new patent pending strip layout coupled with the Company's proprietary edge termination structure, gives the lowest RDS(on) per area, exceptional avalanche and dv/dt capabilities and unrivalled gate charge and switching characteristics.

Applications

- Switching application

Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STP30NS15LFP	P30NS15LFP@	TO-220FP	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	150	V
V_{GS}	Gate- source voltage	± 15	V
I_D	Drain current (continuous) at T_C = 25°C	10	A
I_D(1)	Drain current (continuous) at T_C = 100°C	7	A
I_{DM}(1)	Drain current (pulsed)	40	A
P_{tot}	Total dissipation at T_C = 25°C	30	W
	Derating factor	0.2	W/°C
E_{AS}(2)	Single pulse avalanche energy	300	mJ
dv/dt(3)	Peak diode recovery voltage slope	2.4	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; Tc = 25°C)	2500	V
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. Starting T_j = 25 °C, I_D = 15A, V_{DD} = 75V
3. I_{SD} ≤35A, di/dt ≤300A/µs, V_{DD} ≤$V_{(BR)DSS}$, T_j ≤T_{JMAX}

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	5	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250µA, V_{GS} =0	150			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 15V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1	2	3	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 5A V_{GS} = 5V, I_D = 5A		0.85 0.1	0.1 0.112	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS}= 20V , I_D = 7A		6		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0		1080 170 105		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 15V, I_D = 5A R_G = 4.7Ω V_{GS} = 4.5V (see *Figure 13*)		25 95 55 30		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 120V, I_D = 10A, V_{GS} = 5V (see *Figure 14*)		40 7.5 20	54	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 5. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				10 40	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 10A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10A, di/dt = 100A/µs, V_{DD} = 30V, T_j = 150°C (see *Figure 15*)		160 950 12		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

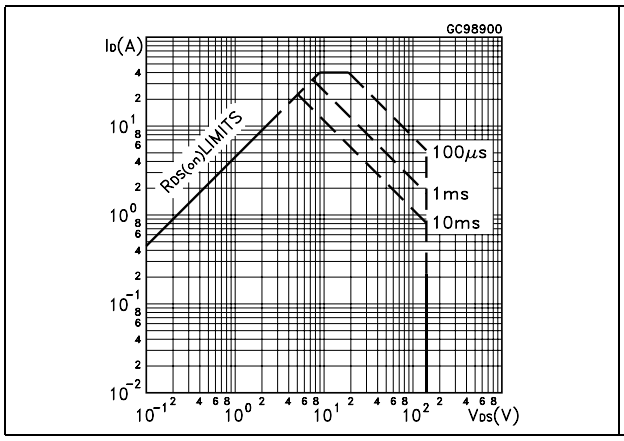


Figure 2. Thermal impedance

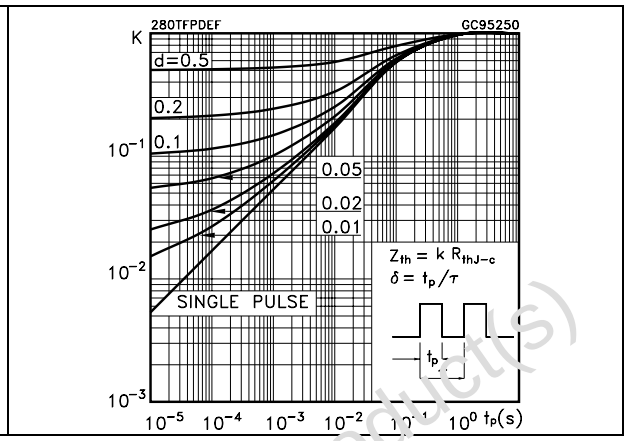


Figure 3. Output characterisics

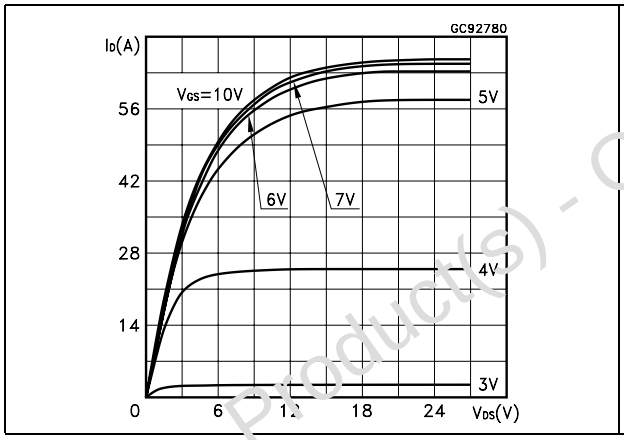


Figure 4. Transfer characteristics

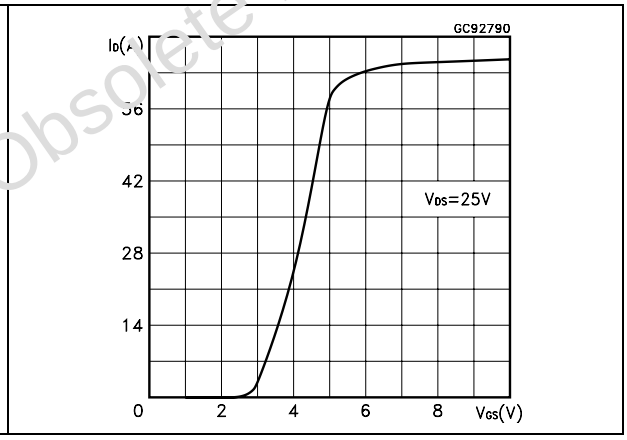


Figure 5. Transconductance

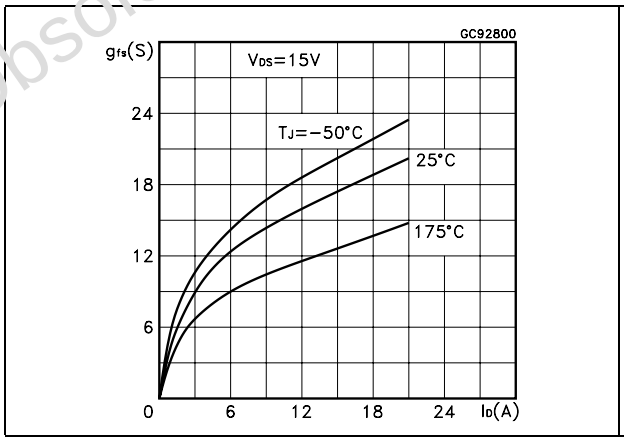


Figure 6. Static drain-source on resistance

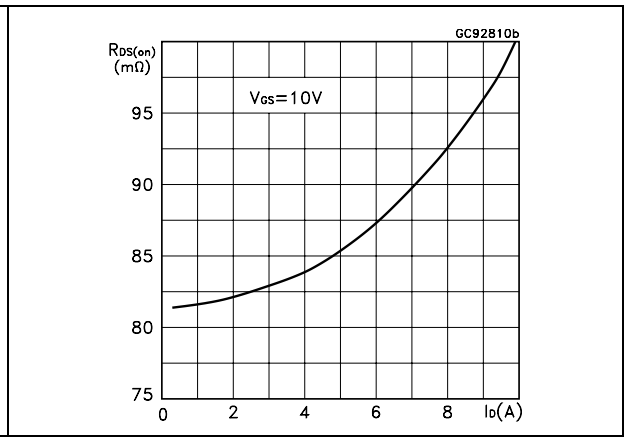


Figure 7. Gate charge vs gate-source voltage

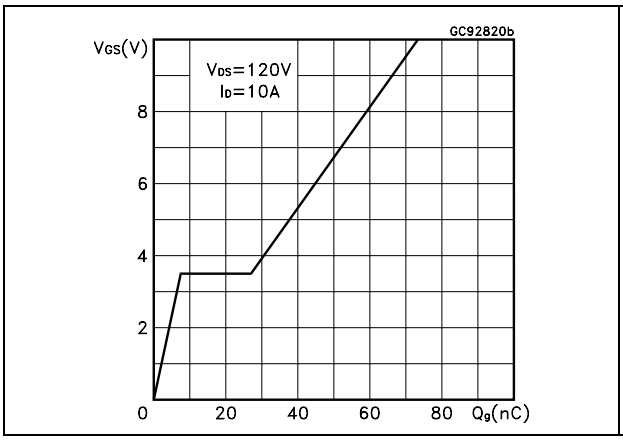


Figure 8. Capacitance variations

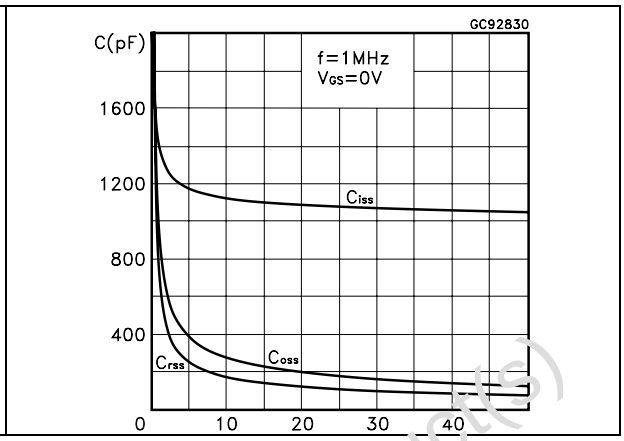


Figure 9. Normalized gate threshold voltage vs temperature

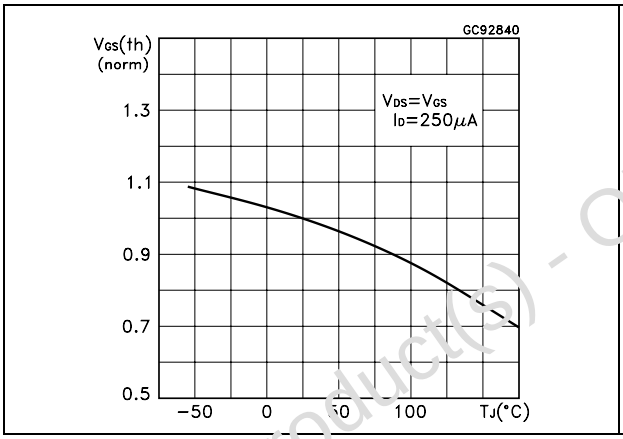


Figure 10. Normalized on resistance vs temperature

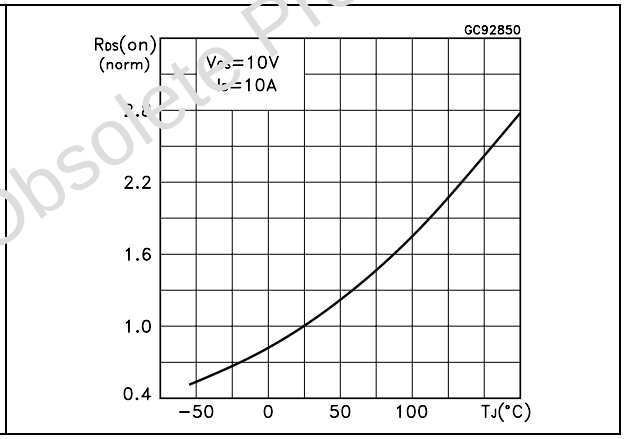


Figure 11. Normalized B_{VDSS} vs temperature

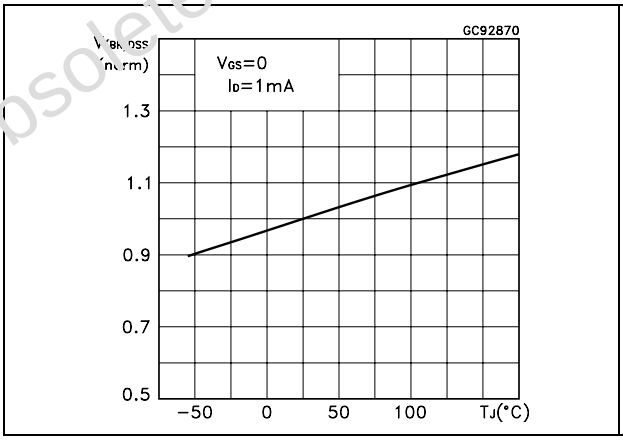
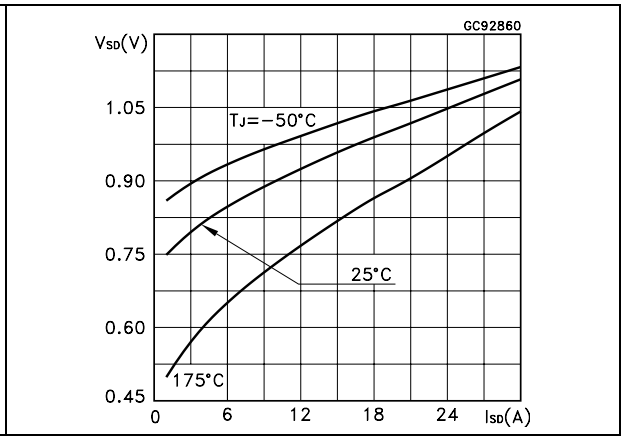


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

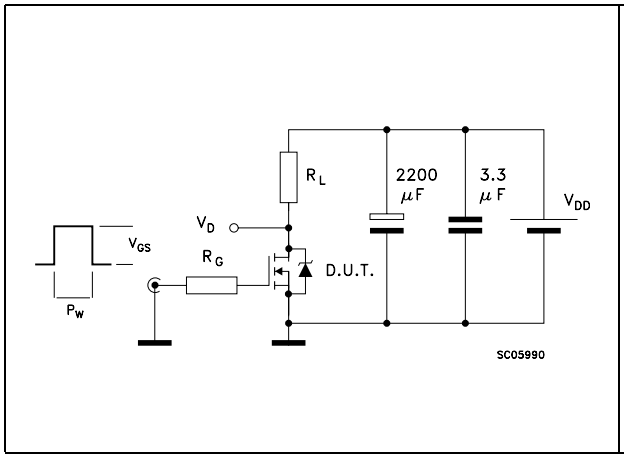


Figure 14. Gate charge test circuit

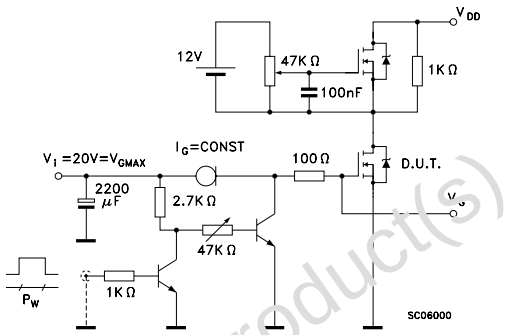


Figure 15. Test circuit for inductive load switching and diode recovery times

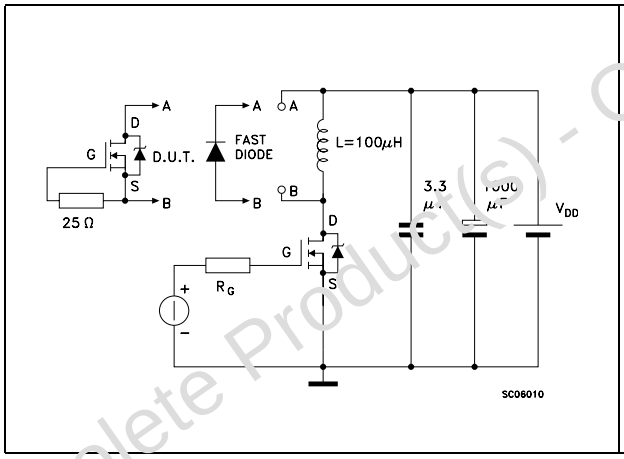


Figure 16. Unclamped Inductive load test circuit

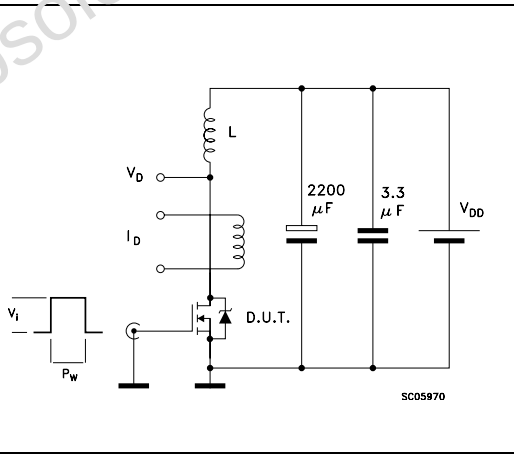


Figure 17. Unclamped inductive waveform

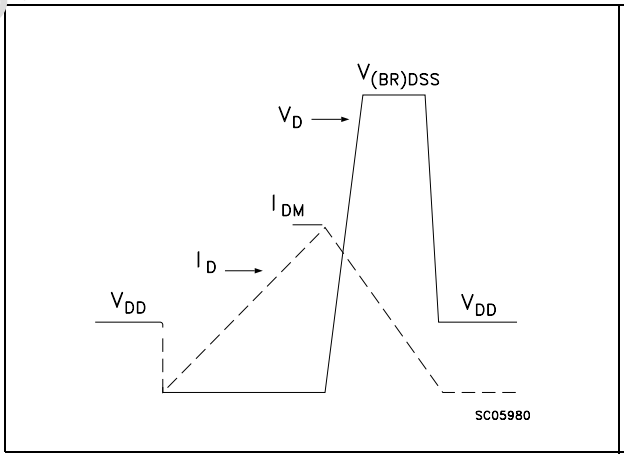
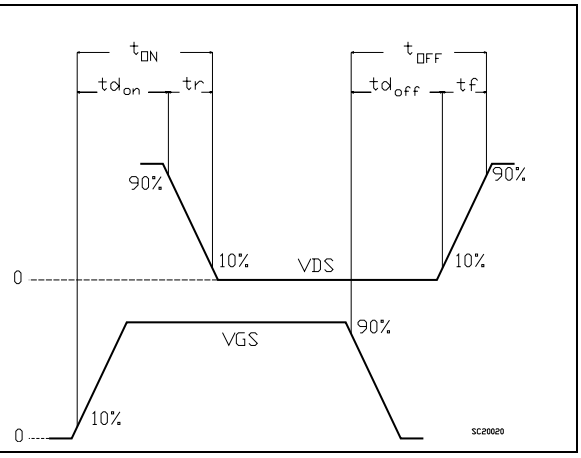


Figure 18. Switching time waveform

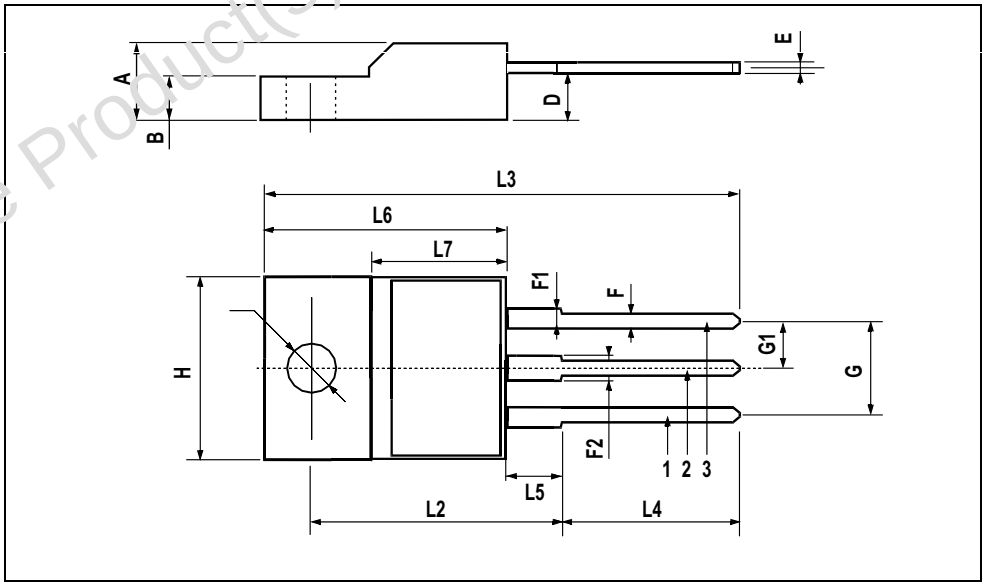


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



5 Revision history

Table 6. Revision history

Date	Revision	Changes
09-Sep-2004	2	Complete document
16-Aug-2006	3	New template, no content change

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