# SOCOT Project Summary

Consortium participants: KLA-Tencor (Israel), IMEC (Belgium), ST Agrate (Italy), QWED (Poland)

SOCOT project goal: To develop and validate in R&D and industrial environments a breakthrough technology for overlay control based on scatterometry

## ***Abstract***


The overlay control budget for the 32nm technology node will be approximately 10nm according to the ITRS. The overlay metrology budget is typically 1/10 of the overlay control budget resulting in overlay metrology performance requirements of 1nm. Theoretical considerations show that overlay technology based on *scatterometry* has inherent advantages, which will allow it to achieve this strict requirement and go beyond it.

We have demonstrated a breakthrough scatterometry overlay technology in preliminary proof-of-concept experiments. The results of these studies are promising, and at this early stage position scatterometry as one of the leading contenders for the overlay technology for the 32nm node and beyond. We propose to carry out a thorough and detailed research program with the goal of transforming the promising concept into a well developed technology, which meets the most strict overlay control requirements of the future.

The anticipated outcome of the project is an optimal methodology for a scatterometry overlay tool design, target design and algorithms, which allow overlay control with a significantly improved Total Measurement Uncertainty (TMU) and reduced systematic bias with respect to device structures, on layers fabricated with the most advanced processes and materials.

We will achieve this through extensive research in target design including the design and fabrication of a dedicated reticle. Extensive measurements of selected targets will be carried out on both R&D and production wafers. The project will also involve a substantial amount of simulations of the lithography process and of the scatterometry signal.

The success of the project will be ensured through a very close collaboration of the leading overlay metrology company worldwide with leading European research institution and semiconductor manufacturer. This consortium will augment the European leadership in the microelectronics industry.

**Project steps:**

1. Definition of validation methodology
    a. Definition of the methodology to validate the scatterometry overlay concept
    b. Methodology of comparison of the performance of the scatterometry overlay control technology to other types of measurements
2. Target geometry
    a. Selection of appropriate geometries for overlay targets
    b. Target design
    c. Design of two R&D reticles
3. Development of research scatterometer
    a. Development of scatterometry overlay software and integration with imaging software
    b. Integration of a scatterometry overlay capabilities with imaging based on Archer platform
    c. Construction of three research scatterometers
4. Algorithm development
    a. Development of algorithms for overlay calculation from scatterometry signals for all target geometries
    b. Testing of the algorithms using simulations
    c. Algorithm improvement
5. Simulation capabilities development
    a. Investigation of several approaches for EM simulations from periodic structures
    b. Simulation software development and optimisation for scatterometry overlay targets
6. Concept validation in R&D environment
    a. Preparation of two R&D reticle sets
    b. Wafer fabrication
    c. Scatterometry overlay measurements
    d. Analysis of scatterometry overlay TMU and correctables
    e. Comparison of scatterometry overlay with imaging
    f. Comparison of scatterometry with CD-SEM
7. Concept validation in industrial environment
    a. Preparation of end-user reticle set
    b. Wafer fabrication
    c. Scatterometry overlay measurements
    d. Analysis of scatterometry overlay TMU and correctables
    e. Comparison of scatterometry overlay with imaging
    f. Comparison of scatterometry with alternative techniques