



Introduction

To meet the demand for more performance, complexity and cost reduction, the semiconductor industry develops microcontrollers with both high density design technology and higher clock frequencies. This has intrinsically increased the potential noise emission and noise sensitivity.

Therefore, application developers must now apply EMC “hardening” techniques in the design of firmware, PCB layout and at system level.

This application note is intended for application designers who need to reach the optimum level of EMC performance. It gives microcontroller EMC features and compliance standards.

This document only concentrates on STM8S features and behaviors. For general information on EMC for ST microcontrollers, refer to the “EMC design guide for ST microcontrollers” application note (AN1709).

General recommendations for STM8S devices are summarized in the “Getting started with the STM8S” application note (AN2752). This document also provides basic EMC recommendations.

Related documents

AN1015: Software techniques for improving microcontroller EMC performance

AN1709: EMC design guide for ST microcontrollers

AN2752: Getting started with the STM8S

RM0016: STM8S microcontroller family

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1 STM8S: designed for EMC robustness

Most STM8S product family applications require a high level of robustness. The STM8S devices have been designed to meet this requirement with a cost effective approach.

The following built-in features have been implemented for this purpose:

- Independent watchdog (IWDG) and window watchdog (WWDG) to detect unexpected code execution, application behavior or code corruption
- Clock security system (CSS) to monitor external clock failures
- POR/BOR to make sure the microcontroller is properly supplied
- Critical registers complemented in order to prevent corruption
- Data EEPROM and Flash program memory which are write protected and which can only be unprotected by entering a key combination
- Built-in I/O protection diodes

All these features could not be efficient enough without following board design EMC recommendations.

2 Power supply

The STM8S product family is designed for standard applications in the 3.3 V to 5 V (+/-10%) supply voltage range.

All power pins must be connected: V_{DD}/V_{SS} , V_{DDA}/V_{SSA} , V_{DDIOx}/V_{SSIOx} .

The V_{CAP} pin is the regulator output. It provides the 1.8 V supply to the core and the peripherals. This pin must be decoupled with a 470 nF capacitor. If not, or if a wrong capacitor value is connected, the reset pin can toggle with a period of about 100 ms.

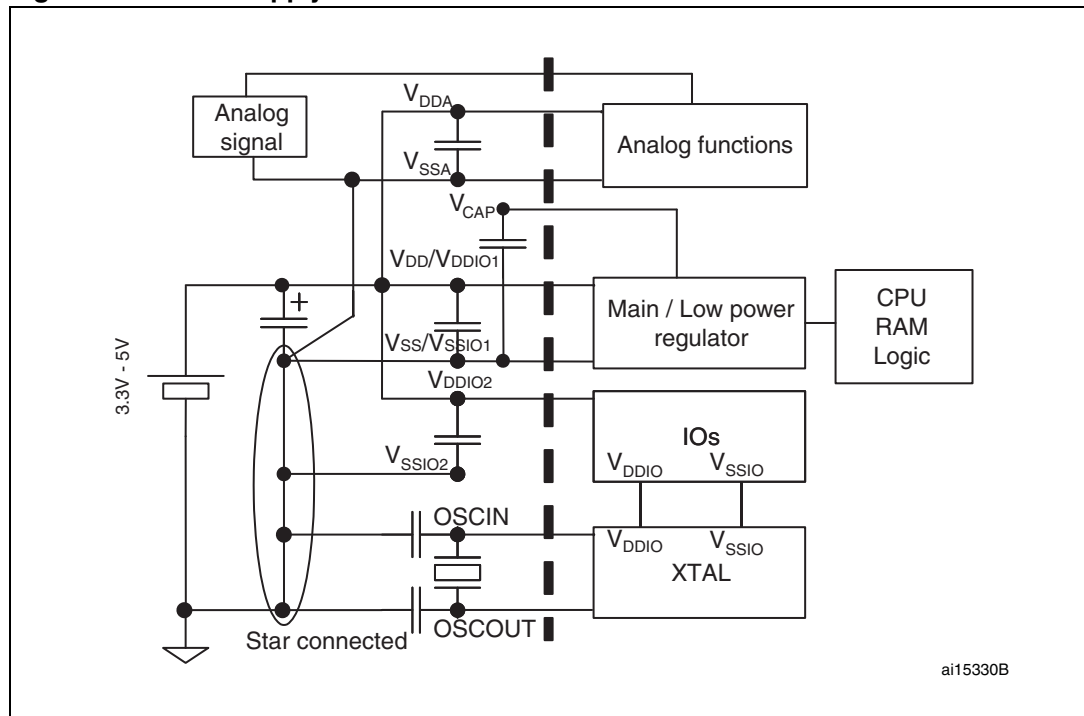
For products with separated V_{DD} and V_{DDIO1} , it is strongly recommended to connect both pins and decouple them with a single capacitor of 100 nF.

V_{DDA} and V_{DDIO2} , when present, must be decoupled with a dedicated 100 nF capacitor.

When designing the layout, all decoupling capacitors (including V_{CAP} capacitor) must be connected as close as possible to the V_{DD} , V_{DDA} , V_{DDIOx} and V_{CAP} pins.

Power supply connections are shown in the following diagram.

Figure 1. Power supply connections



ai15330B

3 Layout recommendations

The schematic diagram defines the appropriate bill of materials but, for EMC performance, special attention must be paid to the layout which defines ground plane, track width and length, etc.

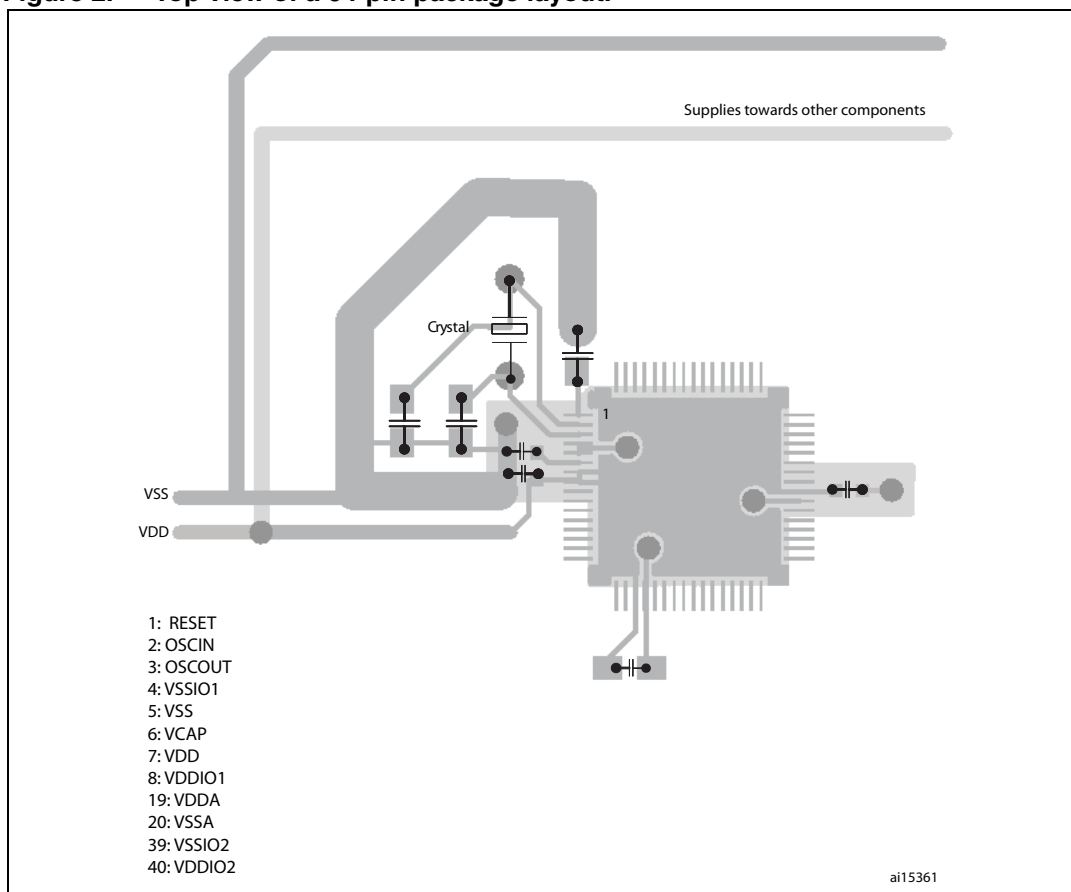
It is important to pay special attention to:

- the ground plane used as a shield below the device
- the supplies which must run around the device towards the other components (to avoid creating a second power supply way).
- the ground path between the capacitor-loaded resonator and V_{SS} which must be as short as possible.

3.1 Two-layer board

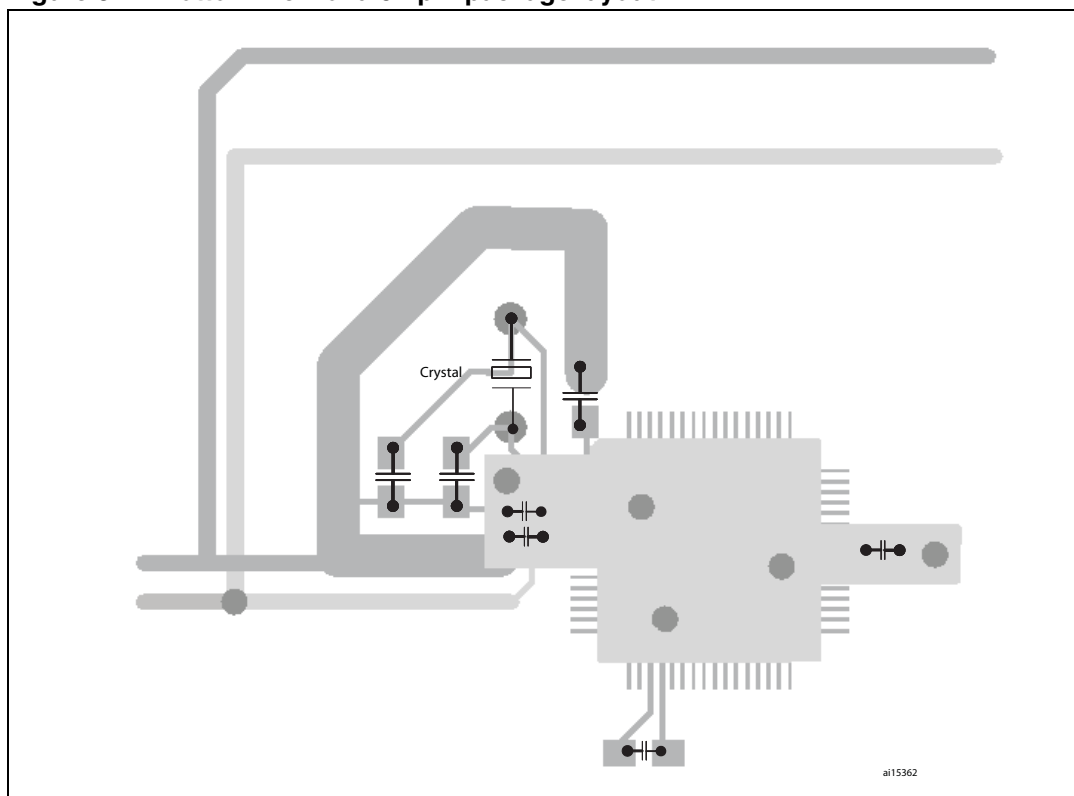
Due to the position of V_{DDIO2} and V_{SSIO2} , a two-layer board design is recommended for 44-pin package and above.

Figure 2. Top view of a 64-pin package layout.



Note: Grey: bottom side
Dark grey: top side

Figure 3. Bottom view of a 64-pin package layout

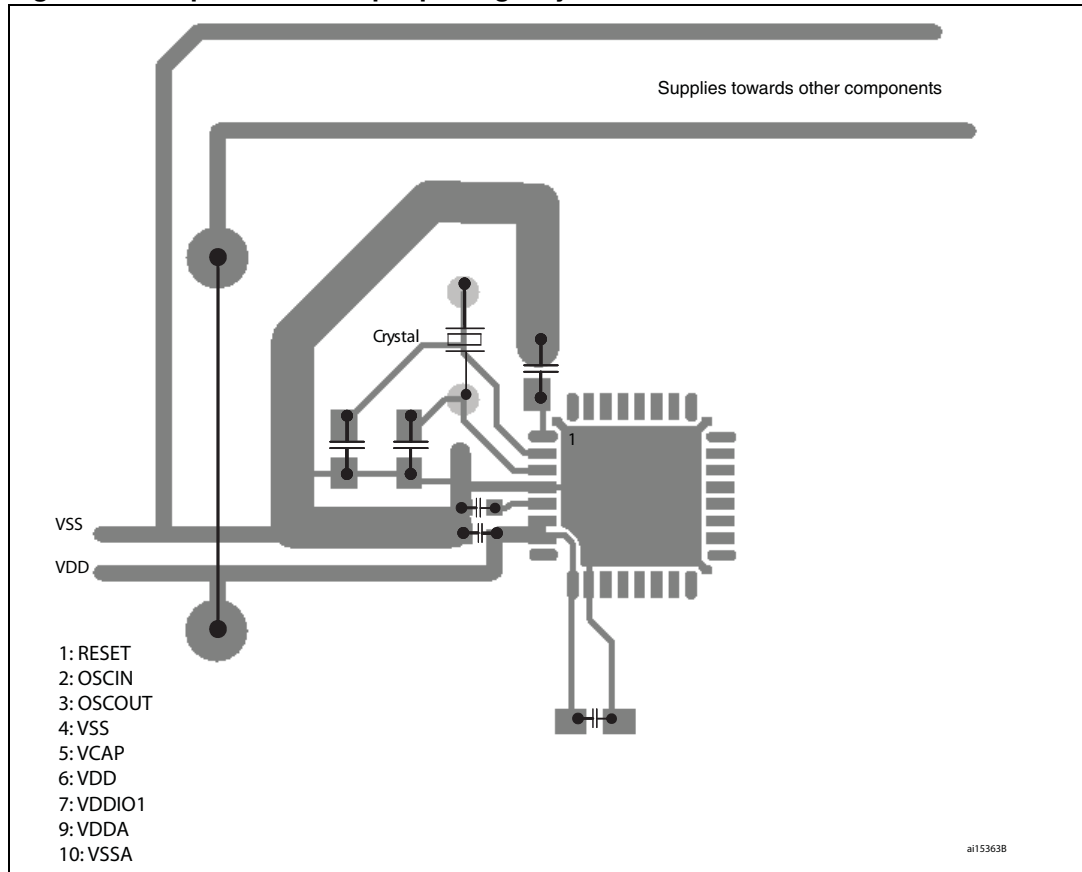


Note: Grey: bottom side
Dark grey: top side

3.2 Single layer board

For 32-pin package and below, a single layer board can offer a very good level of EMC performance.

Figure 4. Top view of a 32-pin package layout



4 EMC characteristics

EMC characteristics are specific to each device. Please refer to the Electrical characteristics section in the product datasheet for any information on these characteristics.

5 Software recommendations

The standard software techniques for improving EMC performance described in the AN1015 application note (“Software techniques for improving microcontroller EMC performance”) also apply to the STM8S product family.

This section lists the STM8S specificities related to the software techniques referred in the AN1015. It gives the values dedicated to STM8S products but it is strongly recommended to read carefully the AN1015 in order to implement safely the software recommendations.

5.1 Critical bytes

It is recommended to avoid occurrences of the following critical bytes in your code:

- 0x8E: opcode for HALT (instruction used to enter low power modes)
- 0x8F: opcode for WFI (instruction Wait For Interrupt)
- 0x82: opcode for INT (instruction used to jump in interrupt routine only)
- 0x8B: opcode for SWBRK (software breakpoint instruction used to stall the CPU in debug mode)

These critical bytes can be generated by the linker when computing the address destination in a branch instruction (JUMP or CALL) in absolute or relative addressing modes. To remove such occurrences you can simply insert a NOP instruction before the target address. For further explanation, refer to the AN1015 application note.

5.2 Illegal opcodes

To keep a better control of unexpected jumps, it is recommended to fill unused memory areas with TRAP opcode (0x83).

Besides, if you want to generate an illegal opcode reset, the simpler illegal opcodes are the following ones: 0x05, 0x0B, 0x71 and 0x75.

With pre-opcode, the list is longer:

- 0x7220..0x722F, 0x7231, 0x7232, 0x7235, 0x723B, 0x7241, 0x7242, 0x7245, 0x724B, 0x7251, 0x7252, 0x7255, 0x725B, 0x7261, 0x7262, 0x7265, 0x726B, 0x7280..0x728E, 0x7290..0x72A1, 0x72A3..0x72A8, 0x72AA..0x72AF, 0x72B1, 0x72B3..0x72B8, 0x72BA, 0x72BC..0x72BF, 0x72E0..0x72EF, 0x72F1, 0x72F3..0x72F8, 0x72FA, 0x72FC..0x72FF
- 0x9000, 0x9003..0x900F, 0x9020..0x9027, 0x902A, 0x902B, 0x9030..0x903F, 0x9041, 0x9045, 0x904B, 0x9051, 0x9055, 0x905B, 0x9061, 0x9065, 0x906B, 0x9071, 0x9072, 0x9075, 0x907B, 0x9080..0x9084, 0x9086..0x9088, 0x908A..0x908F, 0x9090..0x9092, 0x9098..0x909D, 0x90A0..0x90A2, 0x9090A4..0x90A6, 0x90A8..0x90AD, 0x90B0..0x90B2, 0x90B4..0x90BD, 0x90C0..0x90C2, 0x90C4..0x90CD
- 0x9100..0x915F, 0x9161, 0x9162, 0x9165, 0x916B, 0x9170..0x91A6, 0x91A8..0x91AE, 0x91B0..0x91C2, 0x91C4..0x91CD, 0x91E0, 0x91FF
- 0x9200..0x922F, 0x9231, 0x9232, 0x9235, 0x923B, 0x9240..0x925F, 0x9261, 0x9262, 0x9265, 0x926B, 0x9270..0x928C, 0x928E..0x92A6, 0x92A8..0x92AB, 0x92AD, 0x92AE, 0x92B0..0x92BB, 0x92BE, 0x92BF, 0x92E0..0x92FF.

5.3 Reset sources

Reset sources can be checked in the Reset status register RST_SR (at address 0x50B3). The different reset sources which can be identified through the Reset status register are:

- EMC reset,
- SWIM reset,
- Illegal opcode reset,
- Independent watchdog reset,
- Window watchdog reset.

Each of these flags can be cleared by software by writing 1 into the corresponding bit location. They can also all be cleared by a power-on reset.

For a description of these reset sources, please refer to the STM8S microcontroller family reference manual (RM0016).

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
13-Jan-2009	1	Initial release.
27-Jan-2009	2	<i>Figure 4: Top view of a 32-pin package layout on page 7</i> modified : capacitors moved (pins 5 and 7).

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