



Low-cost free-to-air satellite set-top box decoder

Data Brief

Feature summary

- Enhanced ST20 32-bit VL-RISC CPU
 - 200 MHz, single cycle cache, 4-Kbyte instruction cache, 4-Kbyte data cache, 2-Kbyte SRAM
- Unified memory interface
 - Up to 166 MHz, 16-bit wide SDRAM interface
- Serial flash interface
 - Serial flash support (SPI/SSC)
- Embedded DVB-S QPSK demodulator
 - Fast channel acquisition
 - Compatible with direct conversion tuners
 - Digital carrier and timing recovery loops
 - Up to 60 Msps operation
 - Automatic spectral inversion ambiguity resolution
 - Digital cancellation of ADC offset
 - Digital nyquist root filter
- External transport stream input
 - Support for DVB transport streams
- MPEG-2 MP at ML video decoder
 - Fully programmable horizontal and vertical SRCs
- PAL/NTSC/SECAM encoder
 - RGB, CVBS, Y/C and YUV outputs with four 10-bit DAC outputs. RGB/CVBS or YUV/CVBS or YC/CVBS
 - Encoding of CGMS, Teletext, WSS, VPS and closed caption
- Graphics/display
 - Blitter-based display compositor
 - 8 bpp CLUT graphics, 256 x 30-bit (AYCbCr) CLUT entries or 16-bit true color graphics, RGB565 and ARGB1555 formats. Link-list control
 - 2-D paced blitter engine with fill function
 - Multiple channel presentation

- Audio subsystem
 - MPEG-1 layers I/II
 - Direct voltage, single ended, stereo audio DAC
- Central DMA controller
- On-chip peripherals
 - One ASC (UART) with Tx and Rx FIFOs
 - Three 8-bit banks of parallel I/O and one 7-bit bank
 - Two SSCs for I²C/SPI master/slave interfaces
 - Infrared transmitter/receiver
 - Integrated VCXO
 - Low-power RTC watchdog controller
- JTAG/TAP interface
- Package TQFP176 20 mm x 20 mm.

Order codes

Part number	Package
STx5188	TQFP176

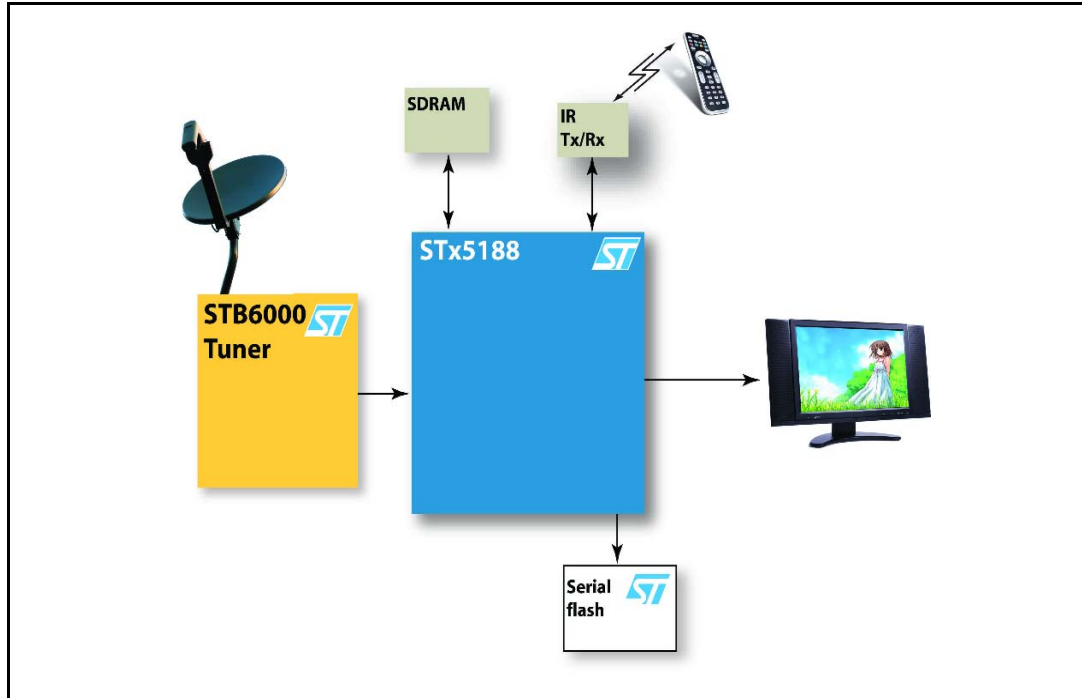
Description

Leader in the low-cost FTA satellite market, STMicroelectronics introduces its latest, low-cost highly integrated solution for the retail market.

Offering a direct migration path from the STx5118/STV0288 platform, The STx5188 uses the same set of IPs, thereby facilitating the porting from previous generations. It is based on the ST-interconnect architecture and the popular ST20 CPU running at 200 MHz, and comes with a serial flash interface. The embedded QPSK demodulator guarantees fast satellite scan times thanks to the blind scan algorithm and a direct connection to zero-IF tuners.

Description (continued)

The STx5188 also includes audio DACs capable of direct connection to the TV input and the capability to operate from the same clock as the STB6000. These cost reductions have been made without compromising ST quality standards and performance: 2-D graphics engine, faster CPU and built-in flexible DMA have been integrated.

STx5188 application diagram

Revision history

Table 1. Document revision history

Date	Revision	Description of changes
10-Mar-2006	1	First release.

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