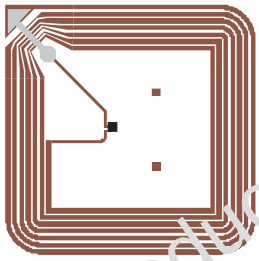
SRIX512

13.56 MHz short range contactless memory chip with 512-bit EEPROM, anticollision and anticlone functions

Not For New Design

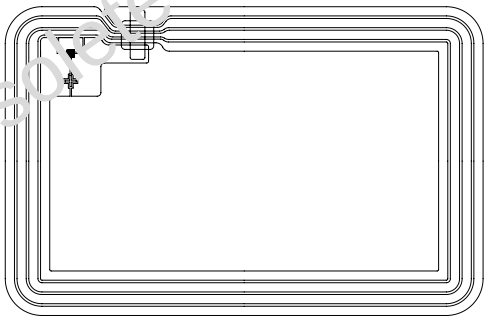
Features

- ISO 14443-2 Type B air interface compliant
- ISO 14443-3 Type B frame format compliant
- 13.56 MHz carrier frequency
- 847 kHz subcarrier frequency
- 106 Kbit/second data transfer
- France telecom proprietary anticlone function
- 8 bit Chip_ID based anticollision system
- 2 count-down binary counters with automated antitearing protection
- 64-bit unique identifier
- 512-bit EEPROM with Write Protect feature
- READ BLOCK and WRITE BLOCK (32 bits)
- Internal tuning capacitor
- 1 million ERASE/WRITE cycles
- 40-year data retention
- Self-timed programming cycle
- 5 ms typical programming time
- Packages
  - ECOPACK® (RoHS compliant)

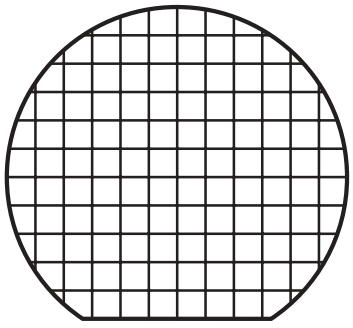


Antenna (A3)

Antenna (A4)



Antenna (A5)



Wafer

Contents

List of tables

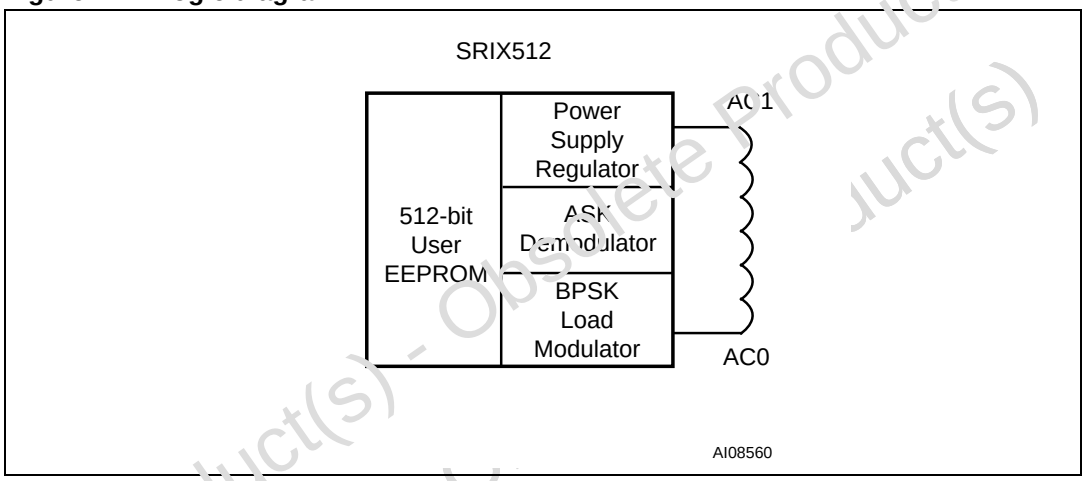
List of figures

1 Description

The SRIX512 is a contactless memory, powered by an externally transmitted radio wave. It contains a 512-bit user EEPROM fabricated with STMicroelectronics CMOS technology. The memory is organized as 16 blocks of 32 bits. The SRIX512 is accessed via the 13.56 MHz carrier. Incoming data are demodulated and decoded from the received amplitude shift keying (ASK) modulation signal and outgoing data are generated by load variation using Bit Phase Shift Keying (BPSK) coding of a 847 kHz subcarrier. The received ASK wave is 10% modulated. The Data transfer rate between the SRIX512 and the reader is 106 Kbit/s in both reception and emission modes.

The SRIX512 follows the ISO 14443-2 Type B recommendation for the radio-frequency power and signal interface.

Figure 1. Logic diagram



The SRIX512 is specifically designed for short range applications that need secure and re-usable products. The SRIX512 includes an anticollision mechanism that allows it to detect and select tags present at the same time within range of the reader. The anticollision is based on a probabilistic scanning method using slot markers. The SRIX512 provides an anticlone function which allows its authentication. Using the STMicroelectronics single chip coupler, CRX14, it is easy to design a reader with the authentication capability and to build a system with a high level of security.

Table 1. Signal names

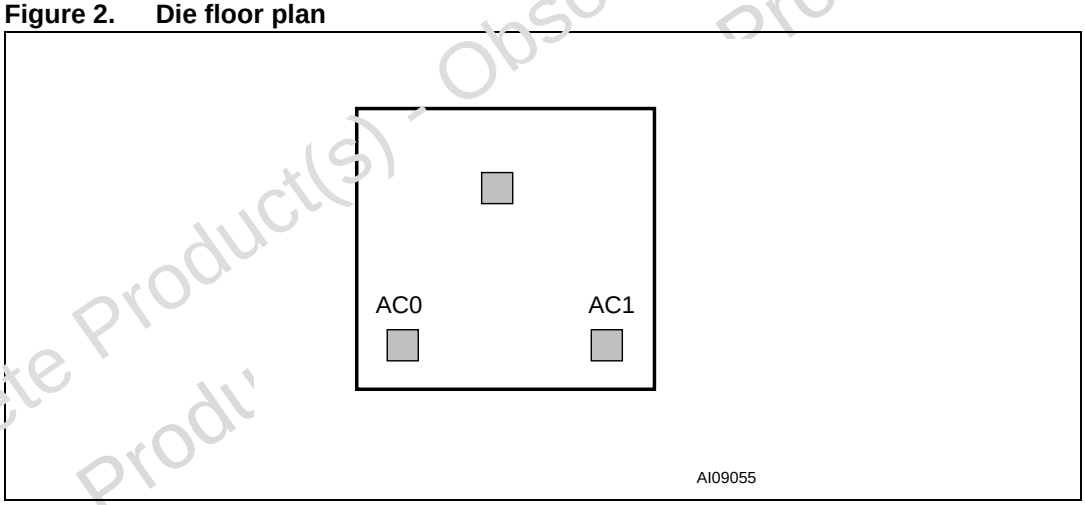
AC1	Antenna coil
AC0	Antenna coil

The SRIX512 contactless EEPROM can be randomly read and written in block mode (each block containing 32 bits). The instruction set includes the following ten commands:

- READ_BLOCK
- WRITE_BLOCK
- INITIATE
- PCALL16
- SLOT_MARKER
- SELECT
- COMPLETION
- RESET_TO_INVENTORY
- AUTHENTICATE
- GET_UID

The SRIX512 memory is organized in three areas, as described in *Table 3*. The first area is a resettable OTP (one time programmable) area in which bits can only be switched from 1 to 0. Using a special command, it is possible to erase all bits of this area to 1. The second area provides two 32-bit binary counters which can only be decremented from FFFF FFFFh to 0000 0000h, and gives a capacity of 4,294,967,296 units per counter. The last area is the EEPROM memory. It is accessible by block of 32 bits and includes an auto-erase cycle during each WRITE_BLOCK command.

Figure 2. Die floor plan



2 Signal description

2.1 AC1, AC0

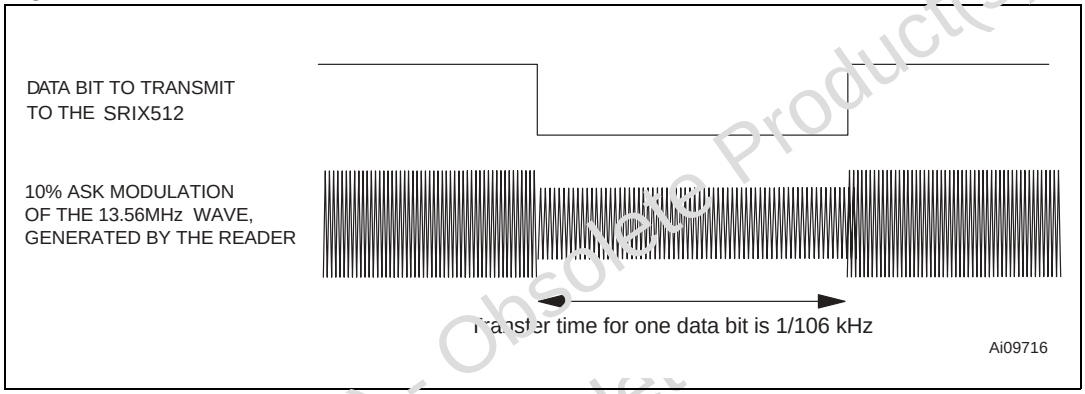
The pads for the Antenna Coil. AC1 and AC0 must be directly bonded to the antenna.

3 Data transfer

3.1 Input data transfer from the Reader to the SRIX512 (request frame)

The reader must generate a 13.56 MHz sinusoidal carrier frequency at its antenna, with enough energy to “remote-power” the memory. The energy received at the SRIX512’s antenna is transformed into a supply voltage by a regulator, and into data bits by the ASK demodulator. For the SRIX512 to decode correctly the information it receives, the reader must 10% amplitude-modulate the 13.56 MHz wave before sending it to the SRIX512. This is represented in *Figure 3*. The data transfer rate is 106 Kbits/s.

Figure 3. 10% ASK modulation of the received wave



3.1.1 Character transmission format for request frame

The SRIX512 transmits and receives data bytes as 10-bit characters, with the least significant bit (b0) transmitted first, as shown in *Figure 4*. Each bit duration, an ETU (Elementary Time Unit), is equal to 9.44 µs (1/106 kHz).

These characters, framed by a Start Of Frame (SOF) and an End Of Frame (EOF), are put together to form a Command Frame as shown in *Figure 10*. A frame includes an SOF, commands, addresses, data, a CRC and an EOF as defined in the ISO 14443-3 Type B Standard. If an error is detected during data transfer, the SRIX512 does not execute the command, but it does not generate an error frame.

Figure 4. SRIX512 request frame character format

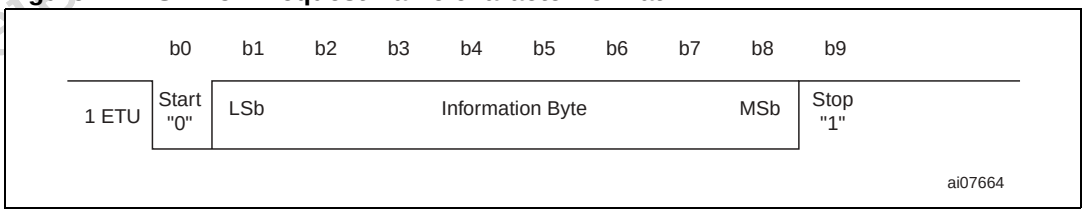


Table 2. Bit description

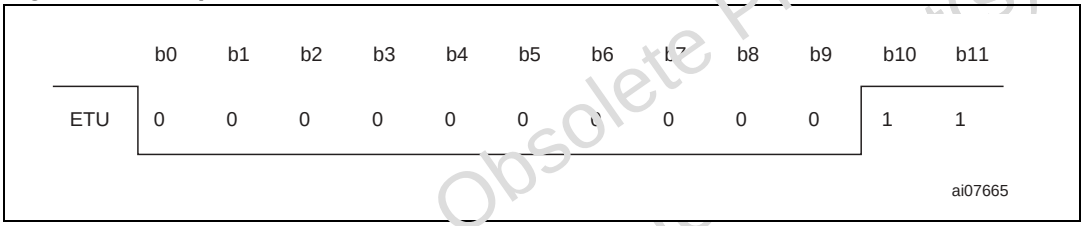
Bit	Description	Value
b_0	Start bit used to synchronize the transmission	$b_0 = 0$
b_1 to b_8	Information Byte (command, address or data)	The information byte is sent with the least significant bit first
b_9	Stop bit used to indicate the end of a character	$b_9 = 1$

3.1.2 Request start of frame

The SOF described in *Figure 5* is composed of:

- one falling edge,
- followed by 10 ETUs at logic-0,
- followed by a single rising edge,
- followed by at least 2 ETUs (and at most 3) at logic-1.

Figure 5. Request start of frame

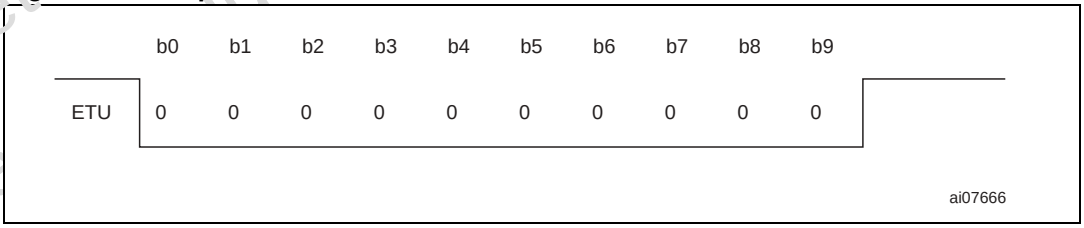


3.1.3 Request end of frame

The EOF shown in *Figure 6* is composed of:

- one falling edge,
- followed by 10 ETUs at logic-0,
- followed by a single rising edge.

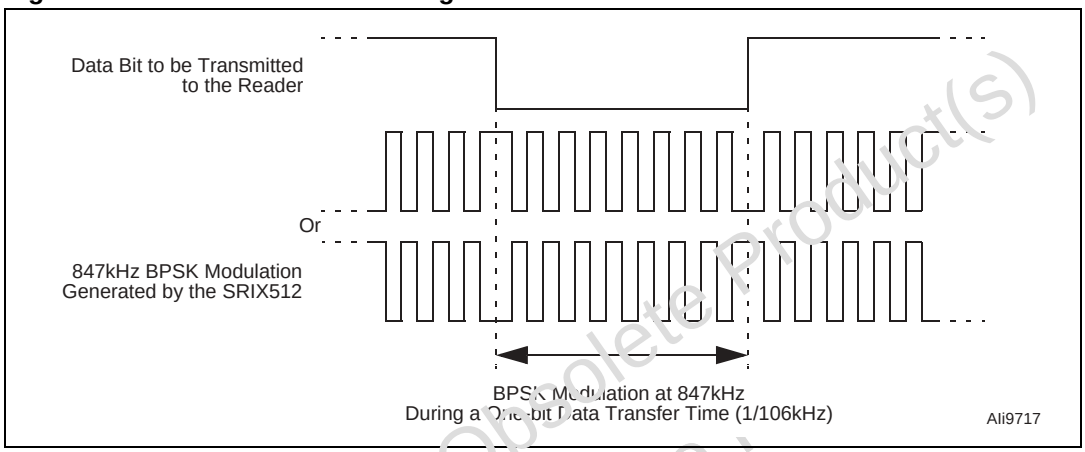
Figure 6. Request end of frame



3.2 Output data transfer from the SRIX512 to the reader (answer frame)

The data bits issued by the SRIX512 use retro-modulation. Retro-modulation is obtained by modifying the SRIX512 current consumption at the antenna (load modulation). The load modulation causes a variation at the reader antenna by inductive coupling. With appropriate detector circuitry, the reader is able to pick up information from the SRIX512. To improve load-modulation detection, data is transmitted using a BPSK encoded, 847 kHz subcarrier frequency f_S as shown in *Figure 7*, and as specified in the ISO 14443-2 Type B Standard.

Figure 7. Wave transmitted using BPSK subcarrier modulation



3.2.1 Character transmission format for answer frame

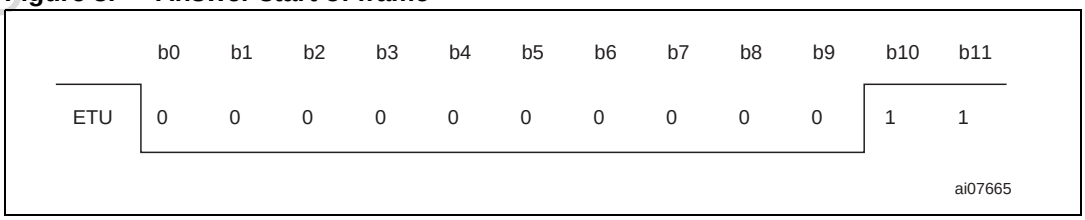
The character format is the same as for input data transfer (*Figure 4*). The transmitted frames are made up of an SOF, data, a CRC and an EOF (*Figure 10*). As with an input data transfer, if an error occurs, the reader does not issue an error code to the SRIX512, but it should be able to detect it and manage the situation. The data transfer rate is 106 Kbits/second.

3.2.2 Answer start of frame

The SOF described in *Figure 8* is composed of:

- followed by 10 ETUs at logic-0
- followed by 2 ETUs at logic-1

Figure 8. Answer start of frame

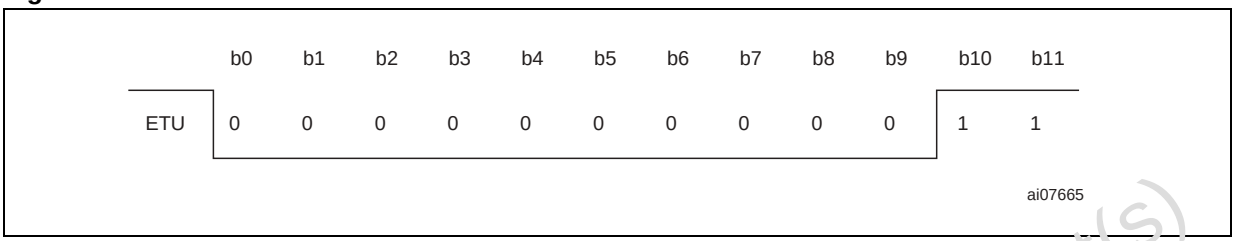


3.2.3 Answer end of frame

The EOF shown in *Figure 9* is composed of:

- followed by 10 ETUs at logic-0,
- followed by 2 ETUs at logic-1.

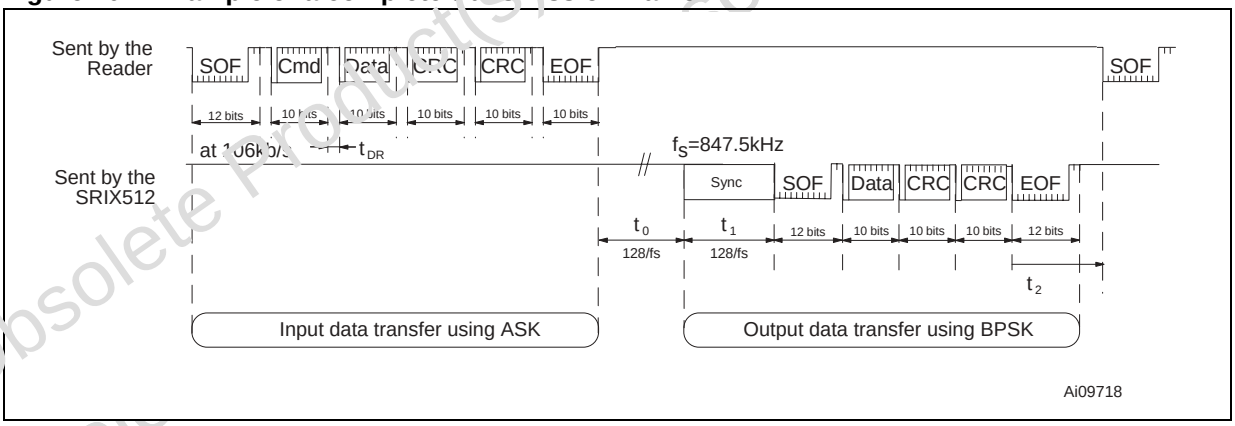
Figure 9. Answer end of frame



3.3 Transmission frame

Between the Request data transfer and the Answer data transfer, all ASK and BPSK modulations are suspended for a minimum time of $t_0 = 128/f_S$. This delay allows the reader to switch from Transmission to Reception mode. It is repeated after each frame. After t_0, the 13.56 MHz carrier frequency is modulated by the SRIX512 at 847 kHz for a period of $t_1 = 128/f_S$ to allow the reader to synchronize. After t_1, the first phase transition generated by the SRIX512 forms the start bit ('0') of the Answer SOF. After the falling edge of the Answer EOF, the reader waits a minimum time, t_2, before sending a new Request Frame to the SRIX512.

Figure 10. Example of a complete transmission frame



3.4 CRC

The 16-bit CRC used by the SRIX512 is generated in compliance with the ISO 14443 Type B recommendation. For further information, please see *Appendix A*. The initial register contents are all 1s: FFFFh.

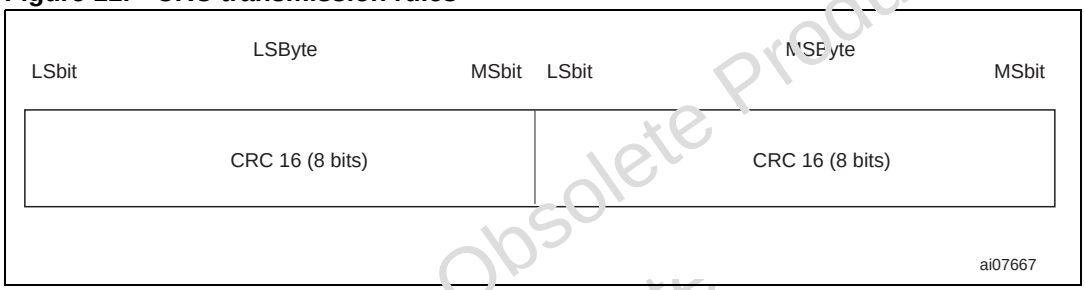
The two-byte CRC is present in every Request and in every Answer Frame, before the EOF. The CRC is calculated on all the bytes between SOF (not included) and the CRC field.

Upon reception of a Request from a reader, the SRIX512 verifies that the CRC value is valid. If it is invalid, the SRIX512 discards the frame and does not answer the reader.

Upon reception of an Answer from the SRIX512, the reader should verify the validity of the CRC. In case of error, the actions to be taken are the reader designer's responsibility.

The CRC is transmitted with the Least Significant Byte first and each byte is transmitted with the least significant bit first.

Figure 11. CRC transmission rules



4 Memory mapping

The SRIX512 is organized as 16 blocks of 32 bits as shown in *Table 3*. All blocks are accessible by the READ_BLOCK command. Depending on the write access, they can be updated by the WRITE_BLOCK command. A WRITE_BLOCK updates all the 32 bits of the block.

Table 3. SRIX512 memory mapping

Block Addr	Msb b_{31}	b_{24} b_{23}	32 bits Block b_{16} b_{15}	b_8 b_7	Lsb b_0	Description
0	32 bits Boolean Area					Resettable OTP bits
1	32 bits Boolean Area					
2	32 bits Boolean Area					
3	32 bits Boolean Area					
4	32 bits Boolean Area					
5	32 bits binary counter					Count down Counter
6	32 bits binary counter					
7	User Area					Lockable EEPROM
8	User Area					
9	User Area					
10	User Area					
11	User Area					
12	User Area					
13	User Area					
14	User Area					
15	User Area					

255	OTP_Lock_Reg	ST Reserved	Fixed Chip_ID (Option)	System OTP bits

UID0	64 bits UID Area	ROM
UID1		

4.1 Resettable OTP area

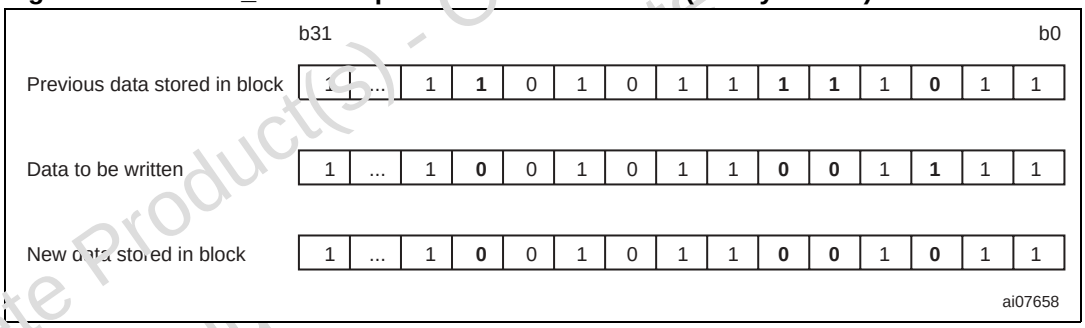
In this area contains five individual 32-bit Boolean Words (see *Figure 12* for a map of the area). A WRITE_BLOCK command will not erase the previous contents of the block as the Write cycle is not preceded by an Auto Erase cycle. This feature can be used to reset selected bits from 1 to 0. All bits previously at 0 remain unchanged. When the 32 bits of a block are all at 0, the block is empty, and cannot be updated any more. See *Figure 13* and *Figure 14* for examples of the result of the WRITE_BLOCK command in the resettable OTP area.

Figure 12. Resettable OTP area (addresses 0 to 4)

Block Address	MSb b31 b24 b23	32-bit Block b16 b15	b8 b7 LSb b0	Description
0	32-bit Boolean Area			Resettable OTP Bit
1	32-bit Boolean Area			
2	32-bit Boolean Area			
3	32-bit Boolean Area			
4	32-bit Boolean Area			

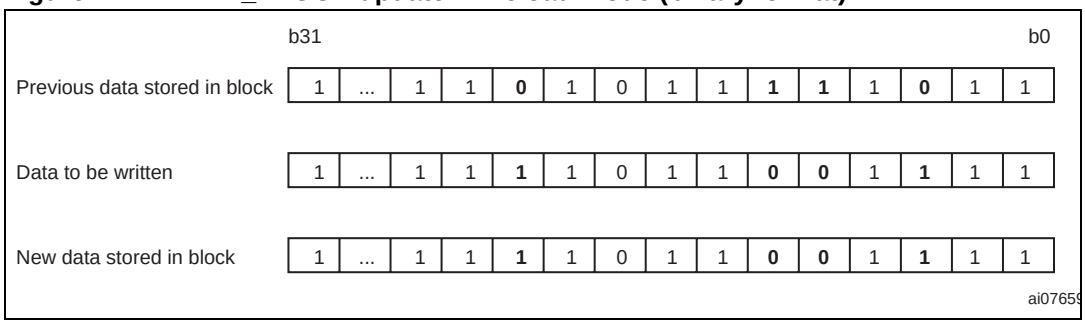
ai07657

Figure 13. WRITE_BLOCK update in Standard mode (binary format)



The five 32-bit blocks making up the Resettable OTP area can be erased in one go by adding an Auto Erase cycle to the WRITE_BLOCK command. An Auto Erase cycle is added each time the SRIX512 detects a Reload command. The Reload command is implemented through a specific update of the 32-bit binary counter located at block address 6 (see "*32-bit binary counters*" for details).

Figure 14. WRITE_BLOCK update in Reload mode (binary format)



4.2 32-bit binary counters

The two 32-bit binary counters located at block addresses 5 and 6, respectively, are used to count down from 2^{32} (4096 million) to 0. The SRIX512 uses dedicated logic that only allows the update of a counter if the new value is lower than the previous one. This feature allows the application to count down by steps of 1 or more. The initial value in Counter 5 is FFFF FFFEh, and is FFFF FFFFh in Counter 6. When the value displayed is 0000 0000h, the counter is empty and cannot be reloaded. The counter is updated by issuing the WRITE_BLOCK command to block address 5 or 6, depending on which counter is to be updated. The WRITE_BLOCK command writes the new 32-bit value to the counter block address. *Figure 16* shows examples of how the counters operate.

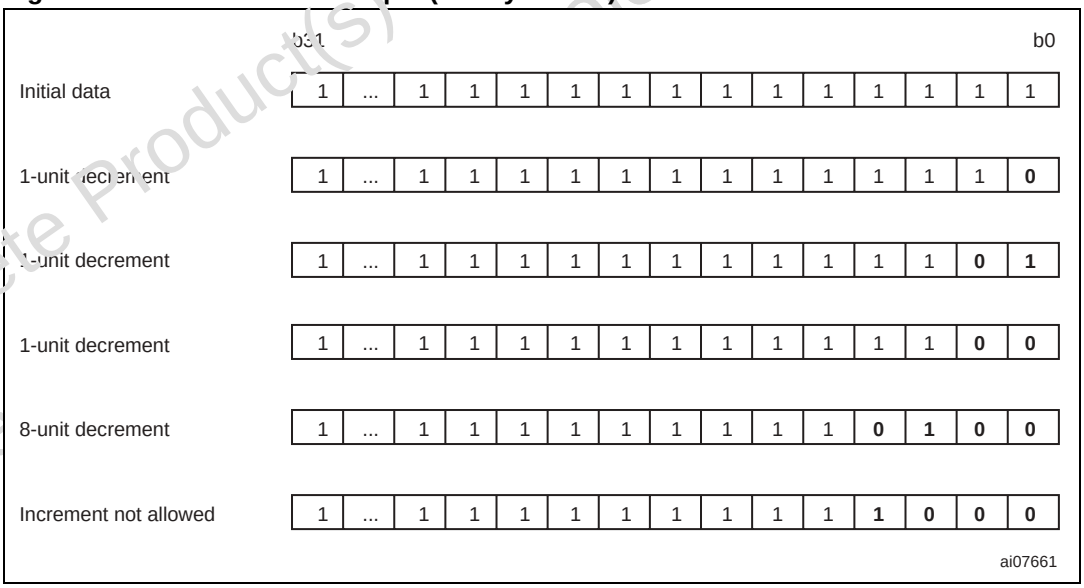
The counter programming cycles are protected by automated antitearing logic. This function allows the counter value to be protected in case of power down within the programming cycle. In case of power down, the counter value is not updated and the previous value continues to be stored.

Figure 15. Binary counter (addresses 5 to 6)

Block Address	MSb b31 b24 b23	32-bit Block b16 b15	b8 b7 LSb b0	Description
5	32-bit Binary Counter			Count down Counter
6	32-bit Binary Counter			

ai07660

Figure 16. Count down example (binary format)



ai07661

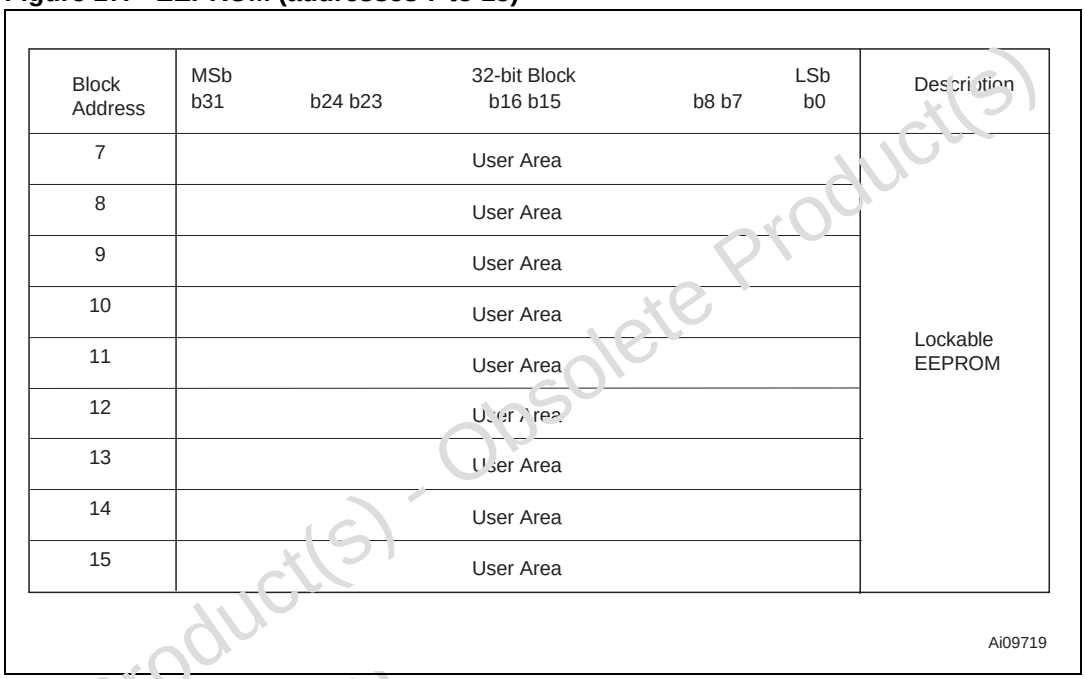
The counter with block address 6 controls the Reload command used to reset the resettable OTP area (addresses 0 to 4). Bits b_{31} to b_{21} act as an 11-bit Reload counter; whenever one of these 11 bits is updated, the SRIX512 detects the change and adds an Erase cycle to the WRITE_BLOCK command for locations 0 to 4 (see the "*Resettable OTP area*" paragraph). The Erase cycle remains active until a POWER-OFF or a SELECT command is issued. The SRIX512's resettable OTP area can be reloaded up to 2,047 times (2^{11}-1).

4.3 EEPROM area

The 9 blocks between addresses 7 and 15 are EEPROM blocks of 32 bits each (36 Bytes in total). (See *Figure 17* for a map of the area.) These blocks can be accessed using the READ_BLOCK and WRITE_BLOCK commands. The WRITE_BLOCK command for the EEPROM area always includes an Auto-Erase cycle prior to the Write cycle.

Blocks 7 to 15 can be Write-protected. Write access is controlled by the 8 bits of the OTP_Lock_Reg located at block address 255 (see "*OTP_Lock_Reg*" for details). Once protected, these blocks (7 to 15) cannot be unprotected.

Figure 17. EEPROM (addresses 7 to 15)

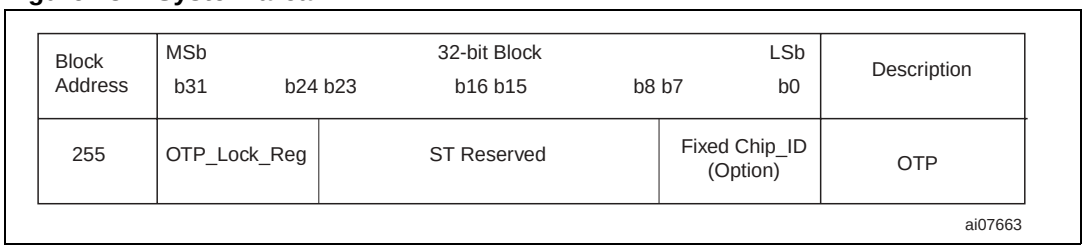


4.4 System area

This area is used to modify the settings of the SRIX512. It contains 3 registers: OTP_Lock_Reg, Fixed Chip_ID and ST Reserved. See *Figure 18* for a map of this area.

A WRITE_BLOCK command in this area will not erase the previous contents. Selected bits can thus be set from 1 to 0. All bits previously at 0 remain unchanged. Once all the 32 bits of a block are at 0, the block is empty and cannot be updated any more.

Figure 18. System area



4.4.1 OTP_Lock_Reg

The 8 bits, b_{31} to b_{24}, of the System Area (block address 255) are used as OTP_Lock_Reg bits in the SRIX512. They control the Write access to the 9 EEPROM blocks with addresses 7 to 15 as follows:

- When b_{24} is at 0, blocks 7 and 8 are Write-protected
- When b_{25} is at 0, block 9 is Write-protected
- When b_{26} is at 0, block 10 is Write-protected
- When b_{27} is at 0, block 11 is Write-protected
- When b_{28} is at 0, block 12 is Write-protected
- When b_{29} is at 0, block 13 is Write-protected
- When b_{30} is at 0, block 14 is Write-protected
- When b_{31} is at 0, block 15 is Write-protected.

The OTP_Lock_Reg bits cannot be erased. Once Write-protected, EEPROM blocks behave like ROM blocks and cannot be unprotected.

4.4.2 Fixed Chip_ID (option)

The SRIX512 is provided with an anticollision feature based on a random 8-bit Chip_ID. Prior to selecting an SRIX512, an anticollision sequence has to be run to search for the Chip_ID of the SRIX512. This is a very flexible feature, however the searching loop requires time to run.

For some applications, much time could be saved by knowing the value of the SRIX512 Chip_ID beforehand, so that the SRIX512 can be identified and selected directly without having to run an anticollision sequence. This is why the SRIX512 was designed with an optional mask setting used to program a fixed 8-bit Chip_ID to bits b_7 to b_0 of the system area. When the fixed Chip_ID option is used, the random Chip_ID function is disabled.

5 SRIX512 operation

All commands, data and CRC are transmitted to the SRIX512 as 10-bit characters using ASK modulation. The start bit of the 10 bits, b_0, is sent first. The command frame received by the SRIX512 at the antenna is demodulated by the 10% ASK demodulator, and decoded by the internal logic. Prior to any operation, the SRIX512 must have been selected by a SELECT command. Each frame transmitted to the SRIX512 must start with a Start Of Frame, followed by one or more data characters, two CRC Bytes and the final End Of Frame. When an invalid frame is decoded by the SRIX512 (wrong command or CRC error), the memory does not return any error code.

When a valid frame is received, the SRIX512 may have to return data to the reader. In this case, data is returned using BPSK encoding, in the form of 10-bit characters framed by an SOF and an EOF. The transfer is ended by the SRIX512 sending the 2 CRC Bytes and the EOF.

6 SRIX512 states

The SRIX512 can be switched into different states. Depending on the current state of the SRIX512, its logic will only answer to specific commands. These states are mainly used during the anticollision sequence, to identify and to access the SRIX512 in a very short time. The SRIX512 provides 6 different states, as described in the following paragraphs and in *Figure 19*.

6.1 POWER-OFF state

The SRIX512 is in POWER-OFF state when the electromagnetic field around the tag is not strong enough. In this state, the SRIX512 does not respond to any command.

6.2 READY state

When the electromagnetic field is strong enough, the SRIX512 enters the READY state. After Power-up, the Chip_ID is initialized with a random value. The whole logic is reset and remains in this state until an INITIATE() command is issued. Any other command will be ignored by the SRIX512.

6.3 INVENTORY state

The SRIX512 switches from the READY to the INVENTORY state after an INITIATE() command has been issued. In INVENTORY state, the SRIX512 will respond to any anticollision commands: INITIATE(), PCALL16() and SLOT_MARKER(), and then remain in the INVENTORY state. It will switch to the SELECTED state after a SELECT(Chip_ID) command is issued if the Chip_ID in the command matches its own. If not, it will remain in INVENTORY state.

6.4 SELECTED state

In SELECTED state, the SRIX512 is active and responds to all READ_BLOCK(), WRITE_BLOCK(), AUTHENTICATE() and GET_UID() commands. When an SRIX512 has entered the SELECTED state, it no longer responds to anticollision commands. So that the reader can access another tag, the SRIX512 can be switched to the DESELECTED state by sending a SELECT(Chip_ID2) with a Chip_ID that does not match its own, or it can be placed in DEACTIVATED state by issuing a COMPLETION() command. Only one SRIX512 can be in SELECTED state at a time.

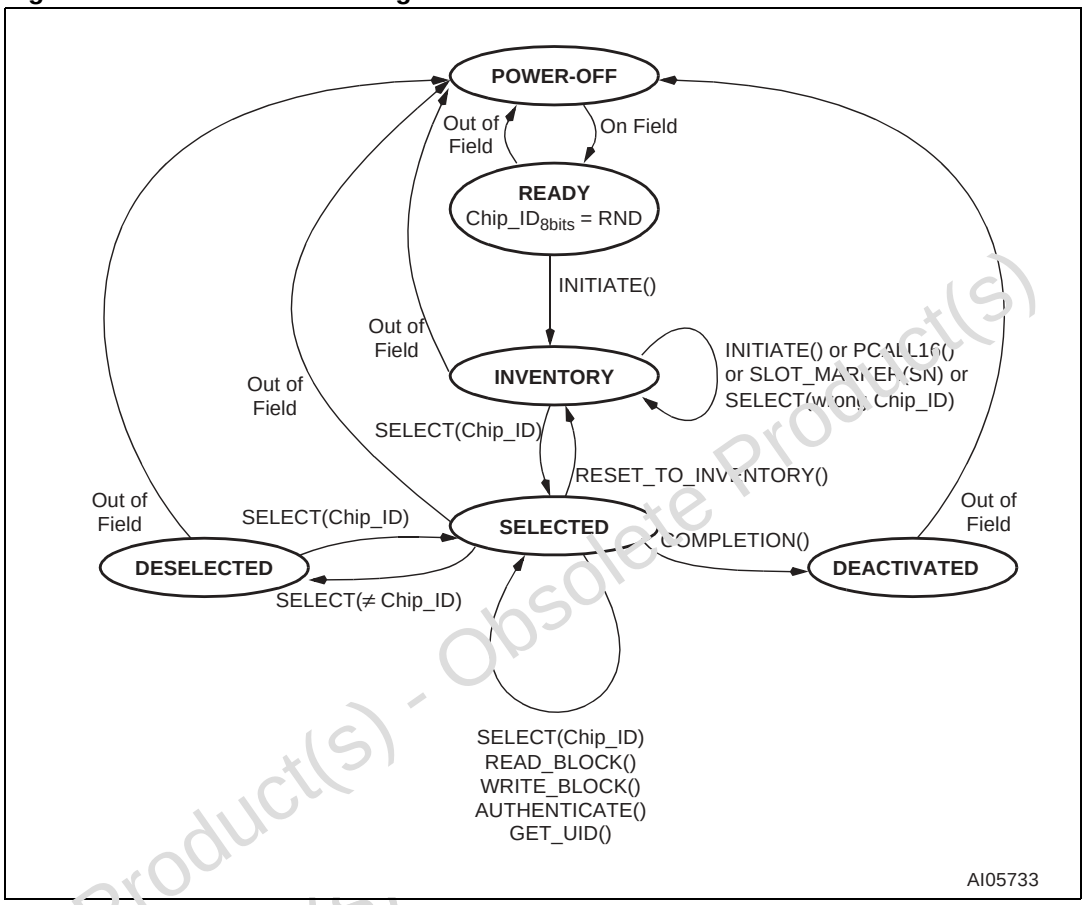
6.5 DESELECTED state

Once the SRIX512 is in DESELECTED state, only a SELECT(Chip_ID) command with a Chip_ID matching its own can switch it back to SELECTED state. All other commands are ignored.

6.6 DEACTIVATED state

When in this state, the SRIX512 can only be turned off. All commands are ignored.

Figure 19. State transition diagram



7 Anticollision

The SRIX512 provides an anticollision mechanism that searches for the Chip_ID of each device that is present in the reader field range. When known, the Chip_ID is used to select an SRIX512 individually, and access its memory. The anticollision sequence is managed by the reader through a set of commands described in the "*SRIX512 operation*" section:

- INITIATE()
- PCALL16()
- SLOT_MARKER().

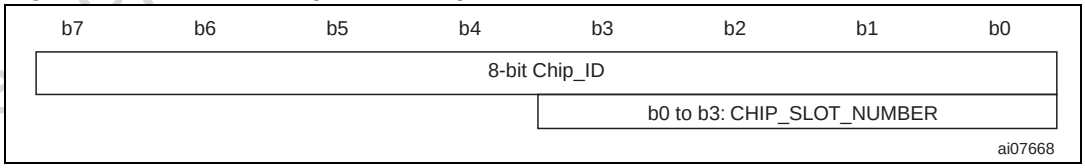
The reader is the master of the communication with one or more SRIX512 device(s). It initiates the tag communication activity by issuing an INITIATE(), PCALL16() or SLOT_MARKER() command to prompt the SRIX512 to answer. During the anticollision sequence, it might happen that two or more SRIX512 devices respond simultaneously, so causing a collision. The command set allows the reader to handle the sequence, to separate SRIX512 transmissions into different time slots. Once the anticollision sequence has completed, SRIX512 communication is fully under the control of the reader, allowing only one SRIX512 to transmit at a time.

The anticollision scheme is based on the definition of time slots during which the SRIX512 devices are invited to answer with minimum identification data: the Chip_ID. The number of slots is fixed at 16 for the PCALL16() command. For the INITIATE() command, there is no slot and the SRIX512 answers after the command is issued. SRIX512 devices are allowed to answer only once during the anticollision sequence. Consequently, even if there are several SRIX512 devices present in the reader field, there will probably be a slot in which only one SRIX512 answers, allowing the reader to capture its Chip_ID. Using the Chip_ID, the reader can then establish a communication channel with the identified SRIX512. The purpose of the anticollision sequence is to allow the reader to select one SRIX512 at a time.

The SRIX512 is given an 8-bit Chip_ID value used by the reader to select only one among up to 256 tags present within its field range. The Chip_ID is initialized with a random value during the READY state, or after an INITIATE() command in the INVENTORY state.

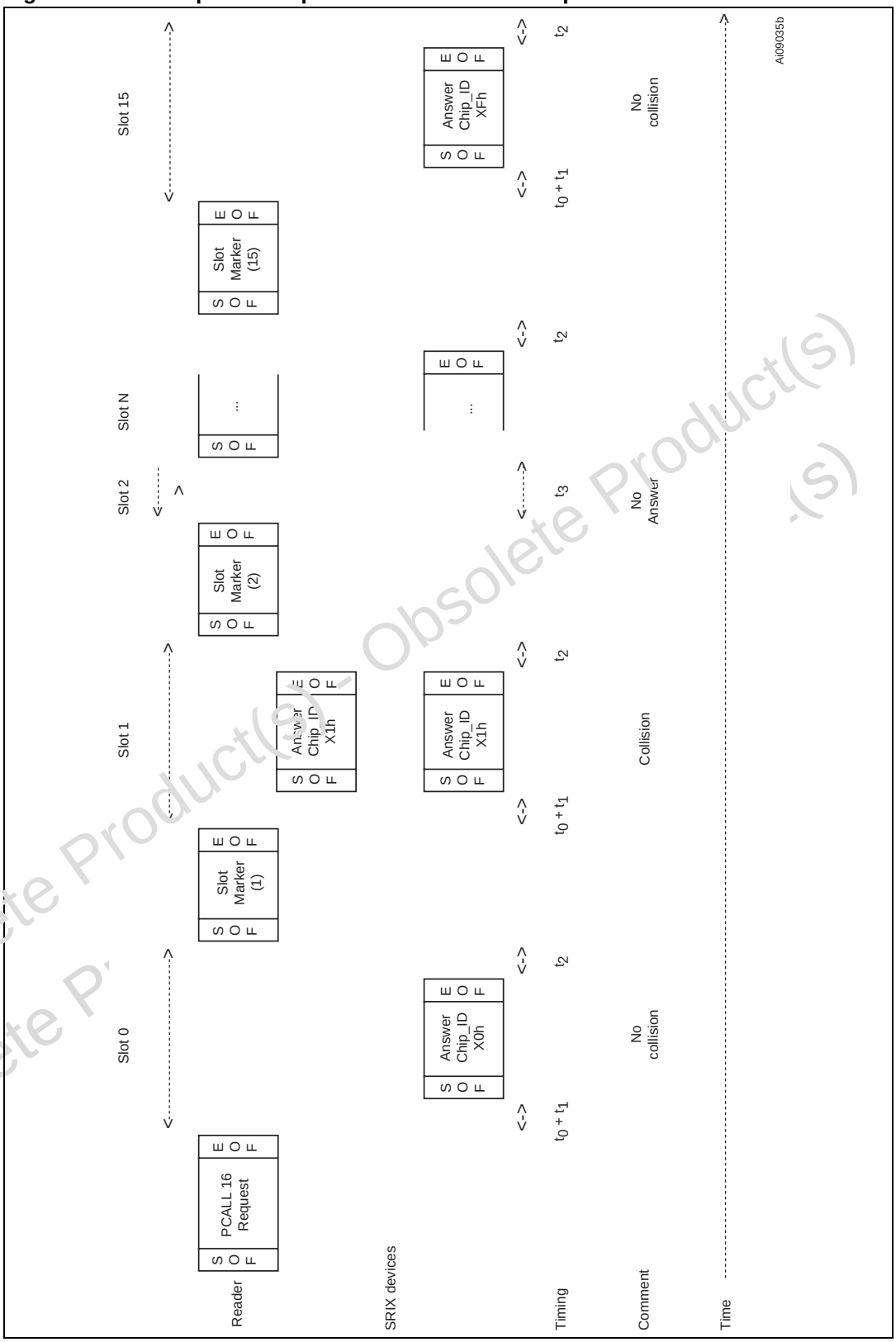
The four least significant bits (b_0 to b_3) of the Chip_ID are also known as the CHIP_SLOT_NUMBER. This 4-bit value is used by the PCALL16() and SLOT_MARKER() commands during the anticollision sequence in the INVENTORY state.

Figure 20. SRIX512 Chip_ID description



Each time the SRIX512 receives a PCALL16() command, the CHIP_SLOT_NUMBER is given a new 4-bit random value. If the new value is 0000_b, the SRIX512 returns its whole 8-bit Chip_ID in its answer to the PCALL16() command. The PCALL16() command is also used to define the slot number 0 of the anticollision sequence. When the SRIX512 receives the SLOT_MARKER(SN) command, it compares its CHIP_SLOT_NUMBER with the SLOT_NUMBER parameter (SN). If they match, the SRIX512 returns its Chip_ID as a response to the command. If they do not, the SRIX512 does not answer. The SLOT_MARKER(SN) command is used to define all the anticollision slot numbers from 1 to 15.

Figure 21. Description of a possible anticollision sequence



1. The value X in the Answer Chip_ID means a random hexadecimal character from 0 to F.

7.1 Description of an anticollision sequence

The anticollision sequence is initiated by the INITIATE() command which triggers all the SRIX512 devices that are present in the reader field range, and that are in INVENTORY state. Only SRIX512 devices in INVENTORY state will respond to the PCALL16() and SLOT_MARKER(SN) anticollision commands.

A new SRIX512 introduced in the field range during the anticollision sequence will not be taken into account as it will not respond to the PCALL16() or SLOT_MARKER(SN) command (READY state). To be considered during the anticollision sequence, it must have received the INITIATE() command and entered the INVENTORY state.

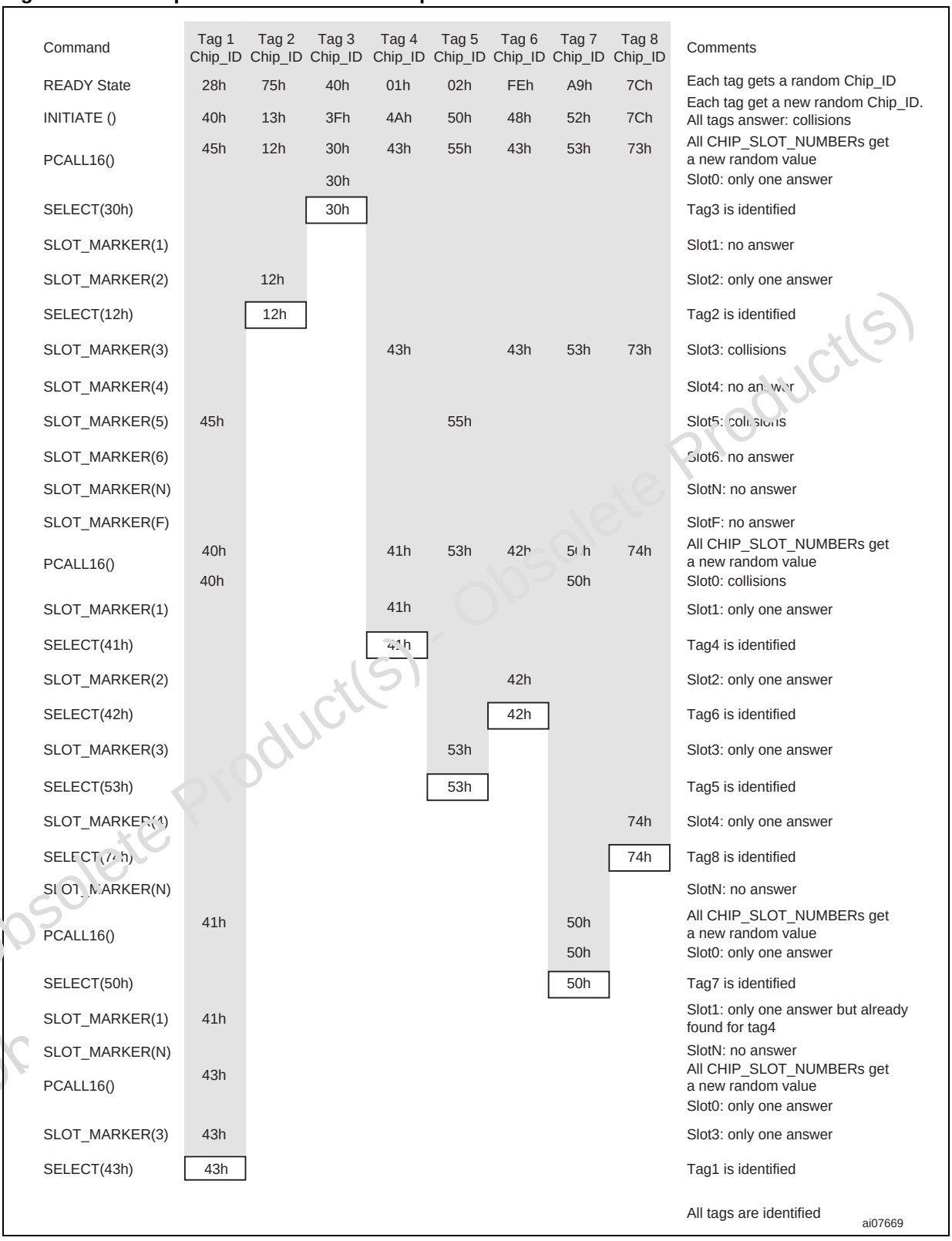
Table 4 shows the elements of a standard anticollision sequence. (See *Figure 22* for an example.)

Table 4. Standard anticollision sequence

Step 1	Init:	Send INITIATE(). – If no answer is detected, go to step1. – If only 1 answer is detected, select and access the SRIX512. After accessing the SRIX512, deselect the tag and go to step1. – If a collision (many answers) is detected, go to step2.
Step 2	Slot 0	Send PCALL16(). – If no answer or collision is detected, go to step3. – If 1 answer is detected, store the Chip_ID, Send SELECT() and go to step3.
Step 3	Slot 1	Send SLOT_MARKER(1). – If no answer or collision is detected, go to step4. – If 1 answer is detected, store the Chip_ID, Send SELECT() and go to step4.
Step 4	Slot 2	Send SLOT_MARKER(2). – If no answer or collision is detected, go to step5. – If 1 answer is detected, store the Chip_ID, Send SELECT() and go to step5.
Step N	Slop N	Send SLOT_MARKER(3 up to 14) ... – If no answer or collision is detected, go to stepN+1. – If 1 answer is detected, store the Chip_ID, Send SELECT() and go to stepN+1.
Step 17	Slot 15	Send SLOT_MARKER(15). – If no answer or collision is detected, go to step18. – If 1 answer is detected, store the Chip_ID, Send SELECT() and go to step18.
Step 18		All the slots have been generated and the Chip_ID values should be stored into the reader memory. Issue the SELECT(Chip_ID) command and access each identified SRIX512 one by one. After accessing each SRIX512, switch them into DESELECTED or DEACTIVATED state, depending on the application needs. – If collisions were detected between Step2 and Step17, go to Step2. – If no collision was detected between Step2 and Step17, go to Step1.

After each SLOT_MARKER() command, there may be several, one or no answers from the SRIX512 devices. The reader must handle all the cases and store all the Chip_IDs, correctly decoded. At the end of the anticollision sequence, after SLOT_MARKER(15), the reader can start working with one SRIX512 by issuing a SELECT() command containing the desired Chip_ID. If a collision is detected during the anticollision sequence, the reader has to generate a new sequence in order to identify all unidentified SRIX512 devices in the field. The anticollision sequence can stop when all SRIX512 devices have been identified.

Figure 22. Example of an anticollision sequence



8 Anticlone function

The SRIX512 provides an anticlone function that allows the application to authentication the device. This function uses reserved data that is stored in the SRIX512 memory at its time of manufacture.

The Authentication system is based on a proprietary challenge/response mechanism which allows the application software to authenticate any member of the secure memory tag SRXxxx family from STMicroelectronics (of which the SRIX512 is the prime example). A reader system, based on the ST CRX14 chip coupler, can check each SRIX512 tag for authenticity, and protect the application system against silicon copies or emulators.

A complete description of the Authentication system is available under Non Disclosure Agreement (NDA) with STMicroelectronics. For more details about this SRIX512 function, please contact your nearest STMicroelectronics sales office.

9 SRIX512 commands

See the paragraphs below for a detailed description of the Commands available on the SRIX512. The commands and their hexadecimal codes are summarized in *Table 5*. A brief is given in *Appendix B*.

Table 5. Command code

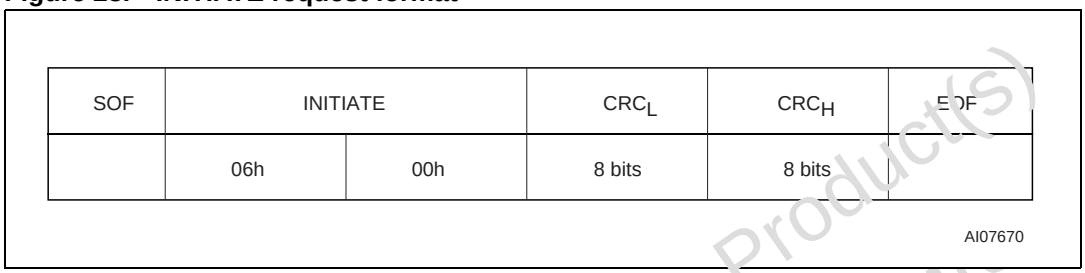
Hexadecimal code	Command
06h-00h	INITIATE()
06h-04h	PCALL16()
x6h	SLOT_MARKER (SN)
08h	READ_BLOCK(Addr)
09h	WRITE_BLOCK(Addr, Data)
0Ah	AUTHENTICATE(RND)
0Bh	GET_UID()
0Ch	RESET_TO_INVENTORY
0Eh	SELECT(Chip_ID)
0Fh	COMPLETION()

9.1 INITIATE() command

Command Code = 06h - 00h

INITIATE() is used to initiate the anticollision sequence of the SRIX512. On receiving the INITIATE() command, all SRIX512 devices in READY state switch to INVENTORY state, set a new 8-bit Chip_ID random value, and return their Chip_ID value. This command is useful when only one SRIX512 in READY state is present in the reader field range. It speeds up the Chip_ID search process. The CHIP_SLOT_NUMBER is not used during INITIATE() command access.

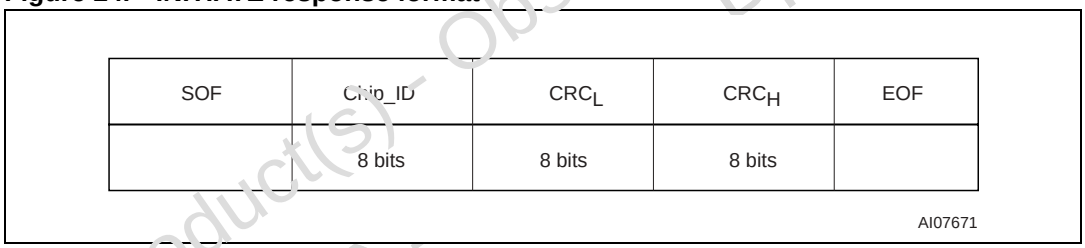
Figure 23. INITIATE request format



Request parameter:

- No parameter

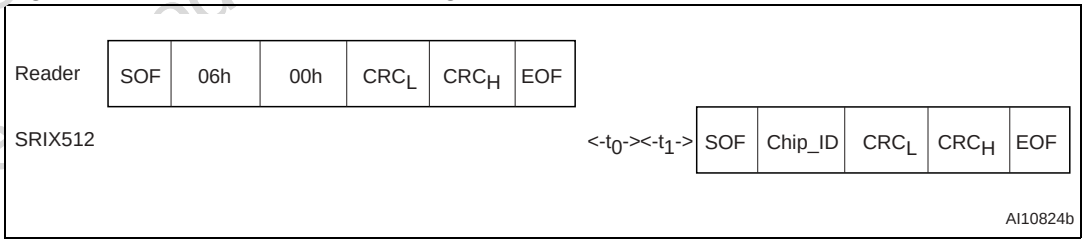
Figure 24. INITIATE response format



Response parameter:

- Chip_ID of the SRIX512

Figure 25. INITIATE frame exchange between Reader and SRIX512



9.2 PCALL16() command

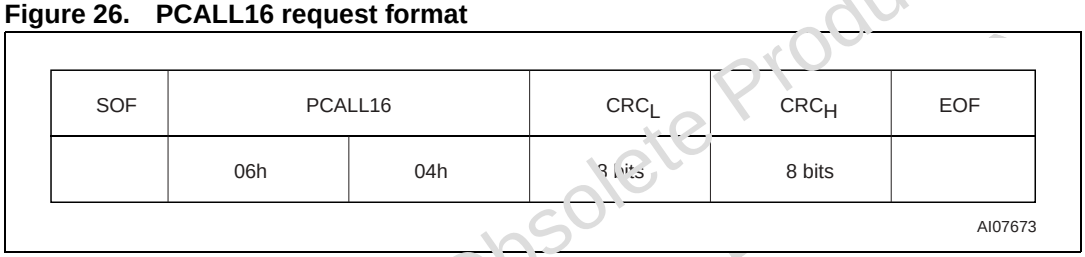
Command Code = 06h - 04h

The SRIX512 must be in INVENTORY state to interpret the PCALL16() command.

On receiving the PCALL16() command, the SRIX512 first generates a new random CHIP_SLOT_NUMBER value (in the 4 least significant bits of the Chip_ID). CHIP_SLOT_NUMBER can take on a value between 0 an 15 (1111_b). The value is retained until a new PCALL16() or INITIATE() command is issued, or until the SRIX512 is powered off. The new CHIP_SLOT_NUMBER value is then compared with the value 0000_b. If they match, the SRIX512 returns its Chip_ID value. If not, the SRIX512 does not send any response.

The PCALL16() command, used together with the SLOT_MARKER() command, allows the reader to search for all the Chip_IDs when there are more than one SRIX512 device in INVENTORY state present in the reader field range.

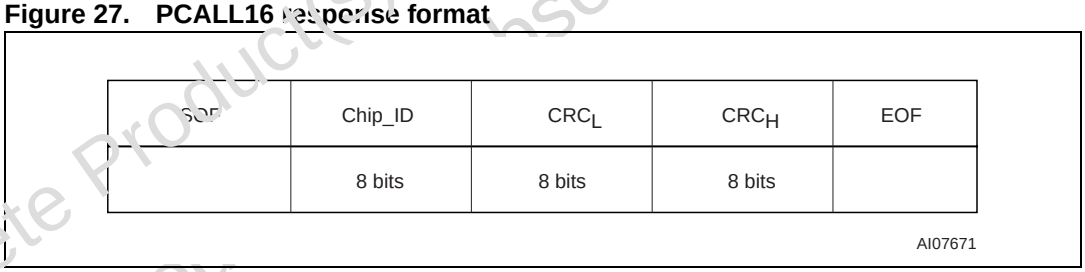
Figure 26. PCALL16 request format



Request parameter:

- No parameter

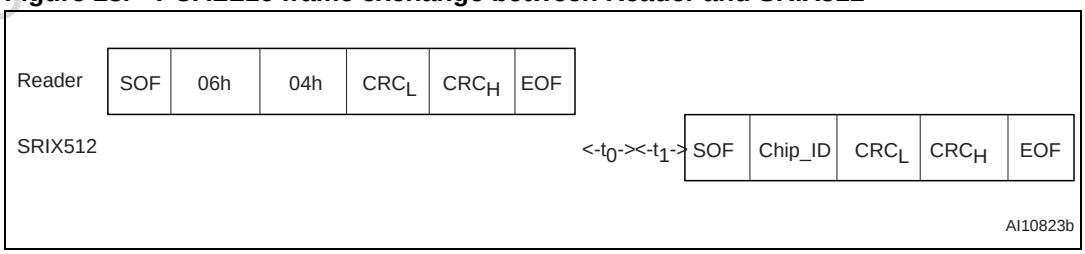
Figure 27. PCALL16 response format



Response parameter:

- Chip_ID of the SRIX512

Figure 28. PCALL16 frame exchange between Reader and SRIX512



9.3 SLOT_MARKER(SN) command

Command Code = x6h

The SRIX512 must be in INVENTORY state to interpret the SLOT_MARKER(SN) command.

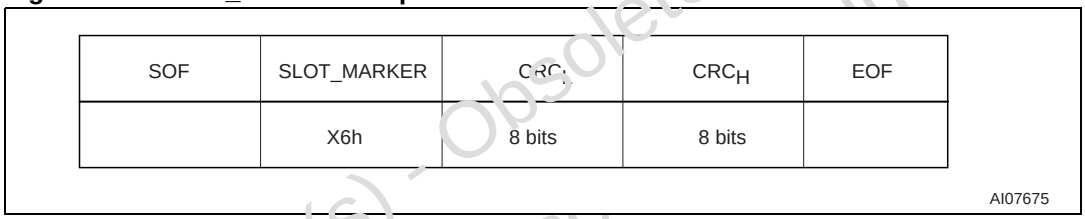
The SLOT_MARKER Byte code is divided into two parts:

- b_3 to b_0: 4-bit command code with fixed value 6.
- b_7 to b_4: 4 bits known as the SLOT_NUMBER (SN). They assume a value between 1 and 15. The value 0 is reserved by the PCALL16() command.

On receiving the SLOT_MARKER() command, the SRIX512 compares its CHIP_SLOT_NUMBER value with the SLOT_NUMBER value given in the command code. If they match, the SRIX512 returns its Chip_ID value. If not, the SRIX512 does not send any response.

The SLOT_MARKER() command, used together with the PCALL16() command, allows the reader to search for all the Chip_IDs when there are more than one SRIX512 device in INVENTORY state present in the reader field range.

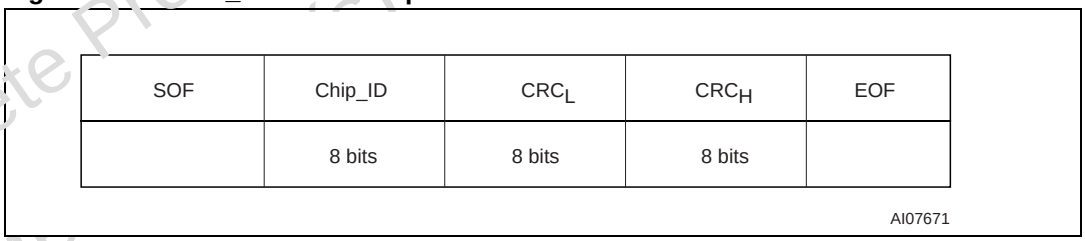
Figure 29. SLOT_MARKER request format



Request parameter:

- x: Slot number

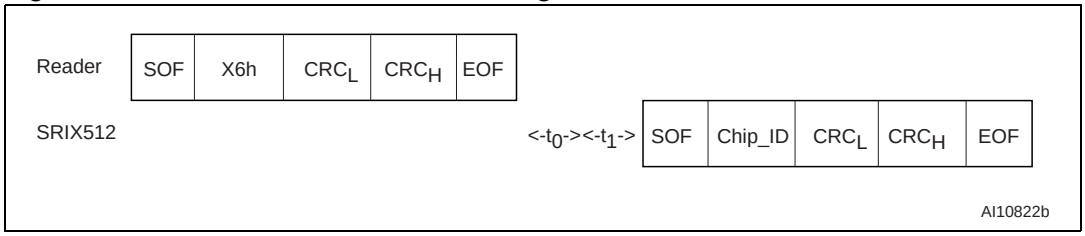
Figure 30. SLOT_MARKER response format



Response parameters:

- Chip_ID of the SRIX512

Figure 31. SLOT_MARKER frame exchange between Reader and SRIX512



9.4 SELECT(Chip_ID) command

Command Code = 0Eh

The SELECT() command allows the SRIX512 to enter the SELECTED state. Until this command is issued, the SRIX512 will not accept any other command, except for INITIATE(), PCALL16() and SLOT_MARKER(). The SELECT() command returns the 8 bits of the Chip_ID value. An SRIX512 in SELECTED state, that receives a SELECT() command with a Chip_ID that does not match its own is automatically switched to DESELECTED state.

Figure 32. SELECT request format

SOF	SELECT	Chip_ID	CRC_L	CRC_H	EOF
	0Eh	8 bits	8 bits	8 bits	

AI07677

Request parameter:

- 8-bit Chip_ID stored during the anticollision sequence

Figure 33. SELECT response format

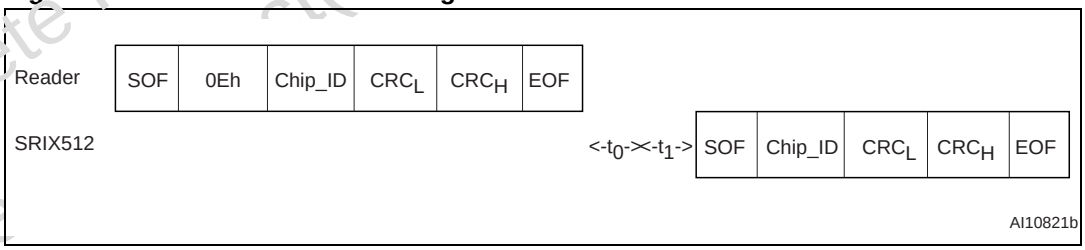
SOF	Chip_ID	CRC_L	CRC_H	EOF
	8 bits	8 bits	8 bits	

AI07671

Response parameters:

- Chip_ID of the selected tag. Must be equal to the transmitted Chip_ID

Figure 34. SELECT frame exchange Between Reader and SRIX512



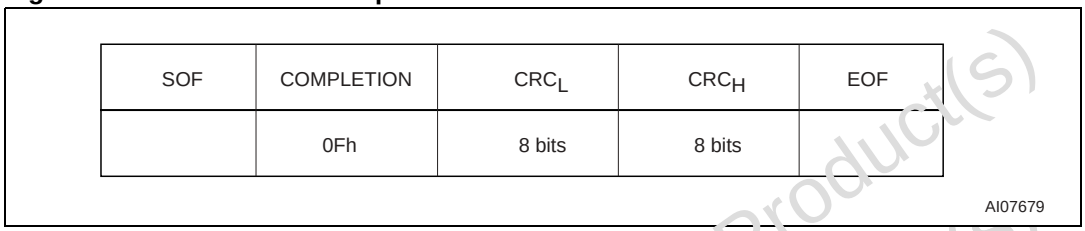
9.5 COMPLETION() command

Command Code = 0Fh

On receiving the COMPLETION() command, a SRIX512 in SELECTED state switches to DEACTIVATED state and stops decoding any new commands. The SRIX512 is then locked in this state until a complete reset (tag out of the field range). A new SRIX512 can thus be accessed through a SELECT() command without having to remove the previous one from the field. The COMPLETION() command does not generate a response.

All SRIX512 devices not in SELECTED state ignore the COMPLETION() command.

Figure 35. COMPLETION request format



Request parameters:

- No parameter

Figure 36. COMPLETION response format

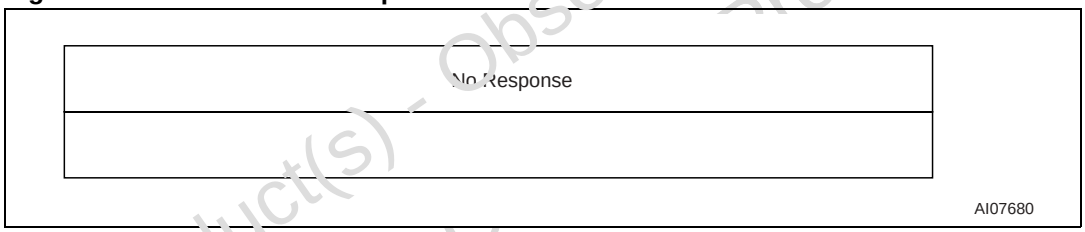
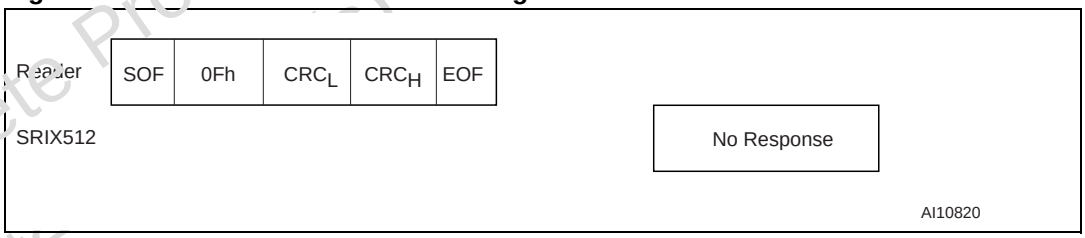


Figure 37. COMPLETION frame exchange between Reader and SRIX512



9.6 RESET_TO_INVENTORY() command

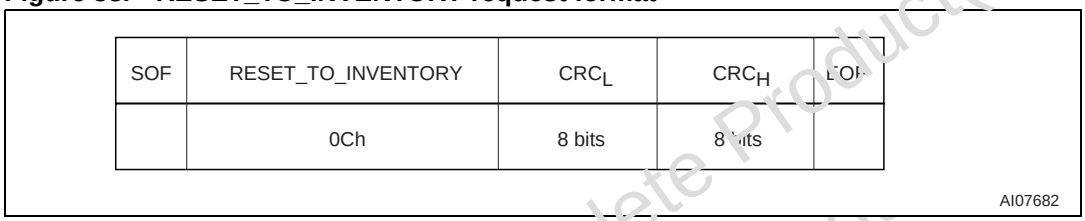
Command Code = 0Ch

On receiving the RESET_TO_INVENTORY() command, all SRIX512 devices in SELECTED state revert to INVENTORY state. The concerned SRIX512 devices are thus resubmitted to the anticollision sequence. This command is useful when two SRIX512 devices with the same 8-bit Chip_ID happen to be in SELECTED state at the same time. Forcing them to go through the anticollision sequence again allows the reader to generates new PCALL16() commands and so, to set new random Chip_IDs.

The RESET_TO_INVENTORY() command does not generate a response.

All SRIX512 devices that are not in SELECTED state ignore the RESET_TO_INVENTORY() command.

Figure 38. RESET_TO_INVENTORY request format



Request parameter:

- No parameter

Figure 39. RESET_TO_INVENTORY response format

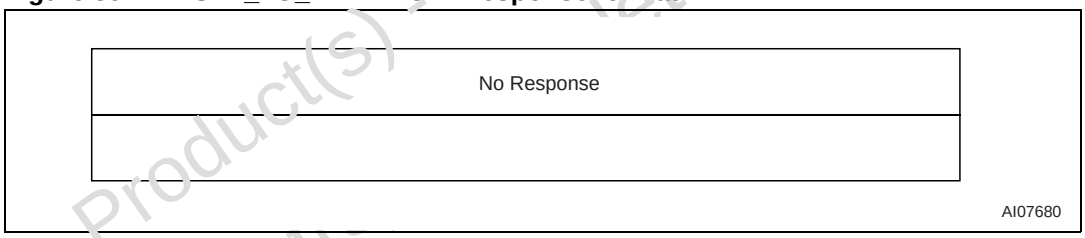
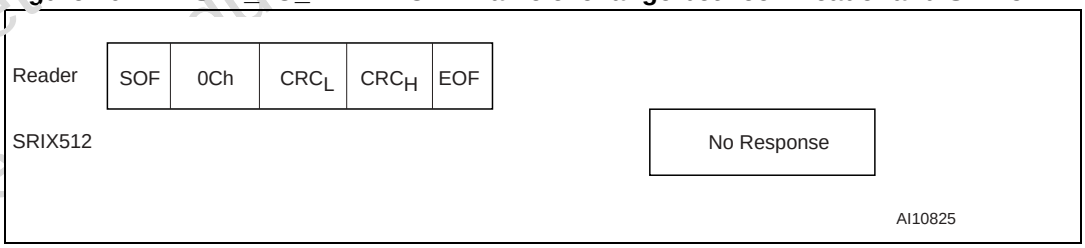


Figure 40. RESET_TO_INVENTORY frame exchange between Reader and SRIX512



9.7 READ_BLOCK(Addr) command

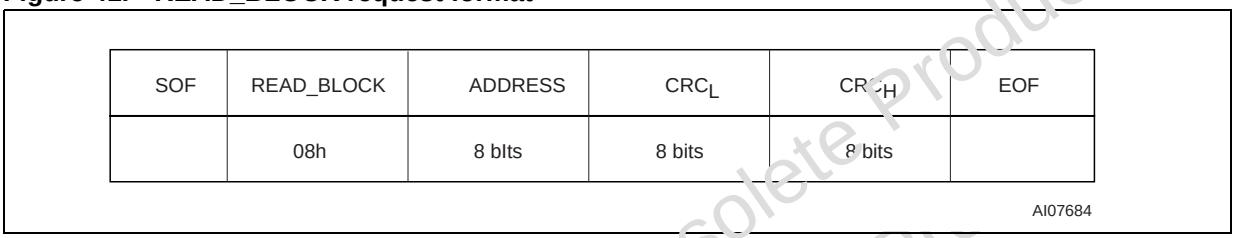
Command Code = 08h

On receiving the READ_BLOCK command, the SRIX512 reads the desired block and returns the 4 data Bytes contained in the block. Data Bytes are transmitted with the Least Significant Byte first and each byte is transmitted with the least significant bit first.

The address byte gives access to the 16 blocks of the SRIX512 (addresses 0 to 15). READ_BLOCK commands issued with a block address above 15 will not be interpreted and the SRIX512 will not return any response, except for the System area located at address 255.

The SRIX512 must have received a SELECT() command and be switched to SELECTED state before any READ_BLOCK() command can be accepted. All READ_BLOCK() commands sent to the SRIX512 before a SELECT() command is issued are ignored.

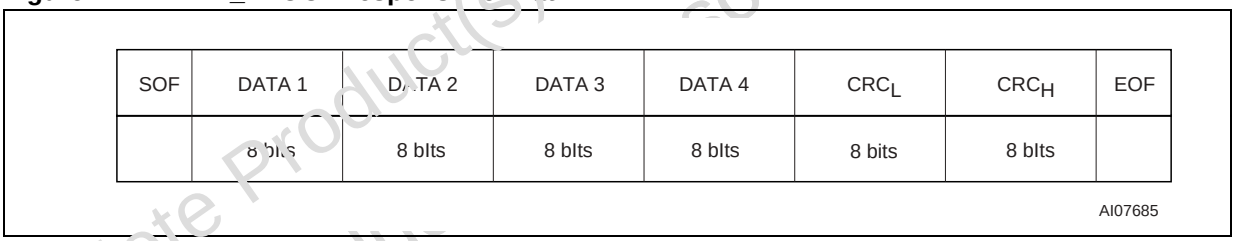
Figure 41. READ_BLOCK request format



Request parameter:

- ADDRESS: block addresses from 0 to 15, or 255

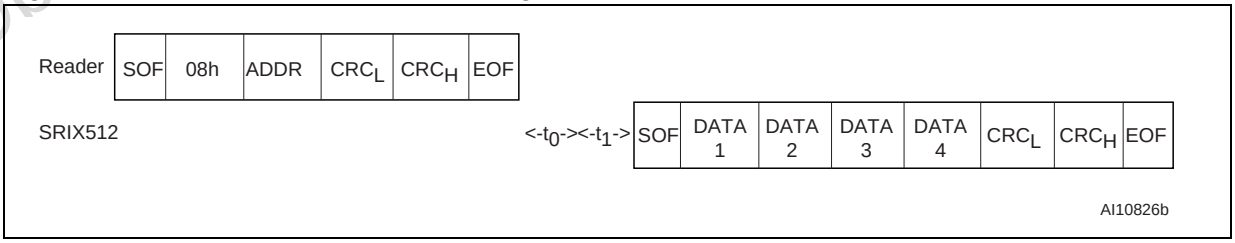
Figure 42. READ_BLOCK response format



Response parameters:

- DATA 1: Less significant data Byte
- DATA 2: Data Byte
- DATA 3: Data Byte
- DATA 4: Most significant data Byte

Figure 43. READ_BLOCK frame exchange between Reader and SRIX512



9.8 WRITE_BLOCK (Addr, Data) command

Command Code = 09h

On receiving the WRITE_BLOCK command, the SRIX512 writes the 4 bytes contained in the command to the addressed block, provided that the block is available and not Write-protected. Data Bytes are transmitted with the Least Significant Byte first, and each byte is transmitted with the least significant bit first.

The address Byte gives access to the 16 blocks of the SRIX512 (addresses 0 to 15). WRITE_BLOCK commands issued with a block address above 15 will not be interpreted and the SRIX512 will not return any response, except for the System area located at address 255.

The result of the WRITE_BLOCK command is submitted to the addressed block. See the following paragraphs for a complete description of the WRITE_BLOCK command:

- *Resettable OTP area (addresses 0 to 4)*.
- *Binary counter (addresses 5 to 6)*.
- *EEPROM (addresses 7 to 15)*.

The WRITE_BLOCK command does not give rise to a response from the SRIX512. The reader must check after the programming time, t_W, that the data was correctly programmed. The SRIX512 must have received a SELECT() command and be switched to SELECTED state before any WRITE_BLOCK command can be accepted. All WRITE_BLOCK commands sent to the SRIX512 before a SELECT() command is issued, are ignored.

Figure 44. WRITE_BLOCK request format

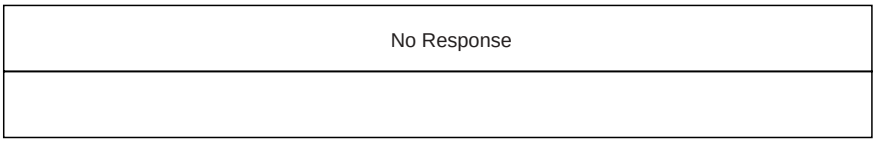
SOF	WRITE_BLOCK	ADDRESS	DATA 1	DATA 2	DATA 3	DATA 4	CRC_L	CRC_H	EOF
	09h	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	

AI07687

Request parameters:

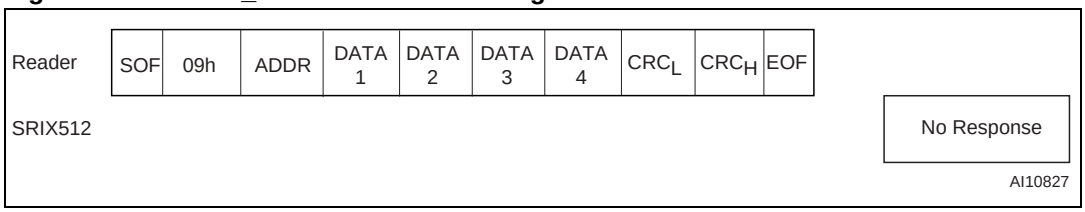
- ADDRESS: block addresses from 0 to 15, or 255
- DATA 1: Less significant data Byte
- DATA 2: Data Byte
- DATA 3: Data Byte
- DATA 4: Most significant data Byte.

Figure 45. WRITE_BLOCK response format



AI07680

Figure 46. WRITE_BLOCK frame exchange between Reader and SRIX512



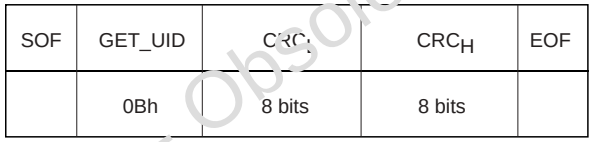
9.9 GET_UID() command

Command Code = 0Bh

On receiving the GET_UID command, the SRIX512 returns its 8 UID Bytes. UID Bytes are transmitted with the Least Significant Byte first, and each byte is transmitted with the least significant bit first.

The SRIX512 must have received a SELECT() command and be switched to SELECTED state before any GET_UID() command can be accepted. All GET_UID() commands sent to the SRIX512 before a SELECT() command is issued, are ignored.

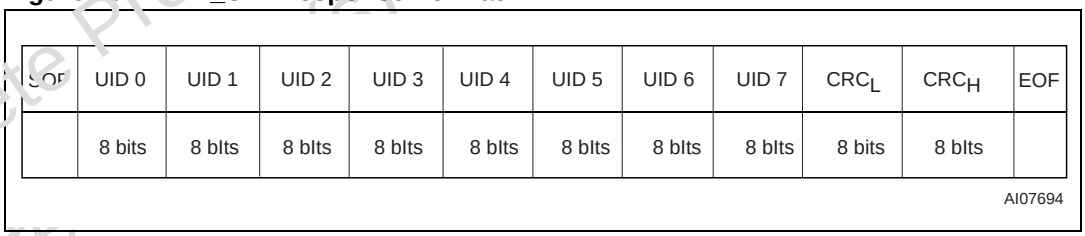
Figure 47. GET_UID request format



Request parameter:

- No parameter

Figure 48. GET_UID Response Format



Response parameters:

- UID 0: Less significant UID Byte
- UID 1 to UID 6: UID Bytes
- UID 7: Most significant UID Byte.

Unique Identifier (UID)

Members of the SRIX512 family are uniquely identified by a 64-bit Unique Identifier (UID). This is used for addressing each SRIX512 device uniquely after the anti-collision loop. The UID complies with ISO/IEC 15963 and ISO/IEC 7816-6. It is a read-only code, and comprises (as summarized in *Figure 49*):

- an 8-bit prefix, with the most significant bits set to D0h
- an 8-bit IC Manufacturer code (ISO/IEC 7816-6/AM1) set to 02h (for STMicroelectronics)
- a 6-bit IC code set to 00 0100b = 4d for SRIX512
- a 42-bit Unique Serial Number

Figure 49. 64-bit unique identifier of the SRIX512

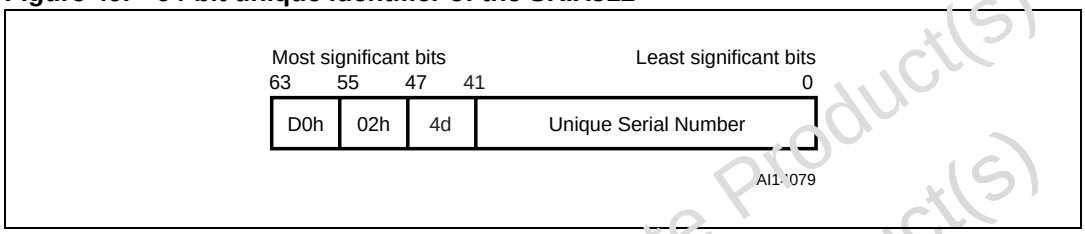
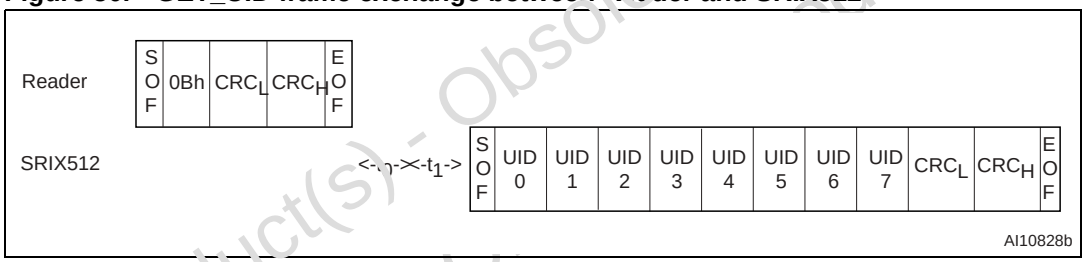


Figure 50. GET_UID frame exchange between Reader and SRIX512



9.10 Power-on state

After Power-on, the SRIX512 is in the following state:

- It is in the low-power state.
- It is in READY state.
- It shows highest impedance with respect to the reader antenna field.
- It will not respond to any command except INITIATE().

10 Maximum rating

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute maximum ratings

Symbol	Parameter		Min.	Max.	Unit
T_{STG}, h_{STG}, t_{STG}	Storage conditions	Wafer	15	25	°C
				23	months
			kept in its antistatic bag		
		A3, A4, A5	15	25	°C
			40%	60%	RH
				2	years
I_{CC}	Supply current on AC0 / AC1		–20	20	mA
V_{MAX}	Input voltage on AC0 / AC1		–7	7	V
V_{ESD}	Electrostatic Discharge Voltage	Machine model(1)	–100	100	V
		Human Body model(1)	–1000	1000	V
		Human Body model (2)	–4000	4000	V

1. Mil. Std. 883, Method 3015.
2. ESD test: ISO10373-6 for proximity cards.

11 DC and ac parameters

Table 7. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	–20	85	°C

Table 8. DC characteristics

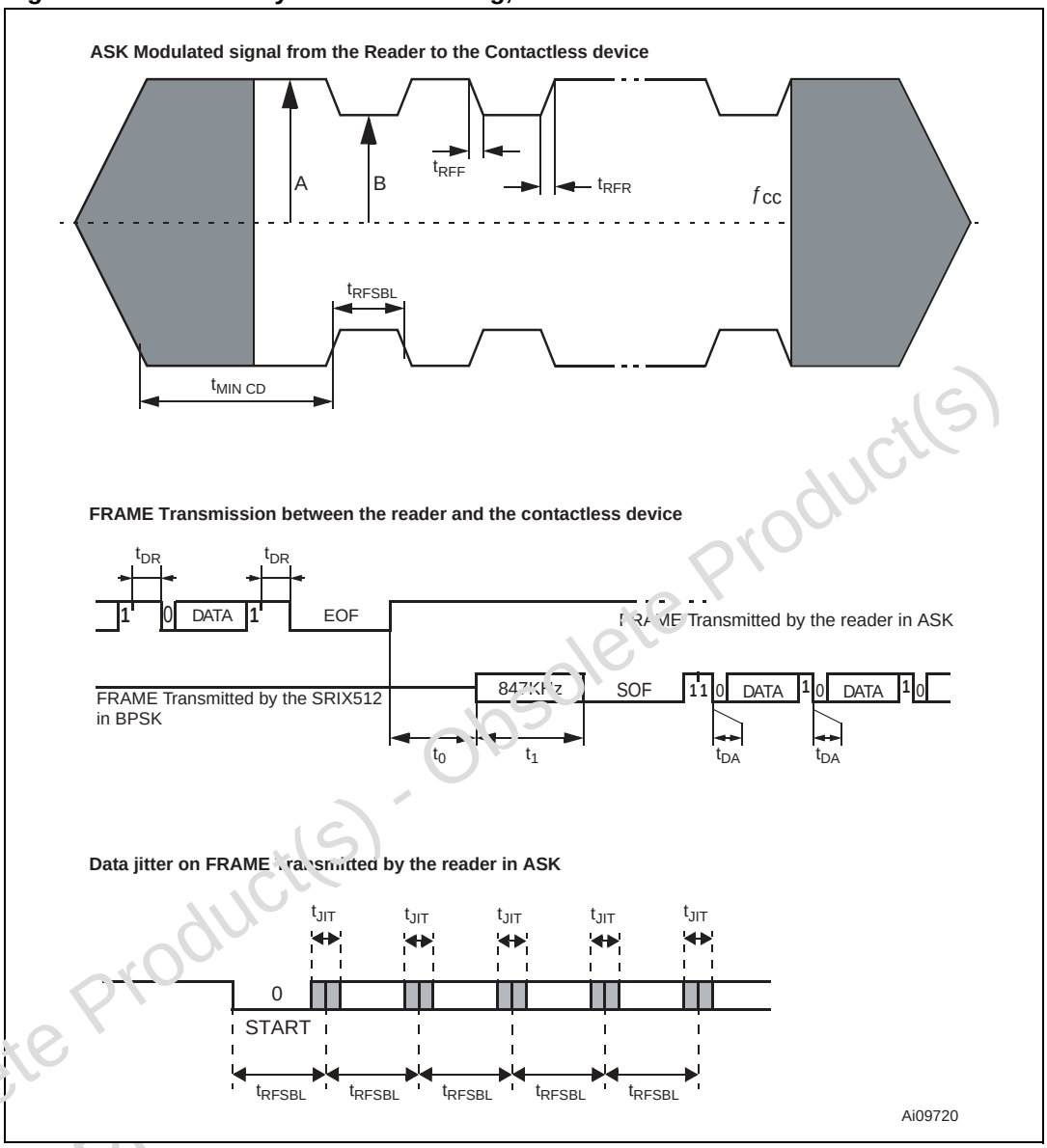
Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{CC}	Regulated voltage		2.5		3.5	V
I_{CC}	Supply current (active in Read)	V_{CC} = 3.0 V			100	µA
I_{CC}	Supply current (active in Write)	V_{CC} = 3.0 V			250	µA
V_{RET}	Back-scattering-induced voltage	ISO 10373-6	20			mV
C_{TUN}	Internal tuning capacitor	13.56 MHz		64		pF

Table 9. AC characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{CC}	External RF signal frequency		13.553	13.567	MHz
$MI_{CARRIER}$	Carrier modulation index	MI=(A-B)/(A+B)	8	14	%
t_{RFR}, t_{RFF}	10% Rise and Fall times		0.8	2.5	µs
t_{RFSBL}	Minimum pulse width for start bit	ETU = 128/f_{CC}	9.44		µs
t_{JIT}	ASK modulation data jitter	Coupler to SRIX512	–2	+2	µs
$t_{MIN\ CD}$	Minimum time from carrier generation to first data		5		ms
f_S	Sub carrier frequency	f_{CC}/16	847.5		kHz
t_0	Antenna reversal delay	128/f_S	151		µs
t_1	Synchronization delay	128/f_S	151		µs
t_2	Answer to new request delay	14 ETU	132		µs
t_{DR}	Time between request characters	Coupler to SRIX512	0	57	µs
t_{DA}	Time between answer characters	SRIX512 to Coupler	0		µs
t_W	Programming time for WRITE	With no Auto-Erase cycle (OTP)		3	ms
		With Auto-Erase cycle (EEPROM)		5	ms
		Binary counter decrement		7	ms

1. All timing measurements were performed on a reference antenna with the following characteristics:
External size: 75 mm x 48 mm
Number of turns: 3
Width of conductor: 1 mm
Space between 2 conductors: 0.4 mm
Value of the coil: 1.4 µH
Tuning Frequency: 14.4 MHz.

Figure 51. SRIX512 synchronous timing, transmit and receive

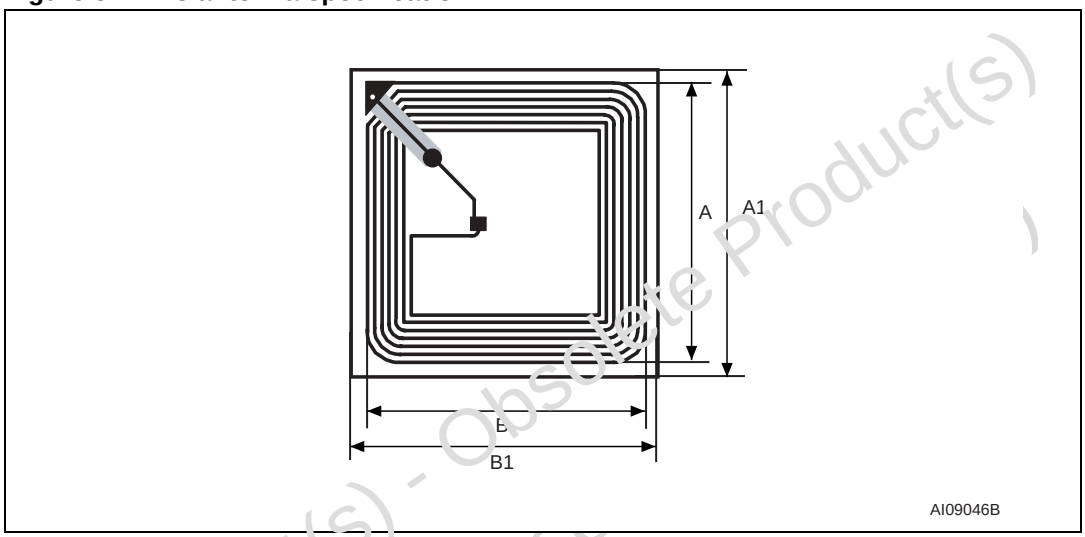


12 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 52. A3 antenna specification

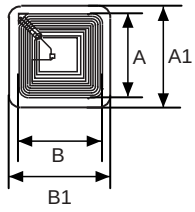


1. Drawing is not to scale.

Table 10. A3 antenna specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	38	37.5	38.5	mm
B	Coil length	38	37.5	38.5	mm
A1	Inlay width	43	42.5	43.5	mm
B1	Inlay length	43	42.5	43.5	mm
	Overall thickness of copper antenna coil	110	90	130	µm
	Silicon thickness	180	165	195	µm
Q	Unloaded Q value	40			
F_{NOM}	Unloaded free-air resonance	15.1			MHz
P_A	H-field energy for device operation		0.5 114		A/m dbµA/m

Figure 53. A4 antenna specification

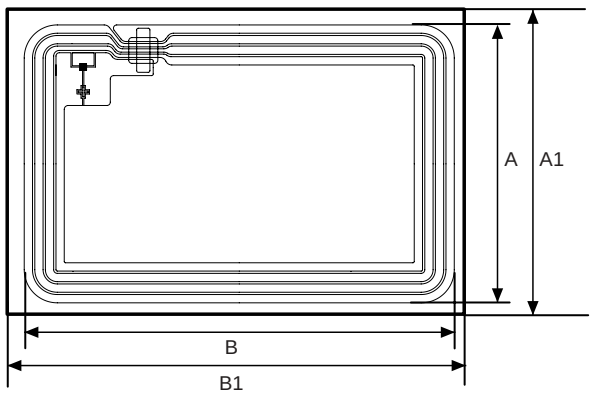


1. Drawing is not to scale.

Table 11. A4 antenna specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	15	14.5	15.5	mm
B	Coil length	15	14.5	15.5	mm
A1	Inlay width	19	18.5	19.5	mm
B1	Inlay length	19	18.5	19.5	mm
	Overall thickness of copper antenna coil	110	90	130	µm
	Silicon thickness	180	165	195	µm
Q	Unloaded Q value	30			
F_{NOM}	Unloaded free-air resonance	14.5			MHz
P_A	H-field energy for device operation		1.5 123.5		A/m dbµA/m

Figure 54. A5 antenna specification



1. Drawing is not to scale.

Table 12. A5 antenna specification

Symbol	Parameter	Type	Min	Max	Unit
A	Coil width	42	41.5	42.5	mm
B	Coil length	65	64.5	65.5	mm
A1	Inlay width	46	45.5	46.5	mm
B1	Inlay length	70	69.5	70.5	mm
	Overall thickness of copper antenna coil	140	130	150	µm
	Silicon thickness	180	165	195	µm
Q	Unloaded Q value	30			
F_{NOM}	Unloaded free-air resonance	14.8			MHz
P_A	H-field energy for device operation		0.25 108		A/m dbµA/m

13 Part numbering

Table 13. Ordering information scheme

Example: SRIX512 – W4 /XXX

Device type

SRIX512

Package

W4 =180 µm ± 15 µm Unsawn Wafer

SBN18 = 180 µm ± 15 µm Bumped and Sawn Wafer on 8-inch Frame

A3T = 38 mm x 38 mm Copper Antenna on Continuous Tape

A3S = 38 mm x 38 mm Copper Singulated Adhesive Antenna on Tape

A4T = 15 mm x 15 mm Copper Antenna on Continuous Tape

A4S = 15 mm x 15 mm Copper Singulated Adhesive Antenna on Tape

A5T = 42 mm x 65 mm Copper Antenna on Continuous Tape

A5S = 42 mm x 65 mm Copper Singulated Adhesive Antenna on Tape

Customer code

XXX = Given by STMicroelectronics

Note: Devices are shipped from the factory with the memory content bits erased to 1.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Appendix A ISO 14443 Type B CRC calculation

```
#include <stdio.h>
#include <stdlib.h>
#include <string.h>
#include <ctype.h>
#define BYTE unsigned char
#define USHORT unsigned short

unsigned short UpdateCrc(BYTE ch, USHORT *lpwCrc)
{
   ch = (ch^(BYTE)((*lpwCrc) & 0x00FF));
   ch = (ch^(ch<<4));
   *lpwCrc = (*lpwCrc >> 8)^((USHORT)ch << 8)^((USHORT)ch<<3)^((USHORT)ch>>4);
   return(*lpwCrc);
}

void ComputeCrc(char *Data, int Length, BYTE *TransmitFirst, BYTE *TransmitSecond)
{
BYTE chBlock; USHORTt wCrc;
   wCrc = 0xFFFF; // ISO 3309
   do
      {
      chBlock = *Data++;
      UpdateCrc(chBlock, &wCrc);
      } while (--Length);
   wCrc = ~wCrc; // ISO 3309
   *TransmitFirst = (BYTE) (wCrc & 0xFF);
   *TransmitSecond = (BYTE) ((wCrc >> 8) & 0xFF);
   return;
}

int main(void)
{
BYTE BuffCRC_B[10] = {0x0A, 0x12, 0x34, 0x56}, First, Second, i;
   printf("Crc 16 G(x) = x^16 + x^12 + x^5 + 1");
   printf("CRC_B of [ ");
   for(i=0; i<4; i++)
      printf("%02X ",BuffCRC_B[i]);
   ComputeCrc(BuffCRC_B, 4, &First, &Second);
   printf("] Transmitted: %02X then %02X.", First, Second);
   return(0);
```

Appendix B SRIX512 command brief

Figure 55. INITIATE frame exchange between Reader and SRIX512

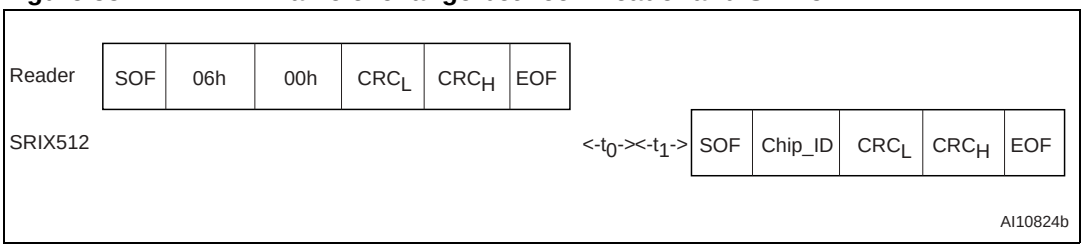


Figure 56. PCALL16 frame exchange between Reader and SRIX512

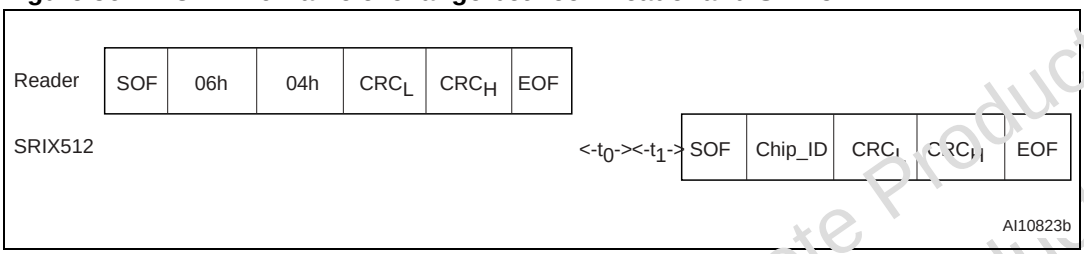


Figure 57. SLOT_MARKER frame exchange between Reader and SRIX512

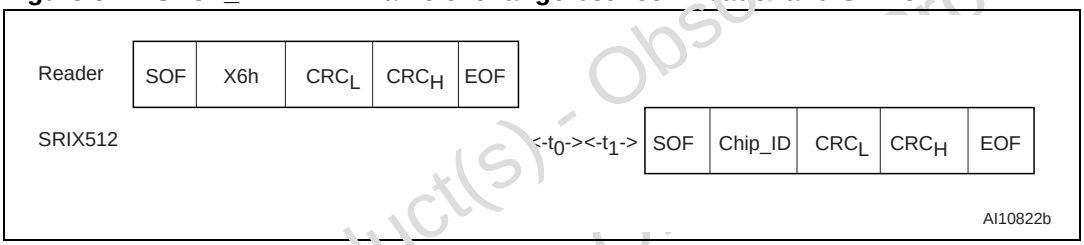


Figure 58. SELECT frame exchange between Reader and SRIX512

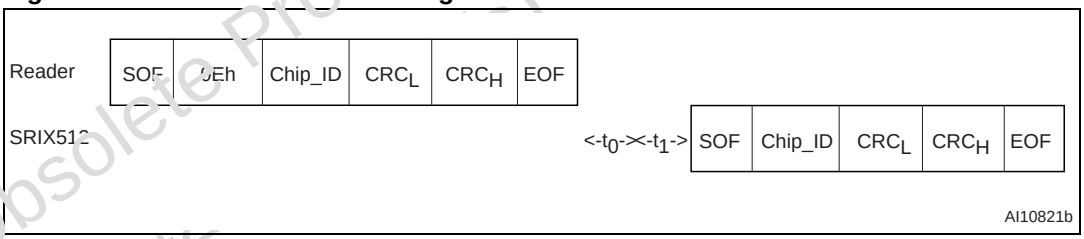


Figure 59. COMPLETION frame exchange between Reader and SRIX512

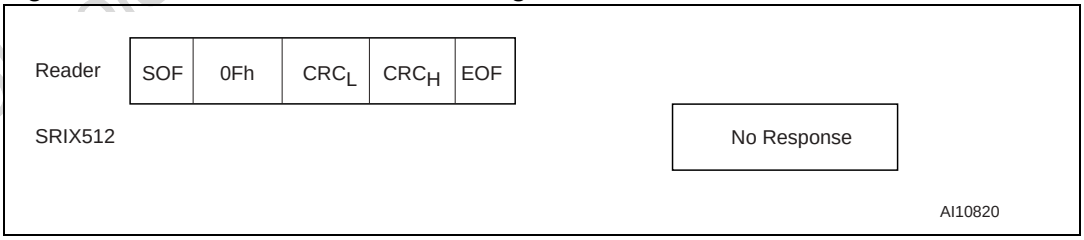


Figure 60. RESET_TO_INVENTORY frame exchange between Reader and SRIX512

Figure 61. READ_BLOCK frame exchange between Reader and SRIX512

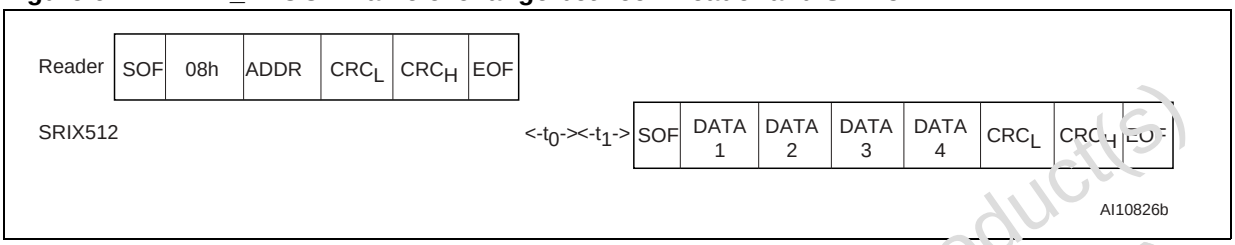


Figure 62. WRITE_BLOCK frame exchange Between Reader and SRIX512

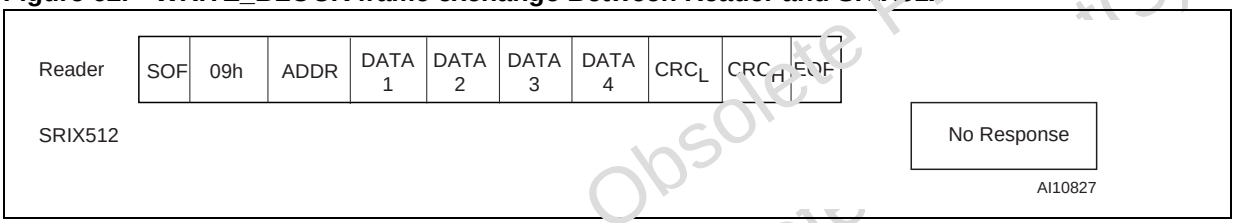
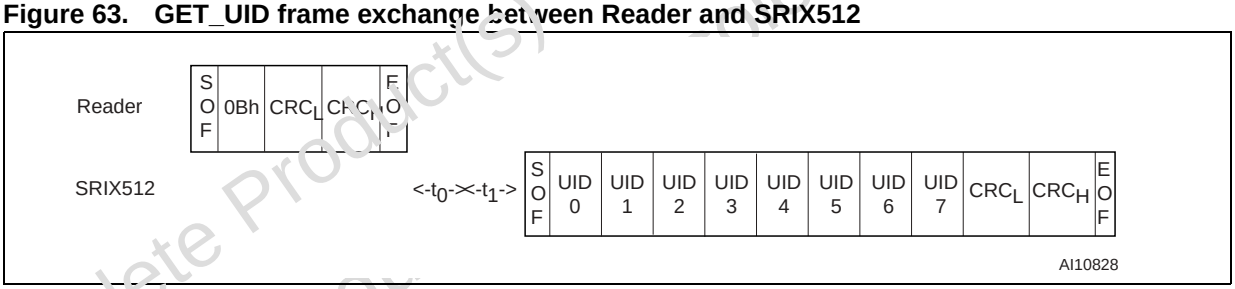


Figure 63. GET_UID frame exchange between Reader and SRIX512



14 Revision history

Table 14. Document revision history

Date	Version	Changes
11-Jul-2003	1.0	First Issue
26-Apr-2004	2.0	First public release of full datasheet
29-Nov-2004	3.0	*Package mechanical* section revised.
13-Dec-2004	4.0	V_{RET} and C_{TUN} parameters added to *Table 8: DC characteristics*.
17-Aug-2005	5.0	Updated initial counter values in *32-bit binary counters on page 16*.
05-Apr-2007	6	Document reformatted. Small text changes. Document status changed from Datasheet to Not For New Design. *Unique Identifier (UID) on page 37* added. C_{TUN} min and max values removed, typ value added in *Table 8: DC characteristics*. Space removed between t_0 and t_1 in all “frame exchange between Reader and SRIX512” figures (see *Appendix B: SRIX512 command brief*). All antennas are ECOPACK® compliant.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com