ST SATA310

Ideal for serial ATA and easily adapted to support SAS interfaces

Offering high-performance, low-power, low-cost, and a modular design, the SATA310 is available as a fully characterized macro-cell for highly integrated SOC solutions, using **STMicroelectronics'** advanced HCMOS9 0.13µ process technology.

Key features

- Compliant with the industry-standard serial ATA specification, both Gen 1 and Gen 2, SATAII speed requirements
- Easily adaptable to meet serial attached SCSI (SAS) specifications
- Support for 1.5 and 3.0Gbaud data rates
- Support for spread spectrum clocking
- Integrated oscillator provides 75MHz and 150MHz system clocks
- 20-bit wide parallel word transmit/receive
- Integrated 8b/10b encode/decode
- Integrated out-of-band signaling
- Integrated elastic buffer for timebase correction
- Integrated I/O impedance adaptation
- JTAG test access port
- Integrated dynamic BIST
- Boundary SCAN
- HCMOS 0.13µ CMOS technology, 1.2V and 2.5V power supply
- Low-power (150mW)
- Shared block for multiple line integration with minimum power and area data frequency

Applications

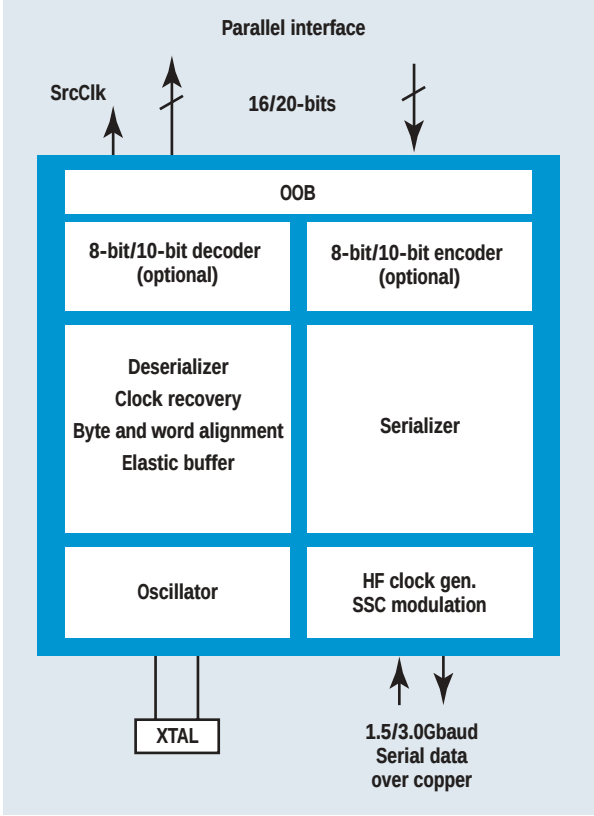
- Serial ATA host controllers
- Serial ATA device controllers
- Serial attached SCSI

The serial ATA standard provides improved bandwidth performance over the widely used parallel ATA standard, while maintaining the same system visibility. It is designed solely for communication between a host computer and a storage device, and operates at 1.5Gb/s for generation 1 and 3.0Gb/s rate for generation 2. The serial attached SCSI standard, SAS, is a new serial point-to-point enterprise device attached interface, leveraging the serial ATA physical layer and the SCSI protocol set to support a wide range of price/performance storage products. SAS extends the legacy of parallel SCSI and operates at 1.5 and 3.0Gb/s.

The SATA310 complies with the industry standard serial ATA specification (revision 1.0) supports SATAII speed requirements and can be easily adapted to support the SAS standard. In a serial ATA application, it is designed for either host or device operations and can drive electrical cables directly, without external components. The architecture is optimized to deliver the highest jitter performance together with small transceiver size, low power and easy migration into future of process geometries. Also, the SATA310 has a modular design, sharing blocks to reduce power consumption and area, on occasions when multiple PHY are to be integrated into a single ASIC. To reduce electromagnetic interference (EMI), the SATA310 supports SSC modulation, though the SSC transmit function can be disabled if required. SATA310 also integrates 8b/10b encode/decode functions offering a higher level of integration.

The SATA310 performs the high-speed serialization and deserialization function and provides a 20-bit wide parallel interface to the link. The parallel interface runs at 75MHz for 1.5Gbaud and 150MHz for 3.0Gbaud. The timing source (clock) can be provided internally or externally, and as it is designed with a true DFT approach, all the internal logic is accessible through a scan path. A self-test capability (BIST) is included.

This latest addition to the ST product family for storage and computer applications completes the ST product and IP portfolio for serial interfaces. The SATA310 enables interoperability, rapid technology integration and fast time to market. During the SATA Plug Fest held in Longmont, CO, in March 2004, the SATA310 has shown full interoperability with existing solutions available on the market.



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