

SPEAr™ Net ethernet controller

SoC-based solution with USB host



STMicroelectronics' SPEAr NET is a SoC based on the ARM720T RISC core, cache and MMU. It is ideal for entry-level consumer applications, industrial control and networking products, medical equipment and any other application that requires a proven ARM-based architecture with basic connectivity features and a full operating temperature range. SPEAr NET is available with a full-features starter kit that enables easy development, including SW libraries, reference design PCB board and detailed documentation.

Key features

- Based on ARM720T (8k unified Cache and MMU included)
- 10/100 Mbps Ethernet connection (IEEE802.3)
- USB 2.0 host controller, supports 12 Mbit/s full-speed devices
- UART interface: 115KBauds
- I²C interface: fast and slow
- IEEE1284 host controller
- Real-time clock
- Timers and watchdog peripherals
- Integrated PLL (25MHz input, 48MHz output)
- Up to 12 GPIOs (including IEEE1284 port)
- 8K SRAM shared with an external microprocessor
- Static memory controller (up to two banks, max 16M each)

- DRAM controller SDRAM/EDO (up to four banks, max 32M each)
- External I/O banks: 2 x 16 KB
- Operating temperature range -40 to 105°C
- Package LFBGA 180 (12 x 12 x 1.7mm). Lead-free

Applications

- Industrial communication controller
- Security remote controller
- Printer server
- Decentralized building device controller
- Companion communication controller for motor drive application
- Power meters

SPEAr is a new family of SoCs from ST, offering a powerful digital engine which allows the introduction of special user functions, in limited time and at limited cost. The family is based on an ARM® architecture that maximizes HW and SW performance and includes an advanced bus system, several IPs for connectivity and memory interfaces. The embedding of user functions is realized via a customizable logic block, which allows high-performance, quick development and a full custom design approach. As an innovative concept in the market, SPEAr is a system rich in most sophisticated and modern IPs, and ideal for developing optimized solutions for specific requirements. Allowing very short lead-time (a few weeks) and a low NRE, it offers an unprecedented cost saving.

SPEAr NET is a general purpose member of the family and it is a complete System-on-Chip based on the ARM720T with MMU (supporting a wide list of embedded OSs, including LINUX). SPEAr NET provides a SMART bridge between different interfaces:

- IEEE802.3/Ethernet MAC core for network interface. A MII (medium independent interface) connection with external PHY chip (i.e. STE100P) gives a 10/100Mbps capability.
- USB host controller compliant with the USB 2.0 full speed specification (12Mbs, OpenHCI)
- IEEE1284 host controller offering compatibility mode, Nibble mode and ECP mode. All lines can be also used as GPIOs
- Shared RAM (mail box method) for communication with other processors

- I²C master controller
- UART port provides a standard serial data communication with transmit and receive channels that can operate concurrently to handle a full-duplex operation (up to 115Kbaude)

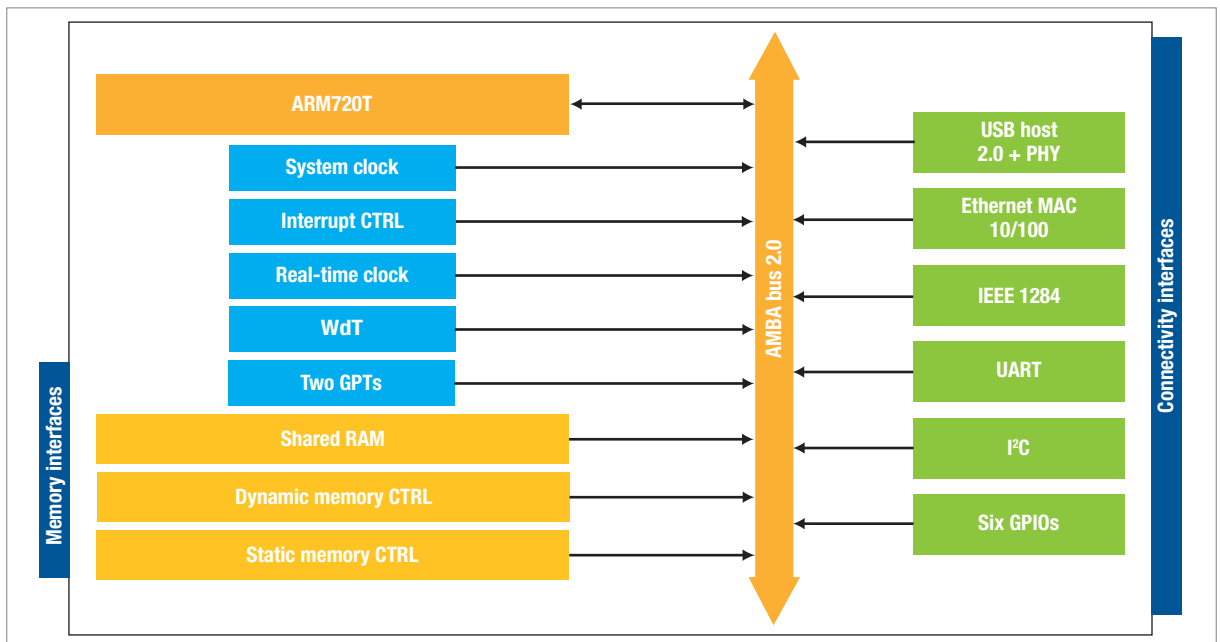
The ARM720T is a general purpose 32-bit RISC microprocessor with 8 KB cache, enlarged write buffer and Memory Management Unit (MMU) combined in a single-chip.

The shared RAM interface is based on two blocks:

- 8 Kbyte static RAM
- Controller to manage access to the RAM, while access to the RAM is driven by a round-robin arbiter, which receives requests from two agents:
 - AHB master, i.e. internal CPU or DMA (by AHB bus)
 - External processor (by asynchronous external bus).

The DRAM controller block is an AHB slave used to provide an interface between the system bus and external memory device. The controller supports four external banks, containing either SDRAM or EDO memories. Memory components with 32-, 16- and 8-bit data buses are supported.

SRAM is used to manage the data flow from the internal AMBA (advanced micro-controller bus architecture) AHB (advanced high-performance bus) and any static memory components (ROM, SRAM and Flash) with all timings fully-programmable.



SPEAr NET is a general purpose device based on the ARM720.



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