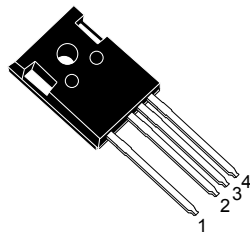
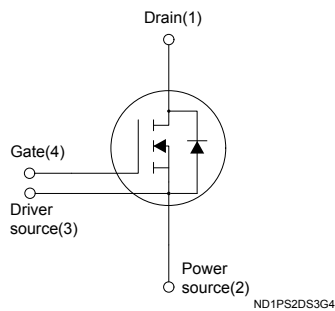


N-channel 650 V, 24 mΩ typ., 84 A MDmesh M5 Power MOSFET in a TO247-4 package


TO247-4

Product status link
[STW88N65M5-4](#)
Product summary

Order code	STW88N65M5-4
Marking	88N65M5
Package	TO247-4
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STW88N65M5-4	650 V	29 mΩ	84 A

- Higher V_{DSS} rating
- Higher dv/dt capability
- Excellent switching performance thanks to the extra driving source pin
- Extremely low $R_{DS(on)}$
- 100% avalanche tested

Applications

- High efficiency switching applications:
 - Servers
 - PV inverters
 - Telecom infrastructure
 - Multi kW battery chargers

Description

This device is an N-channel Power MOSFET based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting product offers extremely low on-resistance, making it particularly suitable for applications requiring high power and superior efficiency.

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	84	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	50.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	336	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	450	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Maximum operating junction temperature	150	

1. Pulse width is limited by safe operating area.

2. $I_{SD} \leq 84\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.28	$^{\circ}\text{C}/\text{W}$
R_{thJA}	Thermal resistance, junction-to-ambient	50	

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max.)	15	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	2	J

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 42\text{ A}$		24	29	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	8825	-	pF
C_{oss}	Output capacitance		-	223	-	pF
C_{rss}	Reverse transfer capacitance		-	11	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	778	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	202	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.79	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 42\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Gate charge test circuit)	-	204	-	nC
Q_{gs}	Gate-source charge		-	51	-	nC
Q_{gd}	Gate-drain charge		-	84	-	nC

- $C_{o(tr)}$ is an equivalent capacitance that provides the same charging time as C_{oss} while V_{DS} is rising from 0 V to the stated value.
- $C_{o(er)}$ is an equivalent capacitance that provides the same stored energy as C_{oss} while V_{DS} is rising from 0 V to the stated value.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 56\text{ A}$, $R_G = 7.2\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	150	-	ns
$t_{r(v)}$	Voltage rise time		-	19	-	ns
$t_{f(i)}$	Current fall time	(see Figure 16. Test circuit for inductive load switching and diode recovery times and Figure 19. Switching time waveform)	-	24	-	ns
$t_{c(off)}$	Crossing time		-	45	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		84	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		336	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 84\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 84\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$	-	544		ns
Q_{rr}	Reverse recovery charge		-	14		μC
I_{RRM}	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	50		A
t_{rr}	Reverse recovery time	$I_{SD} = 84\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$	-	660		ns
Q_{rr}	Reverse recovery charge		-	20		μC
I_{RRM}	Reverse recovery current		-	60		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

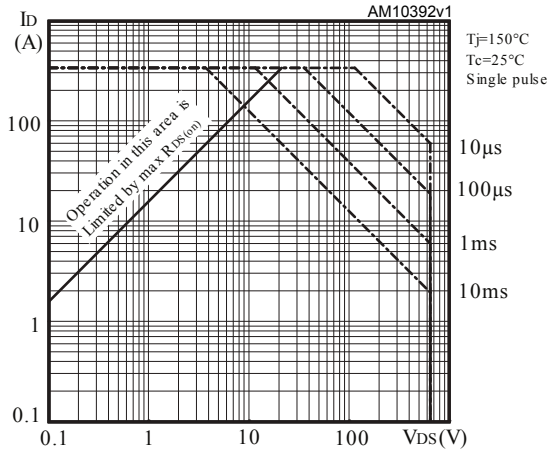
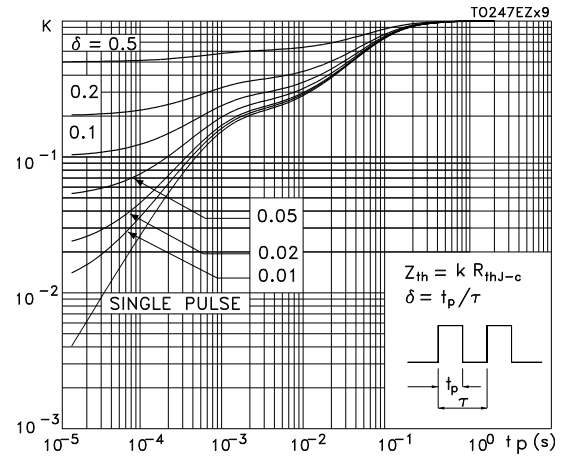
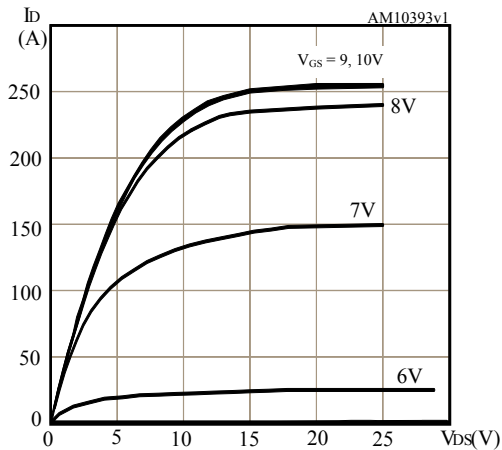
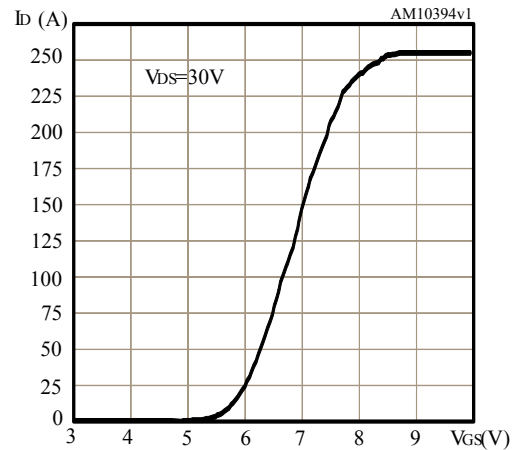
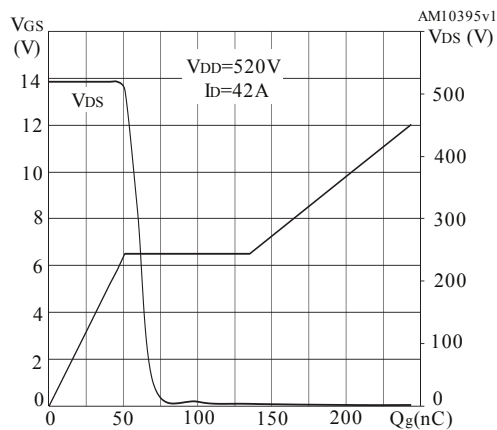
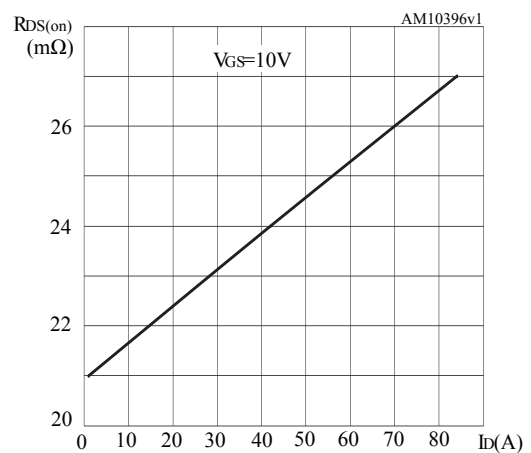
Figure 1. Safe operating area

Figure 2. Normalized transient thermal impedance

Figure 3. Typical output characteristics

Figure 4. Typical transfer characteristics

Figure 5. Typical gate charge characteristics

Figure 6. Typical drain-source on-resistance


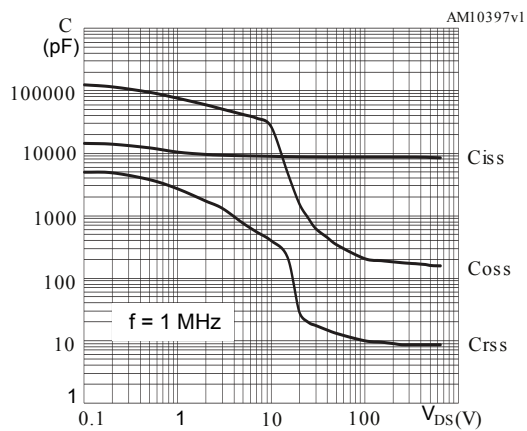
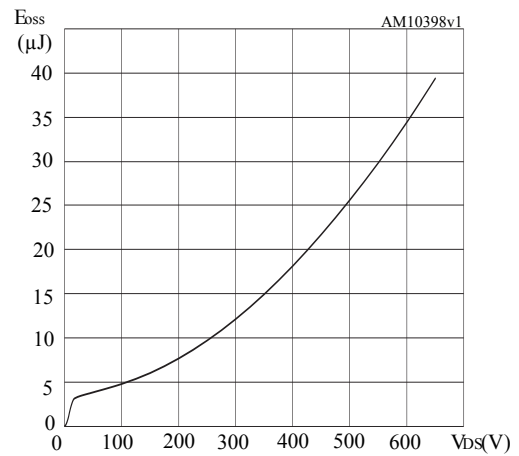
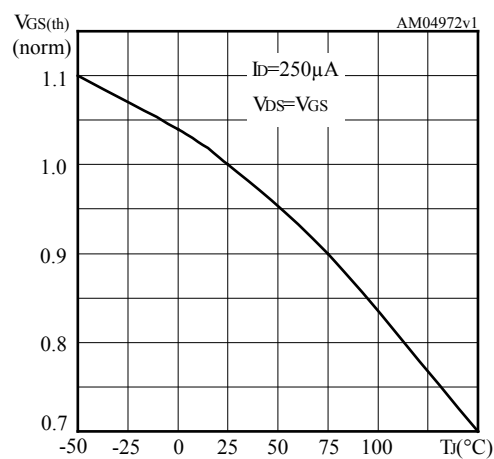
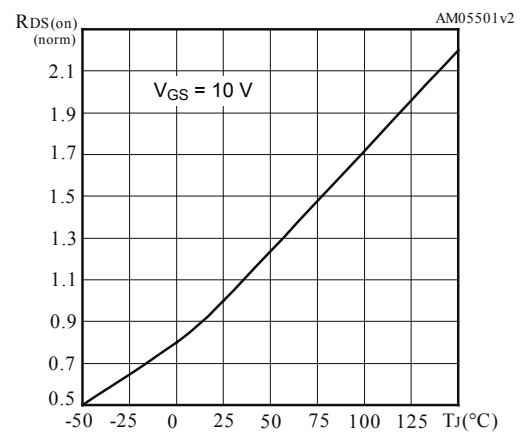
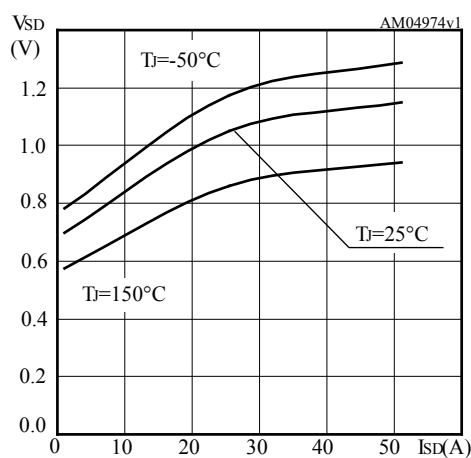
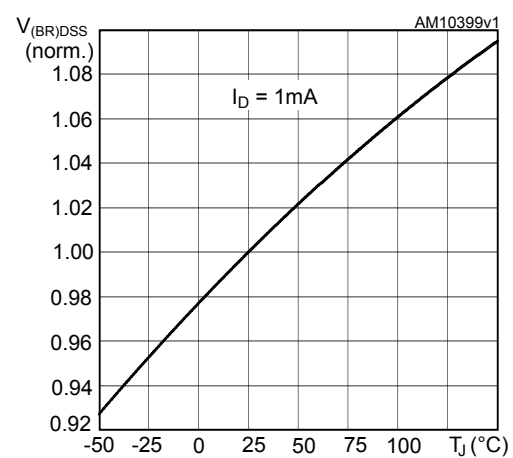
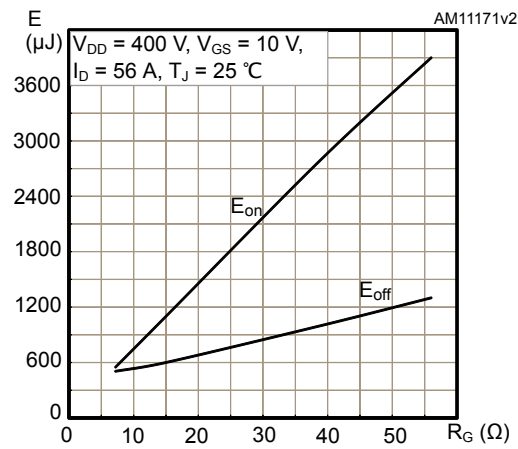
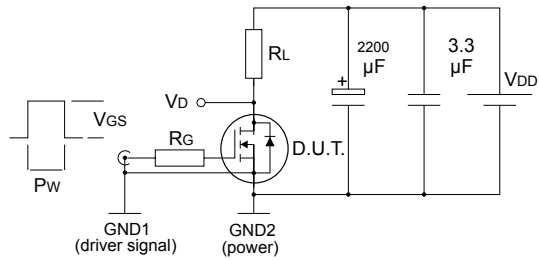
Figure 7. Typical capacitance characteristics

Figure 8. Typical output capacitance stored energy

Figure 9. Normalized gate threshold vs temperature

Figure 10. Normalized on-resistance vs temperature

Figure 11. Typical reverse diode forward characteristics

Figure 12. Normalized breakdown voltage vs temperature


Figure 13. Typical switching energy vs gate resistance

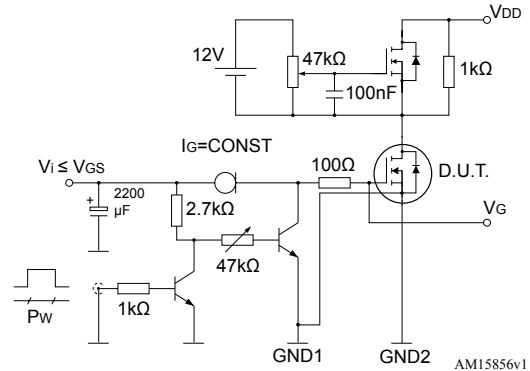


Note: E_{on} including reverse recovery of a SiC diode.

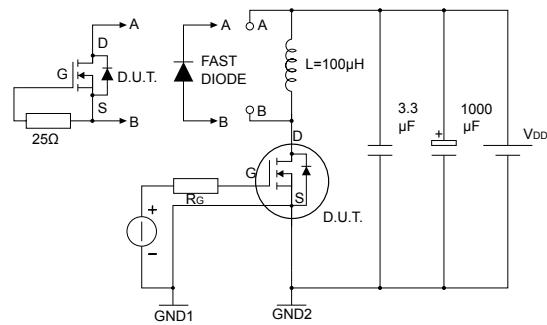
3 Test circuits

Figure 14. Switching times test circuit for resistive load


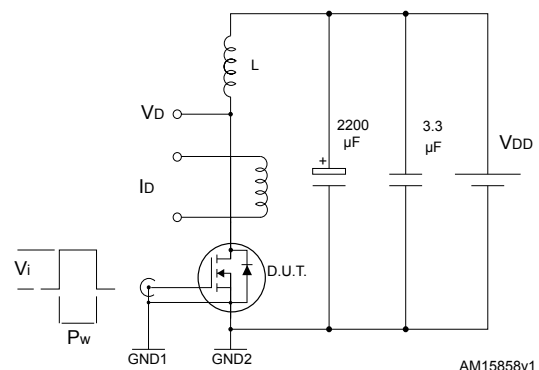
AM15855v1

Figure 15. Gate charge test circuit


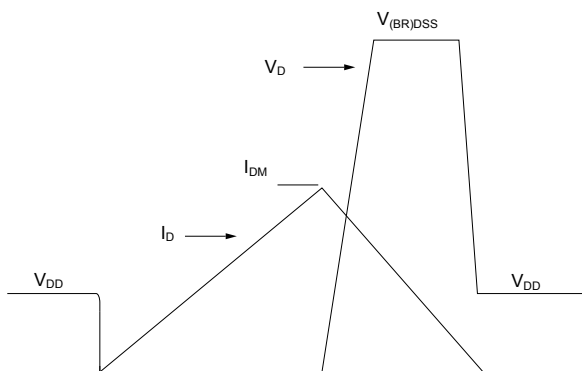
AM15856v1

Figure 16. Test circuit for inductive load switching and diode recovery times


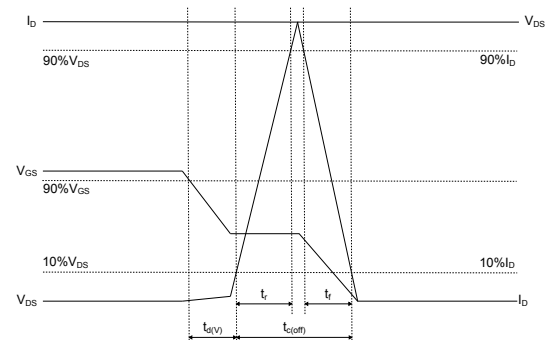
AM15857v1

Figure 17. Unclamped inductive load test circuit


AM15858v1

Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


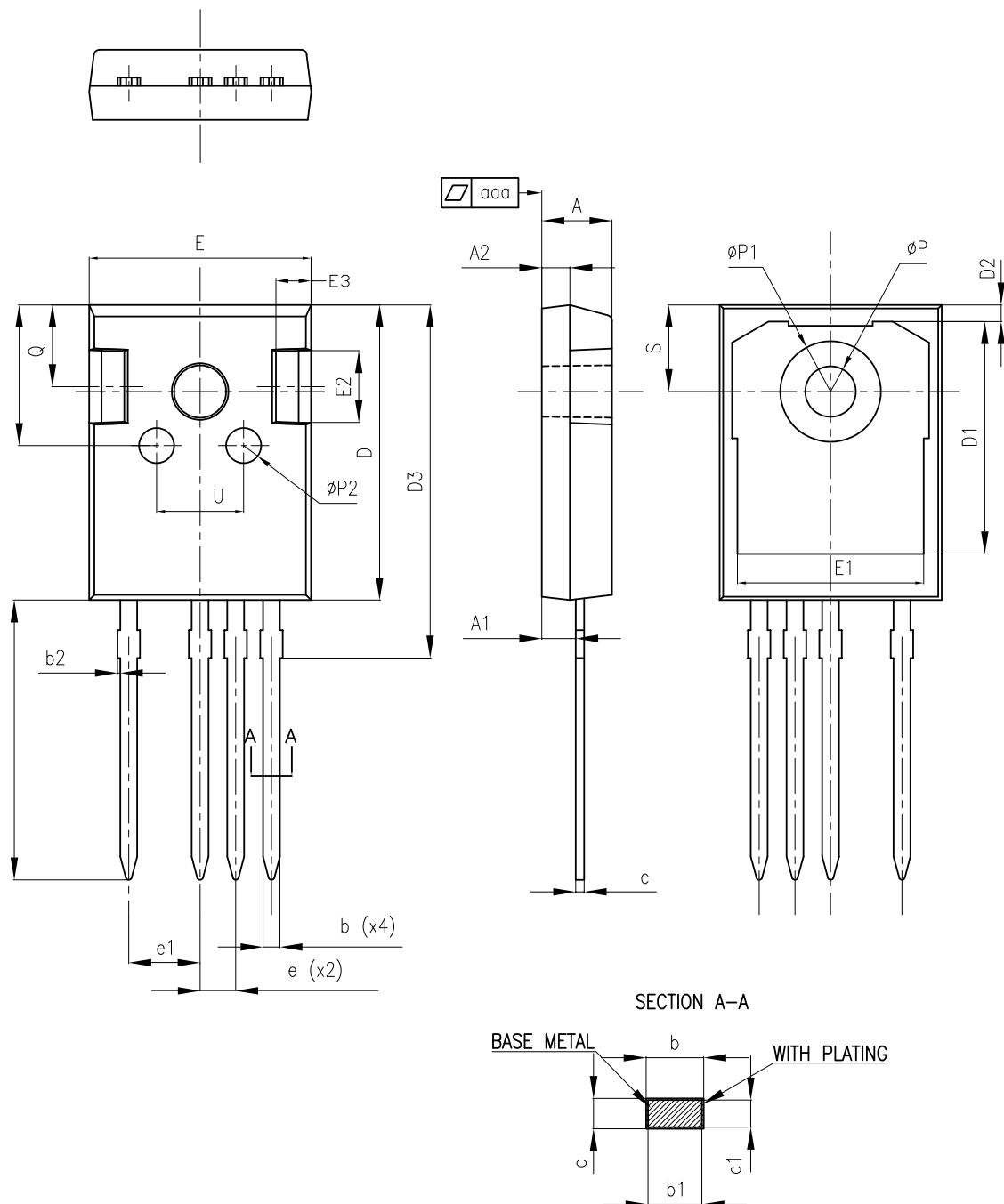
AM05540v2

4 Package information

To meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO247-4 package information

Figure 20. TO247-4 package outline



8405626_Rev_6

Table 8. TO247-4 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.29
b1	1.15	1.20	1.25
b2	0.00		0.20
c	0.59		0.66
c1	0.58	0.60	0.62
D	20.90	21.00	21.10
D1	16.25	16.55	16.85
D2	1.05	1.20	1.35
D3	24.97	25.12	25.27
E	15.70	15.80	15.90
E1	13.10	13.30	13.50
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	2.44	2.54	2.64
e1	4.98	5.08	5.18
L	19.80	19.92	20.10
P	3.50	3.60	3.70
P1			7.40
P2	2.40	2.50	2.60
Q	5.60		6.00
S		6.15	
T	9.80		10.20
U	6.00		6.40
aaa		0.04	0.10

Revision history

Table 9. Document revision history

Date	Revision	Changes
21-Oct-2015	1	First release.
18-Dec-2025	2	Updated Section 4.1: TO247-4 package information . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics.....	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information.....	9
4.1	TO247-4 package information	9
	Revision history	11

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice.

In the event of any conflict between the provisions of this document and the provisions of any contractual arrangement in force between the purchasers and ST, the provisions of such contractual arrangement shall prevail.

The purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

The purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of the purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

If the purchasers identify an ST product that meets their functional and performance requirements but that is not designated for the purchasers' market segment, the purchasers shall contact ST for more information.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2025 STMicroelectronics – All rights reserved