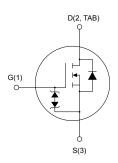


N-channel 1500 V, 1.6 Ω typ., 7 A MDmesh K5 Power MOSFET in a TO-247 package

Features



TO-247



AM01476v1_tab

Order code V _{DS}		R _{DS(on)} max.	I _D
STW12N150K5	1500 V	1.9 Ω	7 A

- Ultra-low gate charge
- Very low FoM (figure of merit)
- Zener-protected
- 100% avalanche tested

Applications

· Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



Product status link

STW12N150K5

Product summary			
Order code STW12N150K5			
Marking	12N150K5		
Package	TO-247		
Packing	Tube		



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±30	V
1-	Drain current (continuous) at T _C = 25 °C	7	A
Ι _D	Drain current (continuous) at T _C = 100 °C	4	
I _{DM} ⁽¹⁾	Drain current (pulsed)	28	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	250	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
TJ	Operating junction temperature range	-55 to 150	°C

- 1. Pulse width is limited by safe operating area.
- 2. $I_{SD} \le 7 A$, $di/dt = 100 A/\mu s$, V_{DS} (peak) $< V_{(BR)DSS}$.
- $3. \quad V_{DD} \leq 1200 \ V.$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	0.5	°C/W
R _{thJA}	Thermal resistance, junction-to-ambient	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max.)	2	Α
E _{AS}	Single pulse avalanche energy (starting $T_J = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	900	mJ

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2 Electrical characteristics

 T_C = 25 °C unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	1500	-	-	V
l	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 1500 V	-	-	1	μА
I _{DSS}		V _{GS} = 0 V, V _{DS} = 1500 V, T _C = 125 °C ⁽¹⁾	_	-	50	
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V	-	-	±10	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 100 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.5 A	-	1.6	1.9	Ω

^{1.} Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	1360	-	pF
C _{oss}	Output capacitance	$V_{DS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	80	-	pF
C _{rss}	Reverse transfer capacitance		-	0.7	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent output capacitance time related	V _{DS} = 0 to 1200 V, V _{GS} = 0 V	-	82	-	pF
C _{o(er)} ⁽²⁾	Equivalent output capacitance energy related		-	32	-	pF
Rg	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	3	-	Ω
Qg	Total gate charge	V _{DD} = 1200 V, I _D = 7 A, V _{GS} = 0 to 10 V	-	47	-	nC
Q _{gs}	Gate-source charge	(see the Figure 15. Test circuit for gate	-	8	-	nC
Q _{gd}	Gate-drain charge	charge behavior)	-	32	-	nC

^{1.} $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 750 V, I _D = 3.5 A,	-	25	-	ns
t _r	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	8	-	ns
t _{d(off)}	Turn-off delay time	(see the Figure 14. Test circuit for resistive load switching times and	-	90	-	ns
t _f	Fall time	Figure 19. Switching time waveform)	-	37	-	ns

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^{2.} $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .



Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-	-	7	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-	-	28	Α
V _{SD} ⁽²⁾	Forward on voltage	V _{GS} = 0 V, I _{SD} = 7 A	-	-	1.5	V
t _{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	302	-	ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V	-	3.71	-	μC
I _{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	24.6	-	Α
t _{rr}	Reverse recovery time	I _{SD} = 7 A, di/dt = 100 A/μs,	-	432	_	ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V, T _J = 150 °C	-	4.71	-	μC
I _{RRM}	Reverse recovery current	(see the Figure 16. Test circuit for inductive load switching and diode recovery times)	-	21.8	-	А

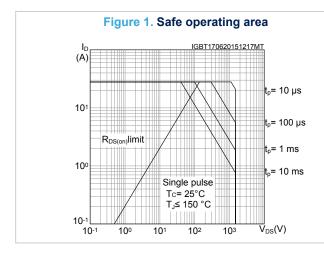
^{1.} Pulse width is limited by safe operating area.

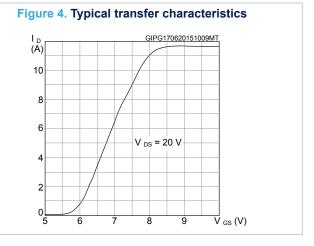
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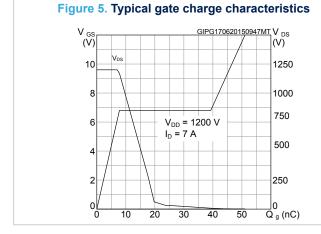
^{2.} Pulse test: pulse duration = $300 \mu s$, duty cycle 1.5%.

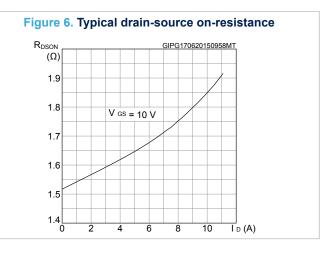


2.1 Electrical characteristics (curves)









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Figure 7. Typical capacitance characteristics

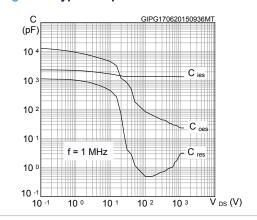


Figure 8. Normalized gate threshold vs temperature

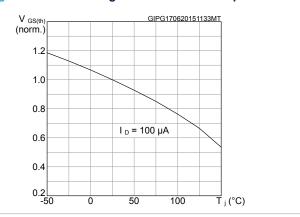


Figure 9. Normalized on-resistance vs temperature

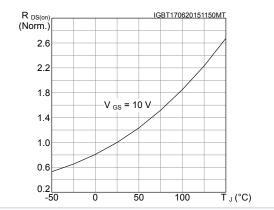


Figure 10. Normalized breakdown voltage vs temperature

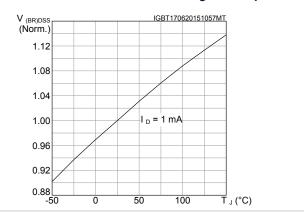


Figure 11. Typical output capacitance stored energy

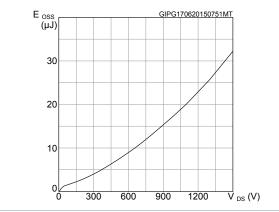
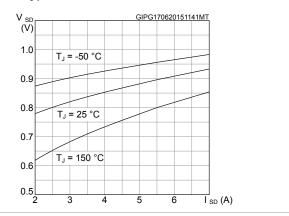


Figure 12. Typical reverse diode forward characteristics



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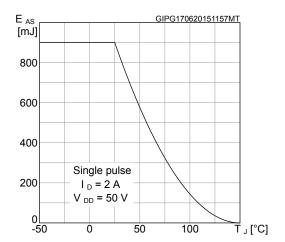


Figure 13. Maximum avalanche energy vs temperature

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3 Test circuits

Figure 14. Test circuit for resistive load switching times

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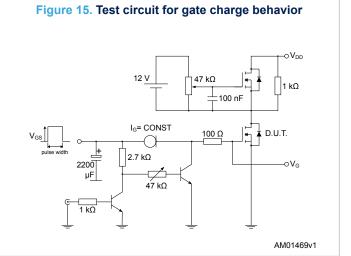
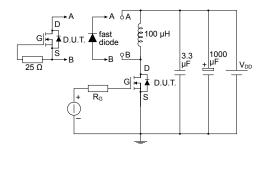


Figure 16. Test circuit for inductive load switching and diode recovery times



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Figure 17. Unclamped inductive load test circuit

Figure 18. Unclamped inductive waveform

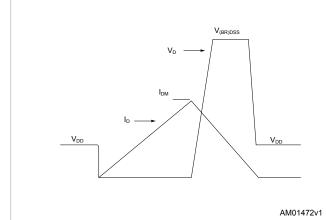
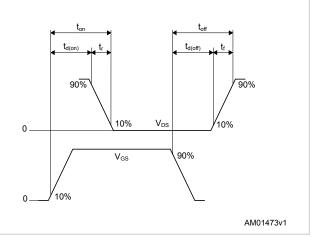


Figure 19. Switching time waveform



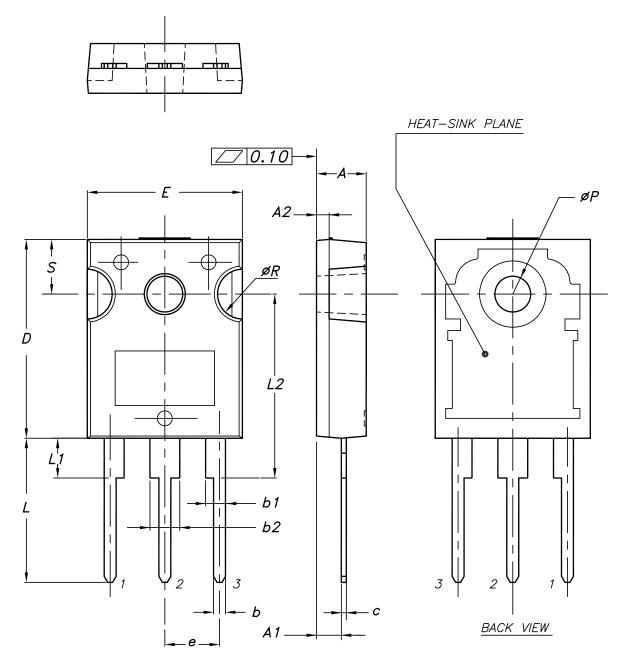
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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 package information

Figure 20. TO-247 package outline



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Table 8. TO-247 package mechanical data

Dim.	mm		
Dilli.	Min.	Тур.	Max.
Α	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
С	0.40		0.80
D	19.85		20.15
E	15.45		15.75
е	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

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Revision history

Table 9. Document revision history

Date	Version	Changes
11-May-2015	1	First release.
30-Jun-2015	2	Updated title and features in cover page. Updated Section 4: "Electrical ratings", Section 5: "Electrical characteristics". Added Section 5.1: "Electrical characteristics (curves)". Minor text changes.
07-Jul-2015	3	Updated Section 5.1: "Electrical characteristics (curves)". Minor text changes.
19-Dec-2025	4	Updated Section 4.1: TO-247 package information. Minor text changes.

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