Truly Innovative 28nm FDSOI Technology for Automotive Microcontroller Applications embedding 16MB Phase Change Memory

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Outline of Presentation

- Introduction
- Technology description
- CMOS devices suite
- PCM analytical cell
- 16MB PCM array results
- Conclusions
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Automotive Microcontrollers

Automotive MCU growth contributors:

**Advanced Powertrain:** combining Electric Motors, Thermal Engine and Transmission management

**Electrification:** smart power supporting electrification

**Gateways:** Secure communication interfaces

**ADAS:** safety microcontrollers

- eNVM trend: increase memory size due to:
  - increased software complexity
  - multiple firmware image storage

*Source: Strategy Analytics*
Microcontroller Chips for Automotive

- eNVM
- PMU
- Real MCU layout for automotive
- Analog
- LOGIC
- I/Os
Physical Mechanisms for eNVM

Charges manipulation

Atoms manipulation

Spin manipulation

© ESF3 structure from SST

GeSbTe phase diagram

Y-H Lin et al, "Excellent high T° retention of In NdxNy ReRAM by interfacial layer engineering" VLSI-TSA, 2018


eFLASH

PCRAM

Ox.RAM

STT MRAM

IEDM conference, Dec 3-5 2018, San-Francisco, CA
Phase Change Memory Principle

**Crystalline phase**

- From **SET (1)** state to **RESET (0)** state

**Amorphous phase**

- From **RESET (0)** state to **SET (1)** state

**Crystalline phase**

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**Crystal**

- Ge or Sb, Te

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**Liquid**

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**Amorphous**

- 6R, 8R, 4R, 10R

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**Crystal**

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**Current**

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**Time**
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Technology Architecture

- GST material
- heater
- Via in PCM array
- Stacked contacts in logic/SRAM
- Contact
- Thin Si film
- Thin buried oxide
- Handle substrate

PCM array

Logic/SRAM area
Process Integration Sequence

1. **<100> 45° off-axis FDSOI Substrate**
2. **HYBRID BRICK (Bulk & FDSOI)**
3. **ISOLATION (STI & well)**
4. **VT ADJUST (NMOS & PMOS)**
5. **GATE STACK (Triple GOx)**
6. **GATE PATTERNING (5V / 1V8 / 1V)**
7. **JUNCTIONS (raised SD & I^2)**
8. **SALICIDE (SiProtect & NiSi)**
9. **CONTACT (barre & hole)**
10. **PCM ELEMENT (heater & GST)**
11. **VIA-0 (to PCM & contact)**
12. **M1 WIRES (single damascene)**
13. **THIN METAL (Trench First HM)**
14. **INTERM. METAL (Trench First HM)**
15. **THICK METAL (xxxxx)**
16. **ALU PAD (Alu & passivation)**
Co-Integrated Memories Morphology

HD SRAM Cell (0.120um$^2$)

PCM Cell (0.036um$^2$)
Devices Suite - Morphology

5V Transistor

0.6µm

1.4A

BULK AREA

1.8V Transistor

0.15µm

3.4A

SOI AREA

Logic Transistor

28mm

1.6A

SOI AREA

SRAM Transistor

36mm

1.6A

SOI AREA

PCM Selector

30mm

1.6A

SOI AREA
PCM Element Morphology

Cell in X direction

Cell in Y direction
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# Devices Table

<table>
<thead>
<tr>
<th>Devices</th>
<th>Logic devices</th>
<th>SRAM devices</th>
<th>I/O devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDnom (Volt)</td>
<td>1</td>
<td>1</td>
<td>1,5 &amp; 1,8</td>
</tr>
<tr>
<td>Lmin (um)</td>
<td>0,028</td>
<td>0,036</td>
<td>0,1 &amp; 0,15</td>
</tr>
<tr>
<td>Tinv (nm)</td>
<td>1,6</td>
<td>1,6</td>
<td>3,4</td>
</tr>
<tr>
<td>VT options</td>
<td>HVT &amp; LVT</td>
<td>LL &amp; HS</td>
<td>RVT LVT</td>
</tr>
<tr>
<td>Substrate</td>
<td>FDSOI</td>
<td>FDSOI</td>
<td>FDSOI</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Devices</th>
<th>HV/Analog devices</th>
<th>ESD devices</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDnom (Volt)</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>Lmin (um)</td>
<td>0,6</td>
<td>0,048</td>
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<tr>
<td>Tinv (nm)</td>
<td>14</td>
<td>1,6</td>
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<tr>
<td>VT options</td>
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<td>RVT</td>
</tr>
<tr>
<td>Substrate</td>
<td>BULK</td>
<td>FDSOI</td>
</tr>
</tbody>
</table>
Core Oxide Transistors – Well Scheme

HIGH VT option (regular well)

LOW VT option (flip well)

Mix & match capability

VT adjust
Digital Performance & Design Flexibility

100% performance enhancement

3 decades reduction

Gate length

Fastest

Reference

FBB

Low leakage

RO delay (ps/stage)

RO IDDq (pA/stage)

Lg = 28nm

Lg = 32nm

Lg = 38nm

Low VT

Low VT @FBB=0.9V

High VT

VT adjust

1000000

100000

10000

1000

100

10

5 7 9 11 13 15
5V Transistors – Digital Characteristics

Transfer characteristic

Output characteristic

PMOS  NMOS  PMOS  NMOS

$V_{GS} = 5V$
$V_{GS} = 4V$
$V_{GS} = 3V$
$V_{GS} = 2V$
$V_{GS} = 1V$

1pA/μm
Triple Gate Oxide Devices Platform for Automotive Micro-Controllers
5V Transistor – Analog Characteristics

Matching NMOS

Matching PMOS

Flicker Noise

Matching NMOS

Matching PMOS

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5V Transistor – Gate Oxide Reliability

PMOS

NMOS

10y life time

10y life time

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5V Transistor – Hot Carrier Injection

AC TTF 1ppm worst case $T^\circ$

- $V_{DD} = 5V + 10\%$
- 10 years lifetime

- 5V PMOS transistor
- 5V NMOS transistor

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MOS Selector Requirements

• Deliver high drive current for cell programming phase (reaching GST melting point)
• Use optimum W/L ratio reducing the cell area (cost effective solution)
• Reading operation at low Voltage
• Mitigate leakage current (IOFF) of un-selected Word-Line and selected Bit-Line during writing and reading steps
MOS Selector Structure

Storage Element

Source Line

Bit Line

Source Line

Word Line

Word Line

NMOS

NMOS

Buried oxide

P WELL = Back Bias (RBB for leakage mitigation)
Enhanced MOS Selector with RBB Technique

 NMOS L=30nm T=165°C

- Optimum Area penalty
- 3Dec. Leakage reduction
- Leakage target for 1024 rows
- Lgate effect
- Body bias effect (Vbb)
1T1R Analytical Cell Description
1T1R Analytical Cell Electrical Characteristics

![Resistance Distribution]

- **LRS** (Low Resistance State) labeled as “1”
- **HRS** (High Resistance State) labeled as “0”

**Set distribution**

**Reset distribution**
Analytical Cell Endurance

Cycling algorithm

LRS trend

HRS trend

10 Mcycles
GST RESET Data Retention vs T°

N.Ciocchini et al
"Modeling Resistance Instabilities of SET and RESET States in Phase Change Memory with Ge-rich GeSbTe"
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 61, NO. 6, JUNE 2014
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16MB Test Chip & Array Organization
16MB SET & RESET States Distributions

![Graph showing normalized cell count against Iread (µA)]

- **Normalized cell count (♯)**
  - Logarithmic scale: 1E-09 to 1E+00

- **Iread [µA]**
  - Linear scale: 0 to 40

- **16MB statistics**
  - Two curves: Reset (yellow) and Set (blue)

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16MB Test Chip Reliability Figures

**ENDURANCE**

- Normalized cell count (#)
- Read Current [uA]
- Lines represent different cycle counts: 1cyc, 10cyc, 100cyc, 1Kcyc, 3Kcyc, 10Kcyc

**RESET RETENTION**

- Normalized cells count (#)
- Iread [μA]
- Lines represent different bake conditions: Bake 150°C - Fresh, Bake 150°C - 1h, Bake 150°C - 3h, Bake 150°C - 10h, Bake 150°C - 50h, Bake 150°C - 120h

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MCU Demo Chip Preliminary Results

**MCU content & specs**
- Core: 32b processor
- SRAM: 640KB
- PCM: 6MB
- T range: -40C - 165C
- Supply: 0.9-1.1V / 4.5-5.5V

**Preliminary reliability tests**
- Soldering: Pass (30/30)
- Data retention: Pass (30/30)
- Endurance (10K): Pass (30/30)
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Conclusions

• For the first time, Non volatile Phase Change Memory has been co-integrated with 28nm FDSOI technology for microcontroller applications in the Automotive market

• Triple gate oxide scheme enabling 5V transistor with FDSOI substrate for analog requirements in Automotive system

• Attractive leakage/drivability of FDSOI NMOS selector leveraging Reverse Body Biasing technique

• Fully validated 0,036um² PCM cell using optimized GST alloy showing robust endurance and good activation energy compatible with Automotive criteria (150°C achieved)

• Excellent PCM current distributions demonstrated on 16MB array before and after 150°C bake without degradation after 10k cycles
Acknowledgements

• Innovation proposed and developed by design, process, electrical characterization and product test teams from European ST sites (Rousset, Agrate and Crolles) using patents in PCM cell design and GST alloy optimization for automotive

• The authors would like to warmly thank our colleagues from CEA-LETI located in Grenoble for their strong technical expertise, PDF Solution and their constant support in deep electrical characterizations on this technology platform
Thank You for your attention!

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