

FD-SOI: a major breakthrough in the pursuit of silicon chip miniaturization

The semiconductor industry's continuing efforts to meet the ever-present demand for greater computing power are running into fundamental physical scaling issues in transistor design that limit performance.

Controlling the electrical behavior of transistors as their size shrinks to the nanometer (one billionth of a meter) scale requires adopting a new approach to transistor design called *full depletion*. More than a dozen years ago, researchers at STMicroelectronics invented the initial idea of making transistors on a substrate of ultra-thin silicon resting on an insulator. Their efforts laid the ground for the development of a fully-depleted transistor architecture that effectively bypasses many of the complexities of continuing to scale conventional (bulk CMOS) chip manufacturing technology.

A major breakthrough in the pursuit of miniaturization of electronic circuits, ST's Fully Depleted Silicon-On-Insulator (FD-SOI) technology enables energy efficient design of next-generation devices in automotive markets, such as infotainment and ADAS, while ideally suited to lead the IoT revolution on both the object and the server sides, which require the highest energy efficiency and the capability to integrate a range of digital, analog, RF, embedded memory and other functions.

FD-SOI isn't the only approach to fully depleted semiconductor technology. An alternative approach, called FinFETs, essentially rotates the 2D planar transistors 90 degrees, building 3D transistors into the bulk substrate. This 3D approach requires disruptive changes to design techniques and process technologies, unlike ST's planar (2D) FD-SOI that uses already-familiar conventional manufacturing techniques and processes, making production of fully-depleted semiconductors cheaper and easier. FD-SOI is simpler, but the benefits don't stop there.

FD-SOI also benefits from unique features of the technology, including the absence of parasitic effects and dopants in the conduction channel. As a result, FD-SOI transistors can operate at significantly higher frequencies than conventional CMOS transistors. In fact, ST's 28nm FD-SOI Technology Platform, manufactured at its Crolles 300mm facility in France, can deliver 30% higher speed at the same power and up to 50% greater power efficiency at the same performance as comparable bulk processes—at similar cost.

And it is cooler, too: FD-SOI transistors are more power-efficient than transistors manufactured in bulk CMOS, so they dissipate less heat than the equivalent bulk technology. As a result, end-user devices run cooler and last longer.

With a pipeline of designs in process, ST's FD-SOI technology is ready for high-volume manufacturing and Samsung, one of the world's largest foundries, has licensed ST's 28nm technology, opening a path to the holy grail of electronics—outstanding performance with longer battery life and assured high-volume capacity. ST has captured numerous opportunities for FD-SOI in both the consumer space and ASICs for a range of applications.

A fruit of scientific genius, strategic vision, and long-standing determination, FD-SOI industrialization strengthens ST's role in shaping the future of the microelectronics industry.

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